

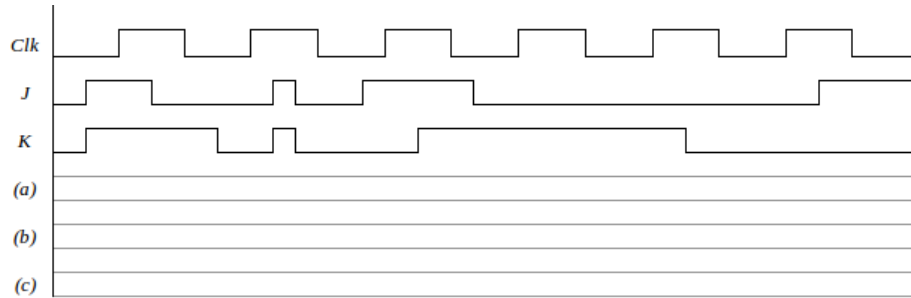
Curso: Bacharelado em Ciência da Computação
Disciplina: Introdução aos Sistemas Lógicos
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Lista de Exercícios 3

Exercícios Teóricos

1. Identify the following statements as either true or false:
 - (a) The inputs to a level-sensitive latch always affect its outputs.
 - (b) Flip-flop delays from the change in the clock edge to the change in the output are typically shorter than flip-flop hold times, so shift registers can be constructed from cascaded flip-flops.
 - (c) Assuming zero setup and hold times, clocked latches and flip-flops produce the same outputs as long as the inputs do not change while the clock is asserted.
 - (d) A master/slave flip-flop behaves similarly to a clocked latch, except that its output can change only near the rising edge of the clock.
 - (e) An edge-triggered D flip-flop requires more internal gates than a similar device constructed from a J - K master/slave flip-flop.
2. Any flip-flop type can be implemented from another type with suitable logic applied to the latter's inputs.
 - (a) Show how to implement a T flip-flop starting with a J - K flip-flop.
 - (b) Show how to implement a T flip-flop starting with a D flip-flop.
3. Given the input and clock transitions in the figure below, draw a waveform for the output of a J - K device, assuming:
 - a. It is a master/slave flip-flop.
 - b. It is a positive edge-triggered flip-flop.
 - c. It is a negative edge-triggered flip-flop. You may assume 0 setup, hold, and propagation times, and that the initial state of the flip-flop is 0.
4. Design the basic cell of a universal shift-register to the following specifications. The internal storage elements will be positive edge-triggered D flip-flops. Besides the clock, the shifter stage has two external control inputs, S_0 and S_1 , and three external data inputs, SR , SL , and DI . SR is input data being shifted into the cell from the right, SL is data being



shifted from the left, and DI is parallel load data. The current value of the flip-flop will be replaced according to the following settings of the control signals: $S0 = S1 = 0$: replace D with DI ; $S0 = 0, S1 = 1$: replace D with SL ; $S0 = 1, S1 = 0$: replace D with SR ; $S0 = S1 = 1$: hold the current state. Draw a schematic for this basic shifter cell.

5. Design a 2-bit counter that behaves according to the two control inputs I_0 and I_1 as follows: $I_0, I_1 = 0, 0$: stop counting; $I_0, I_1 = 0, 1$: count up by one; $I_0, I_1 = 1, 0$: count down by one; $I_0, I_1 = 1, 1$: count by two.
 - a. Draw the state diagram and state transition table.
 - b. Implement the counter using T flip-flops, D flip-flops, and J - K flip-flops.
6. Consider the design of a 4-bit BCD counter that counts in the following sequence: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, and then back to 0000, 0001, etc.
 - a. Draw the state diagram and next-state table.
 - b. Implement the counter using D flip-flops, toggle flip-flops, S - R flip-flops, and J - K flip-flops.
 - c. Implement the counter making it self-starting just for the D flip-flop case.