DCC007 – Organização de Computadores II

# Aula 9 – Superescalar 3

**Prof. Omar Paranaiba Vilela Neto**

# Introdução

- Processadores estudados até aqui estão limitados a CPI ≥ 1

- Processadores superescalares **permitem CPI < 1**
  - Executam múltiplas instruções em paralelo

- Tipos de processadores superescalares
  - In-order
  - Out-of-order

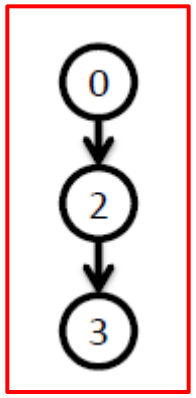
# Introdução

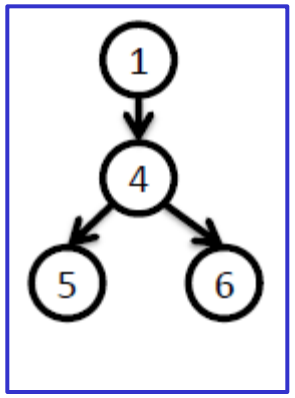

| Name | Frontend | Issue | Writeback | Commit | |
|---|---|---|---|---|---|
| I4 | IO | IO | IO | IO | Fixed Length Pipelines<br>Scoreboard |
| I2O2 | IO | IO | OOO | OOO | Scoreboard |
| I2OI | IO | IO | OOO | IO | Scoreboard,<br>Reorder Buffer, and Store Buffer |
| I03 | IO | OOO | OOO | OOO | Scoreboard and Issue Queue |
| IO2I | IO | OOO | OOO | IO | Scoreboard, Issue Queue,<br>Reorder Buffer, and Store Buffer |

IO – In-order
OOO – Out-of-Order

# Motivação

```
0 MUL    R1, R2, R3
1 ADDIU R11,R10,1
2 MUL    R5, R1, R4
3 MUL    R7, R5, R6
4 ADDIU R12,R11,1
5 ADDIU R13,R12,1
6 ADDIU R14,R12,2
```

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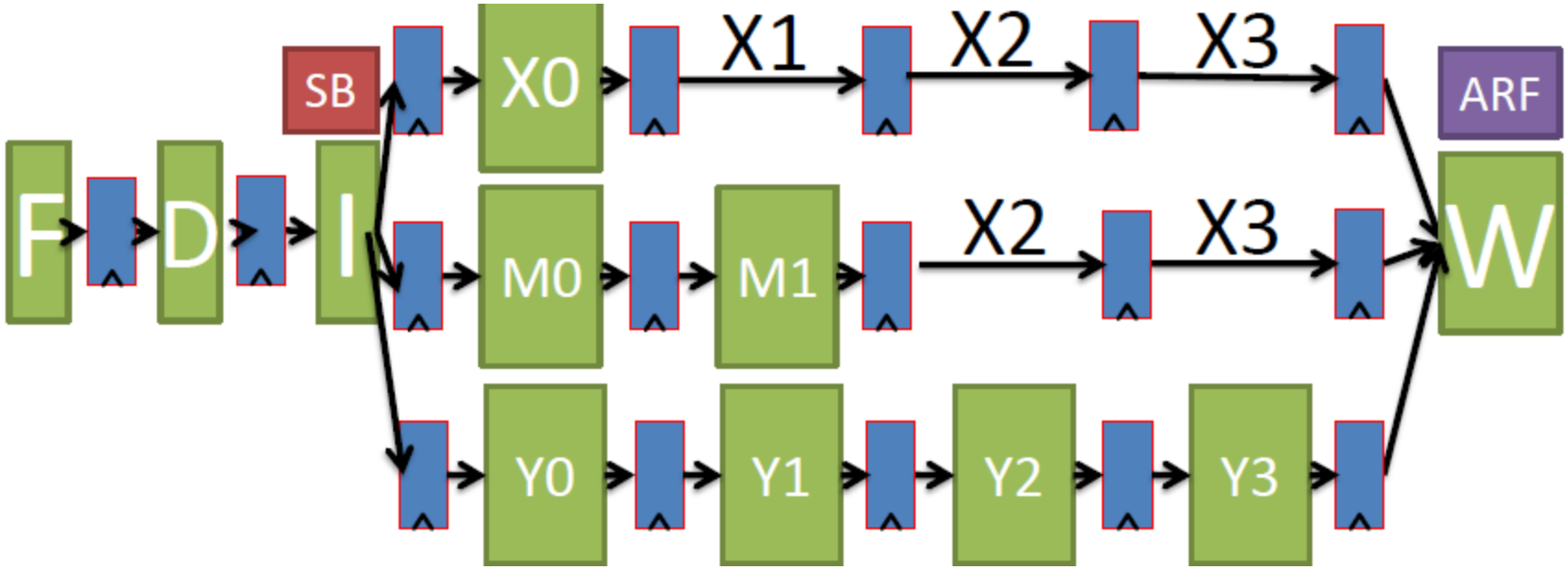
- Duas sequências independentes
  - Permite flexibilizar a ordem em que instruções são planejadas

- Estaticamente em Software
- Dinamicamente em Hardware

# Processador I4




| | | |
|---|---|---|
| ARF | R | W |
| SB | R/W | W |

```
0 MUL   R1, R2, R3 F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1     F  D  I  X0 X1 X2 X3 W
2 MUL   R5, R1, R4       F  D  I  I  I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6          F  D  D  D  I  I  I  I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1              F  F  F  D  D  D  D  I  X0 X1 X2 X3 W
5 ADDIU R13,R12,1                       F  F  F  F  D  I  X0 X1 X2 X3 W
6 ADDIU R14,R12,2                                   F  D  I  X0 X1 X2 X3 W
```

```
Cyc  D I        4 3 2 1 0     Dest Regs
1    0
2    1 0
3    2 1        1             R1
4               1 1             R11
5                 1 1
6    3 2            1 1
7               1     1 1           R5
8                 1     1
9                   1
10   4 3              1
11   5 4        1           1  R7
12   6 5        1 1               R12
13     6        1 1 1                 R13
14              1 1 1 1                  R14
15                1 1 1 1
16                  1 1 1
17                    1 1
18                      1
```

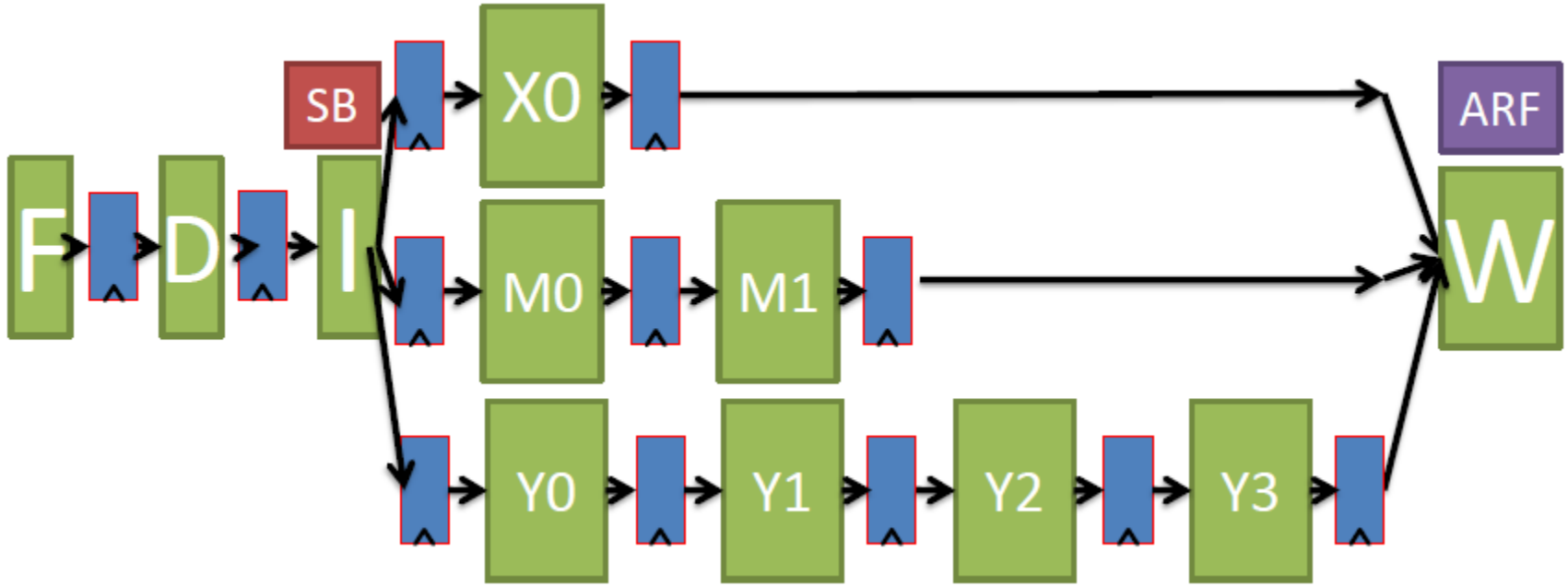
**D**: Qual instrução em Decode.

**I**: Qual instrução em Disparo.

**0 a 4**: Onde está o dado no pipeline da Unidade Funcional.

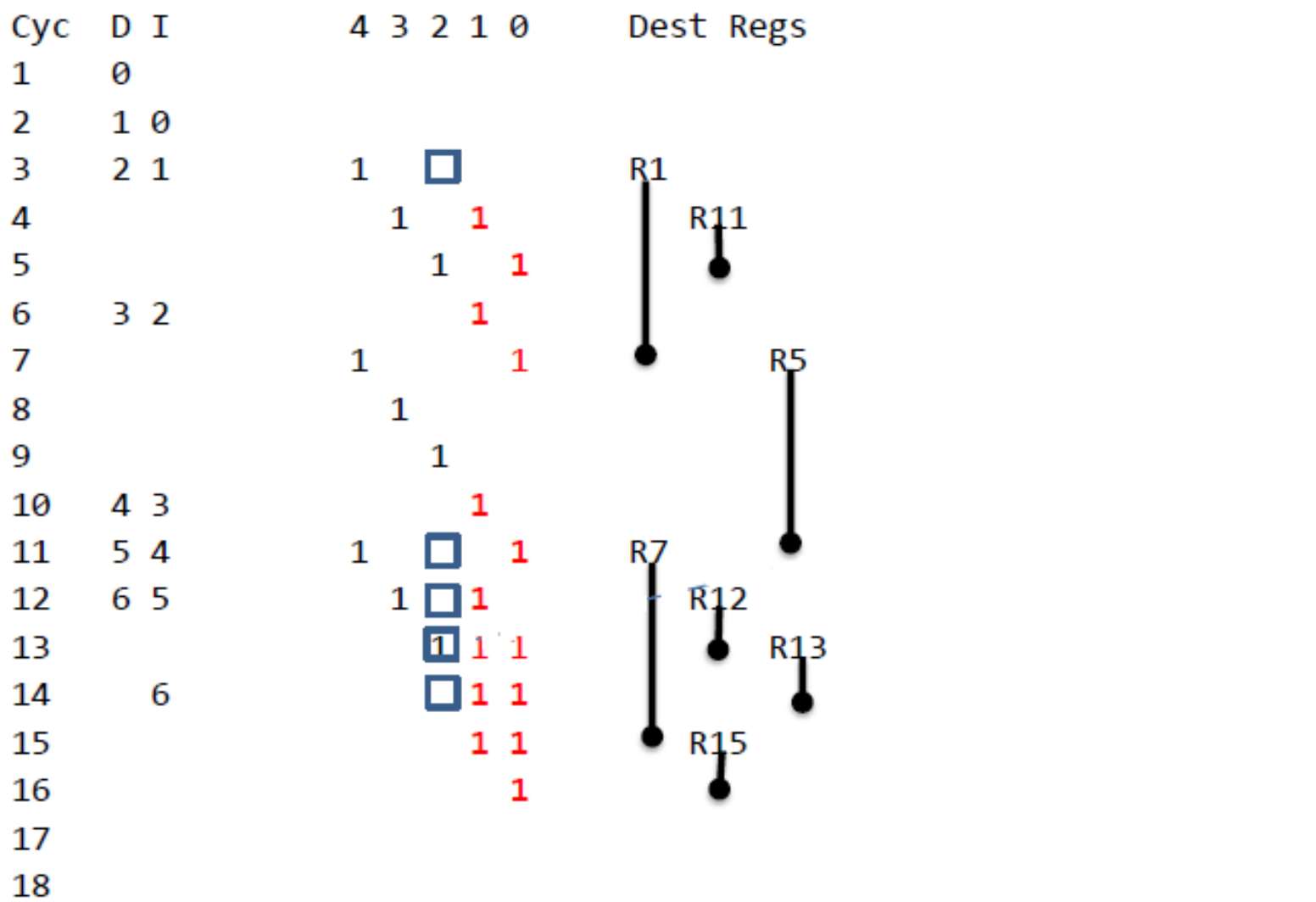
**Vermelho**: Dado está disponível.

# Processador I2O2

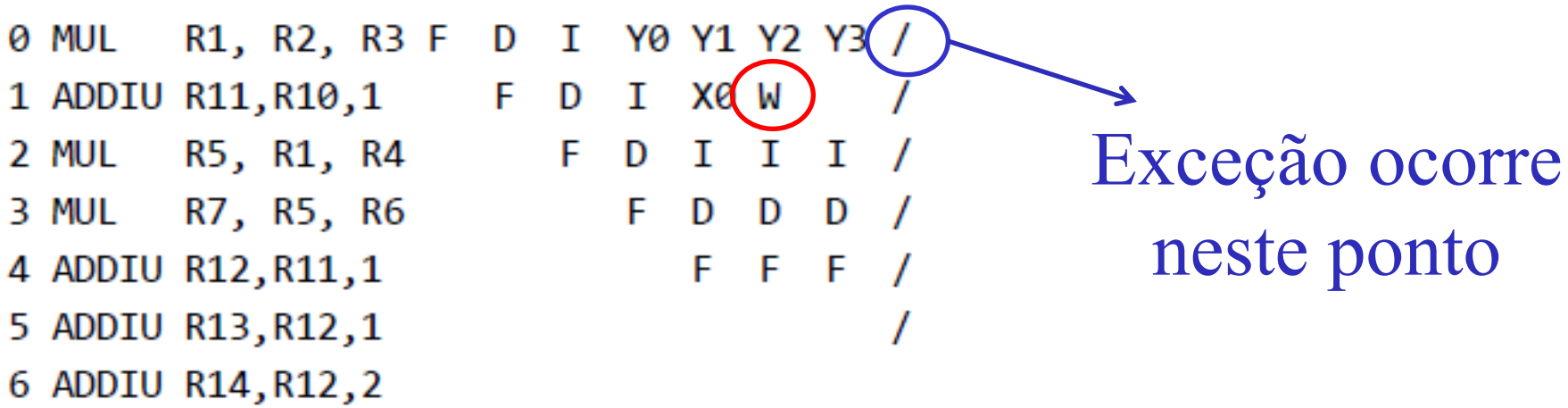



| | | | |
|---|---|---|---|
| ARF | | R | W |
| SB | R | R/W | W |

```
0 MUL   R1, R2, R3 F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1     F  D  I  X0 W
2 MUL   R5, R1, R4       F  D  I  I  I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6          F  D  D  D  I  I  I  I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1              F  F  F  D  D  D  D  I  X0 W
5 ADDIU R13,R12,1                       F  F  F  F  D  I  X0 W
6 ADDIU R14,R12,2                                   F  D  I  I X0 W
```

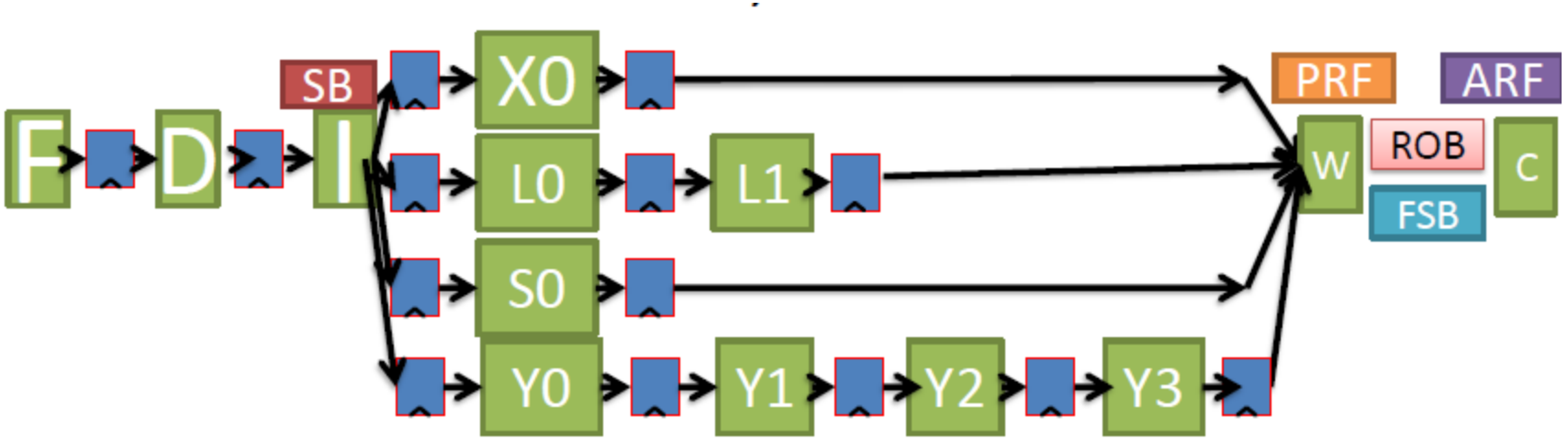


# Problema com exceção



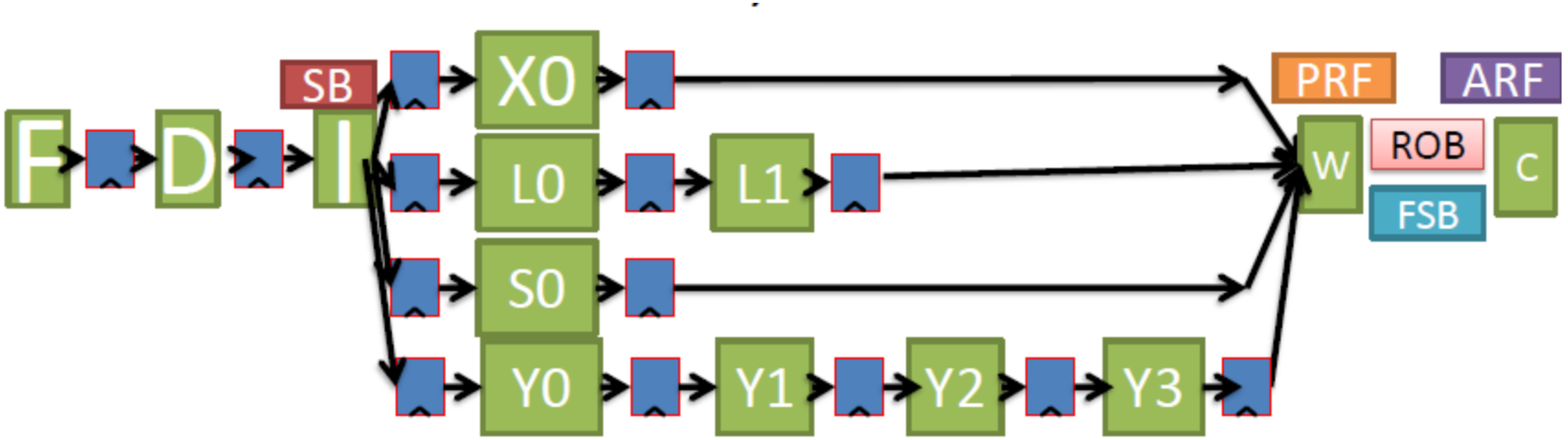

- Limits certain types of exceptions.

# Processador I2OI




- PRF(Physical Register File): Future File – É especulativo: valores podem ser descartados.
- ROB (Reorder Buffer): Garante a escrita dos valores em ordem, mesmo que calculados fora de ordem.
- FSB (Finished Store Buffer): Faz a escrita da memória ocorrer mais tarde.

# Processador I2OI




| | | | | | |
|---|---|---|---|---|---|
| ARF | | | | | W |
| SB | | R/W | | W | |
| PRF | | R | | W | |
| ROB | R/W | | | W | R/W |
| FSB | | | | W | R/W |

# Reorder Buffer Básico

| State | S | ST | V | Preg |
|---|---|---|---|---|
| -- | | | | |
| P | 1 | | | |
| F | 1 | | | |
| P | 1 | | | |
| P | | | | |
| F | | | | |
| P | | | | |
| P | | | | |
| -- | | | | |
| -- | | | | |

**State**: (Free, Pending, Finished)
**S**: especulativo;
**ST**: Store bit;
**V**: Physical Register File Specifier Valid;
**Preg**: Physical Register File Specifier

# Reorder Buffer Básico

| State | S | ST | V | Preg |
|---|---|---|---|---|
| -- | | | | |
| P | 1 | | | |
| F | 1 | | | |
| P | 1 | | | |
| P | | | | |
| F | | | | |
| P | | | | |
| P | | | | |
| -- | | | | |
| -- | | | | |

Próxima instrução vem aqui.

Fim do ROB

Especulação pq branch está sendo processado.

Escreveu no ROB fora de ordem

Início do ROB

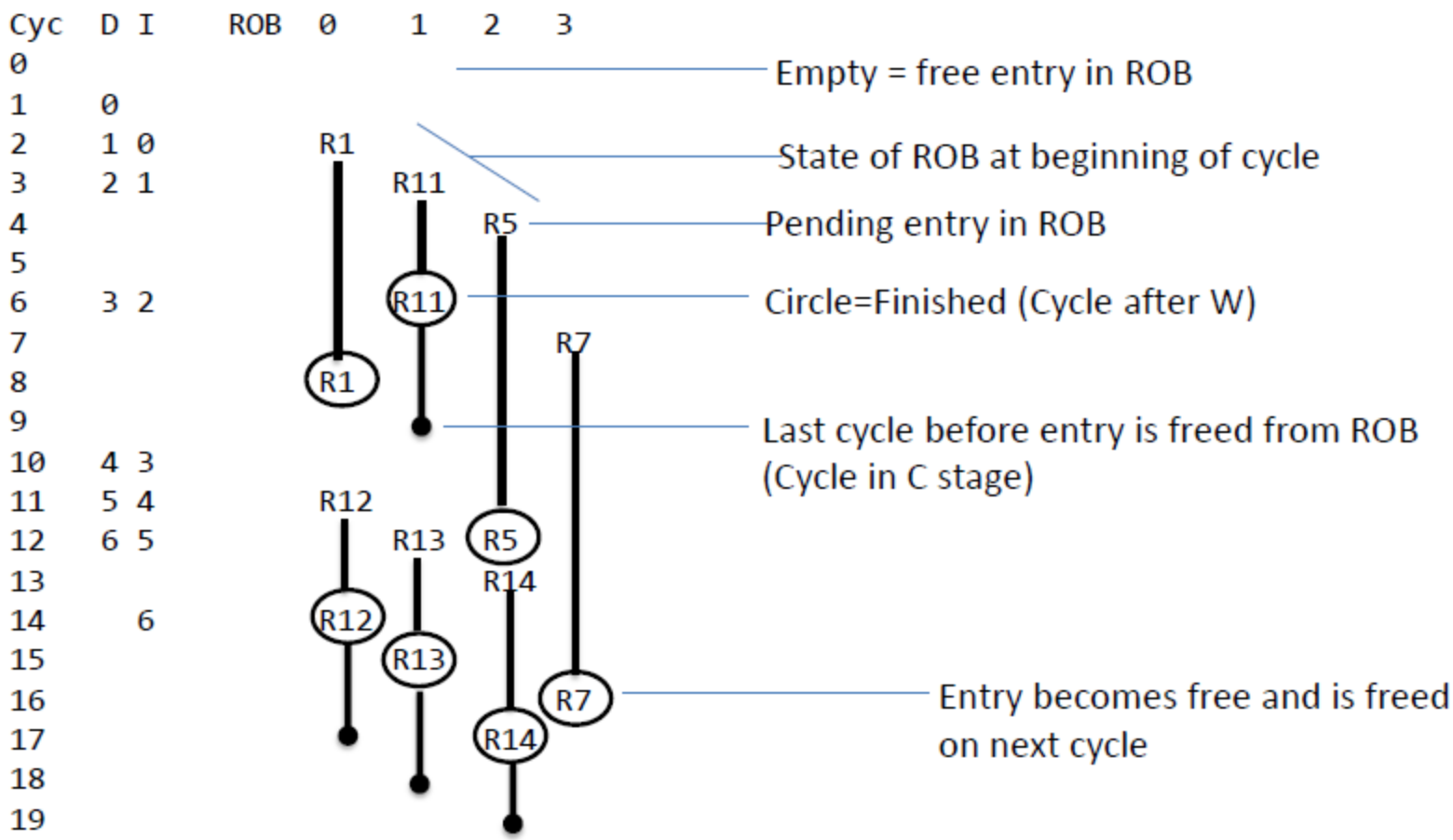
O estágio commit espera a instrução do início terminar.

**State**: (Free, Pending, Finished)
**S**: especulativo;
**ST**: Store bit;
**V**: Physical Register File Specifier Valid;
**Preg**: Physical Register File Specifier

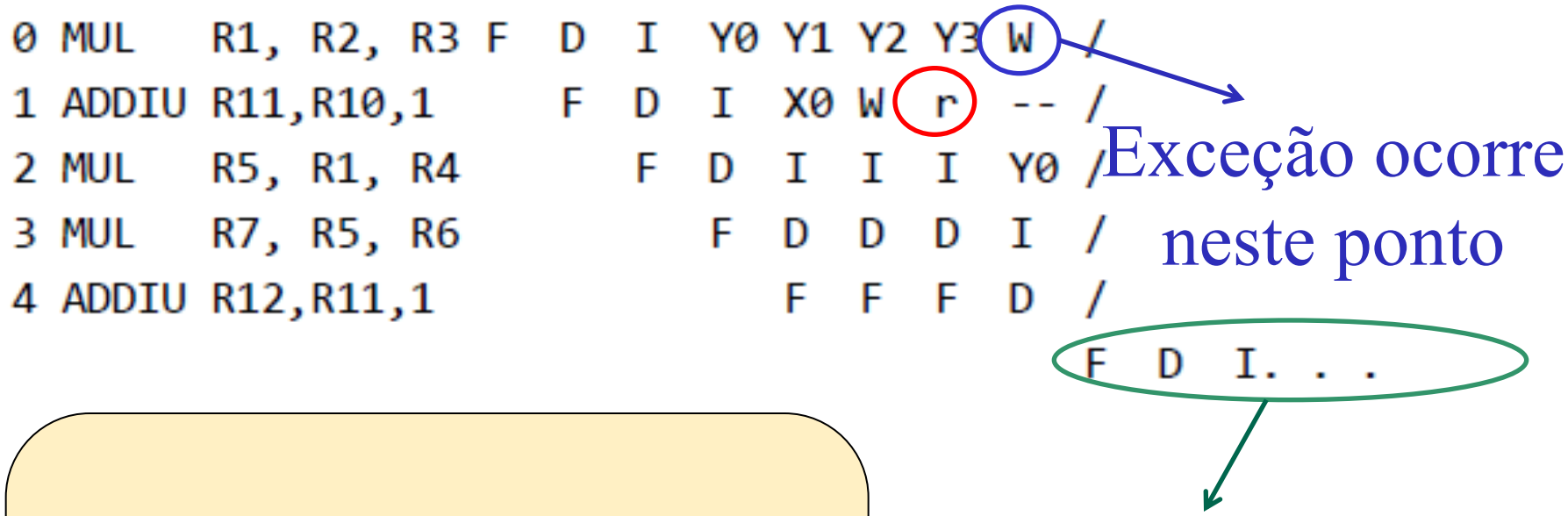
# Finished Store Buffer Básico


- Só necessita de uma entrada se suportamos apenas uma instrução de memória por vez.
- Entrada única de FSB faz alocação trivial.
- Se dermos suporte a mais de uma instrução de memória por vez, temos que nos preocupar com endereços (e encaminhamentos) de load/store.

```
0 MUL   R1, R2, R3 F  D  I  Y0 Y1 Y2 Y3 W  C
1 ADDIU R11,R10,1     F  D  I  X0 W  r        C
2 MUL   R5, R1, R4       F  D  I  I  I  Y0 Y1 Y2 Y3 W  C
3 MUL   R7, R5, R6          F  D  D  D  I  I  I  I  Y0 Y1 Y2 Y3 W  C
4 ADDIU R12,R11,1              F  F  F  D  D  D  D  I  X0 W  r        C
5 ADDIU R13,R12,1                       F  F  F  F  D  I  X0 W  r        C
6 ADDIU R14,R12,2                                   F  D  I  I  X0 W  r     C
```



# Problema com exceção




Não ocorreu o commit, logo o estado da máquina pode ser recuperado pelo ARF e PRF.

# O que ocorre com branches?

Option 2

```
0 BEQZ  R1, target F  D  I  X0 W  C
1 ADDIU R11,R10,1     F  D  I  X0 /
2 ADDIU R5, R1, R4       F  D  I  /
3 ADDIU R7, R5, R6          F  D  /
T ADDIU R12,R11,1              F  D  I . . .
```

Mata as instruções assim que branch finaliza (commit)

Option 1

```
0 BEQZ  R1, target F  D  I  X0 W  C
1 ADDIU R11,R10,1     F  D  I  -
2 ADDIU R5, R1, R4       F  D  -
3 ADDIU R7, R5, R6          F  -
T ADDIU R12,R11,1              F  D  I . . .
```

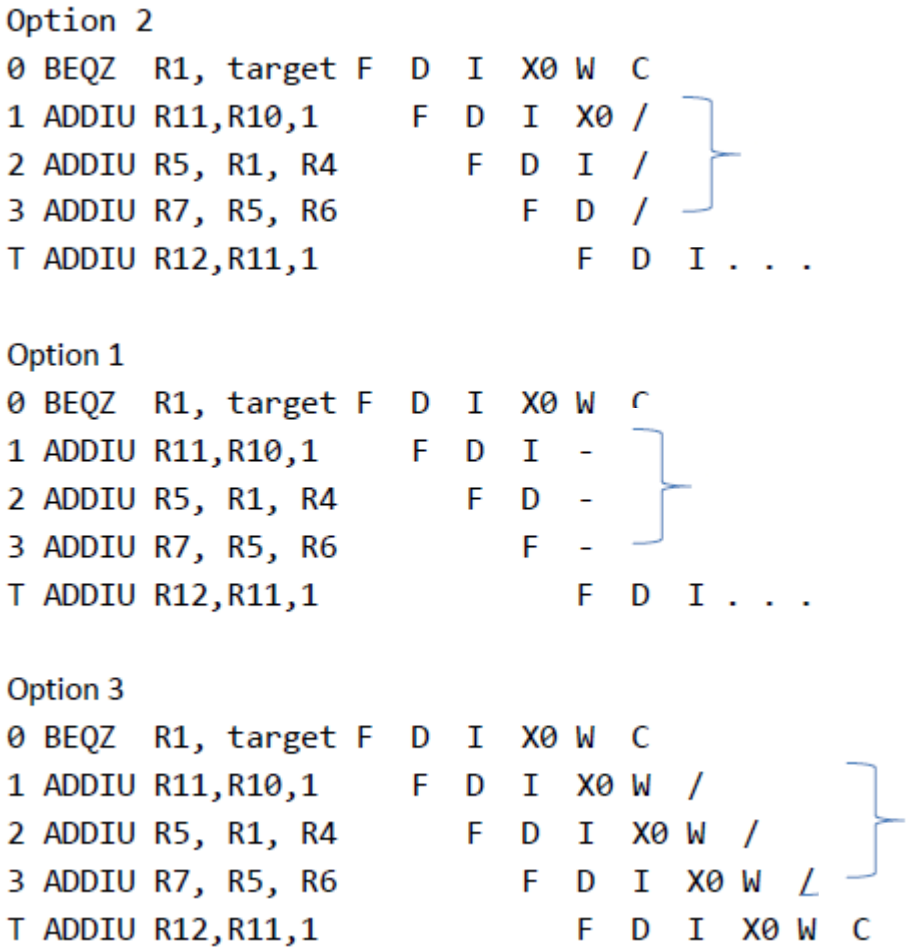
Mata as instruções imediatamente

Option 3

```
0 BEQZ  R1, target F  D  I  X0 W  C
1 ADDIU R11,R10,1     F  D  I  X0 W  /
2 ADDIU R5, R1, R4       F  D  I  X0 W  /
3 ADDIU R7, R5, R6          F  D  I  X0 W  /
T ADDIU R12,R11,1              F  D  I  X0 W  C
```

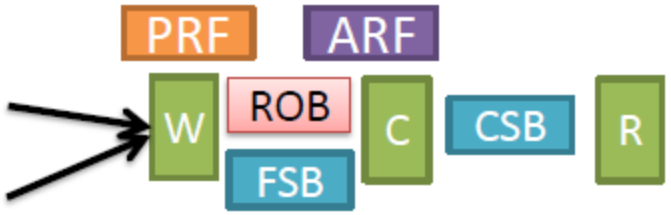
Mata as instruções apenas no commit

# O que ocorre com branches?




| | Eficiência | Complexidade |
|---|---|---|
| Option 2 | Intermediário | Intermediário |
| Option 1 | Mais eficiente | Mais complexo |
| Option 3 | Menos eficiente | Menos complexo |

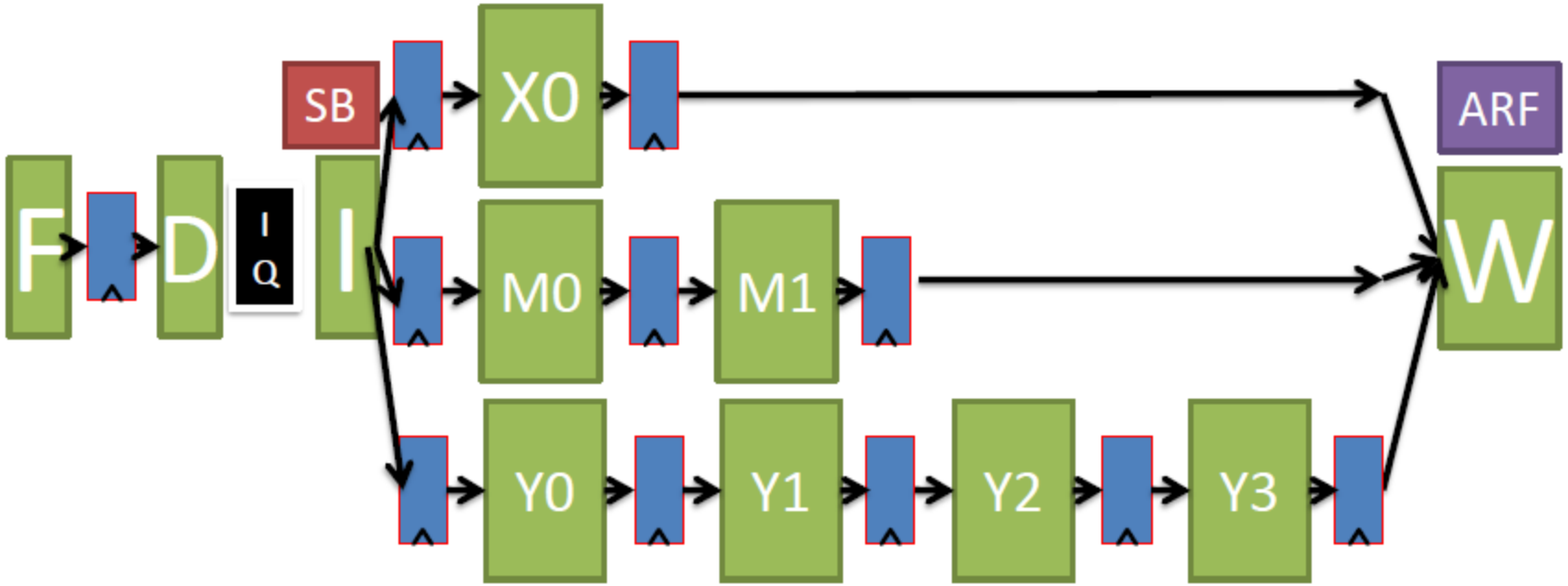
# Evitando stall em miss de Store




CSB – Committed Store Buffer

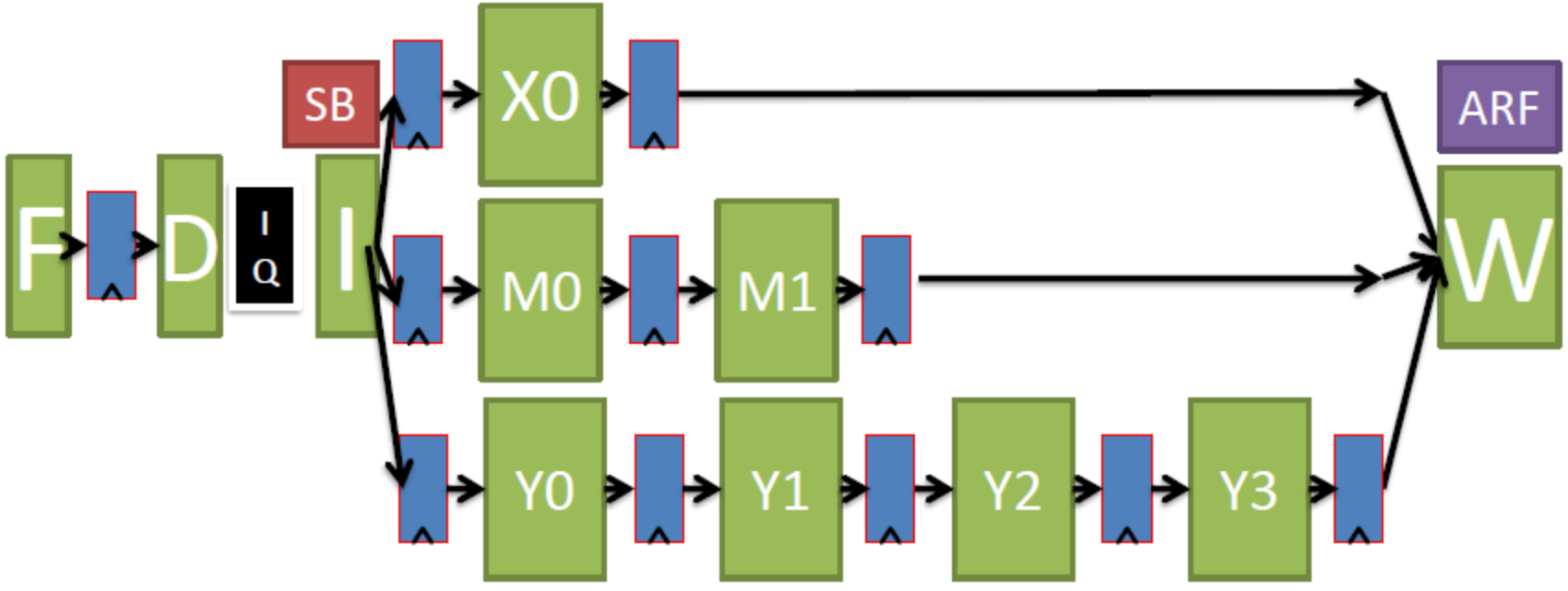
```
0 OpA    F  D  I  X0 W  C
1 SW        F  D  I  S0 W  C  C  C  C
2 OpB          F  D  I  X0 W  W  W  W  C
3 OpC             F  D  I  X  X  X  X  W  C
4 OpD                F  D  I  I  I  I  X  W  C

With Retire Stage
0 OpA    F  D  I  X0 W  C
1 SW        F  D  I  S0 W  C  R  R  R
2 OpB          F  D  I  X0 W  C
3 OpC             F  D  I  X  W  C
4 OpD                F  D  I  X  W  C
```

# Processador IO3



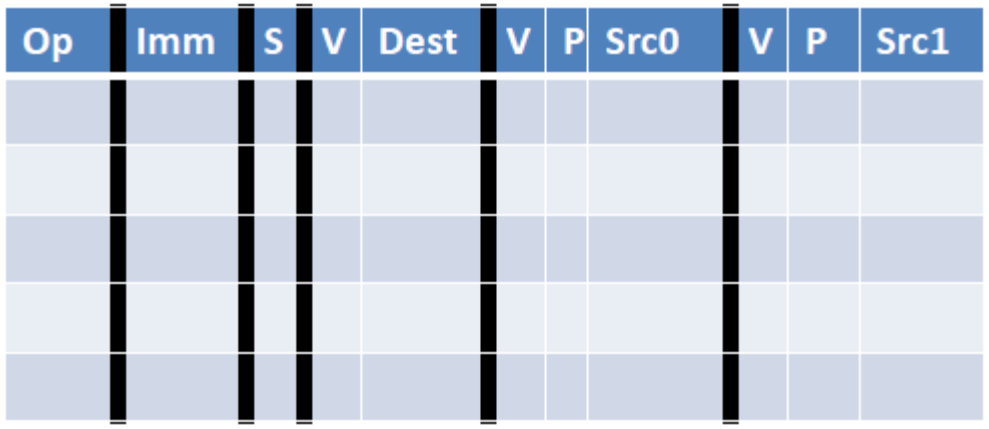

- **IQ (Issue Queue):** Dispara as instruções fora de ordem.

# Processador IO3




| | | | |
|---|---|---|---|
| ARF | | R | W |
| SB | R | R/W | W |
| I Q | W | R/W | W |

# Issue Queue Básico

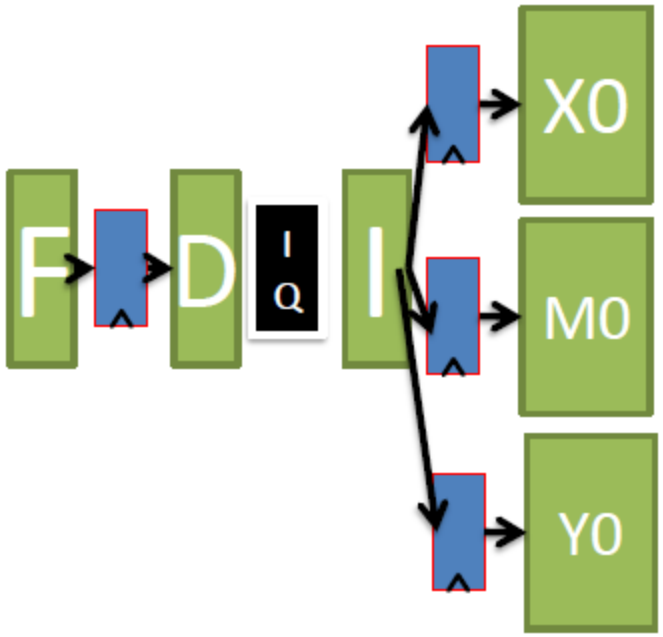



**Op**: Opcode
**Imm**: Imediato
**S**: bit especulativo
**V**: Válido (Existe no Src e Dest)
**P**: Pendente

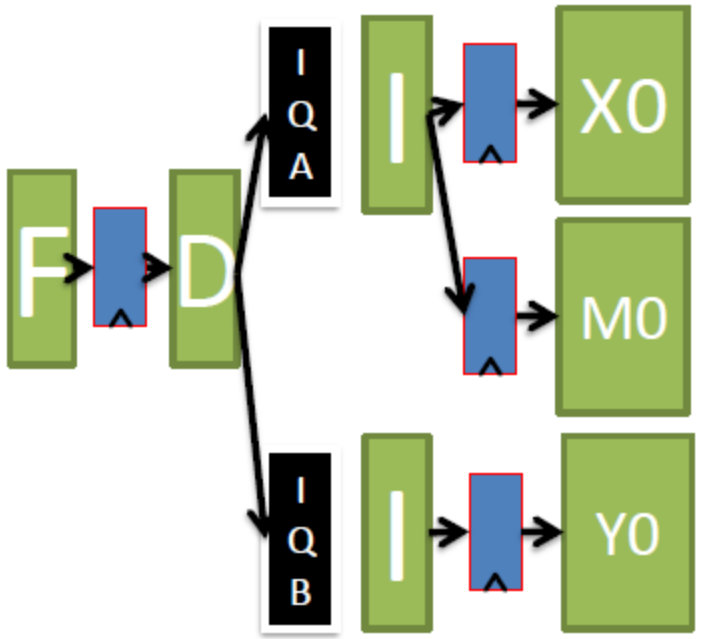
**Instrução Pronta** = (!VSrc0 || !PSrc0) && (!VSrc1 || !PSrc1) && Sem Hazard Estrutural

**Para alto desempenho**: Considerar encaminhamentos

# Issue Queue Centralizado vs Distribuído




Centralizado




Distribuído

# Scoreboard Avançado

Data Avail.

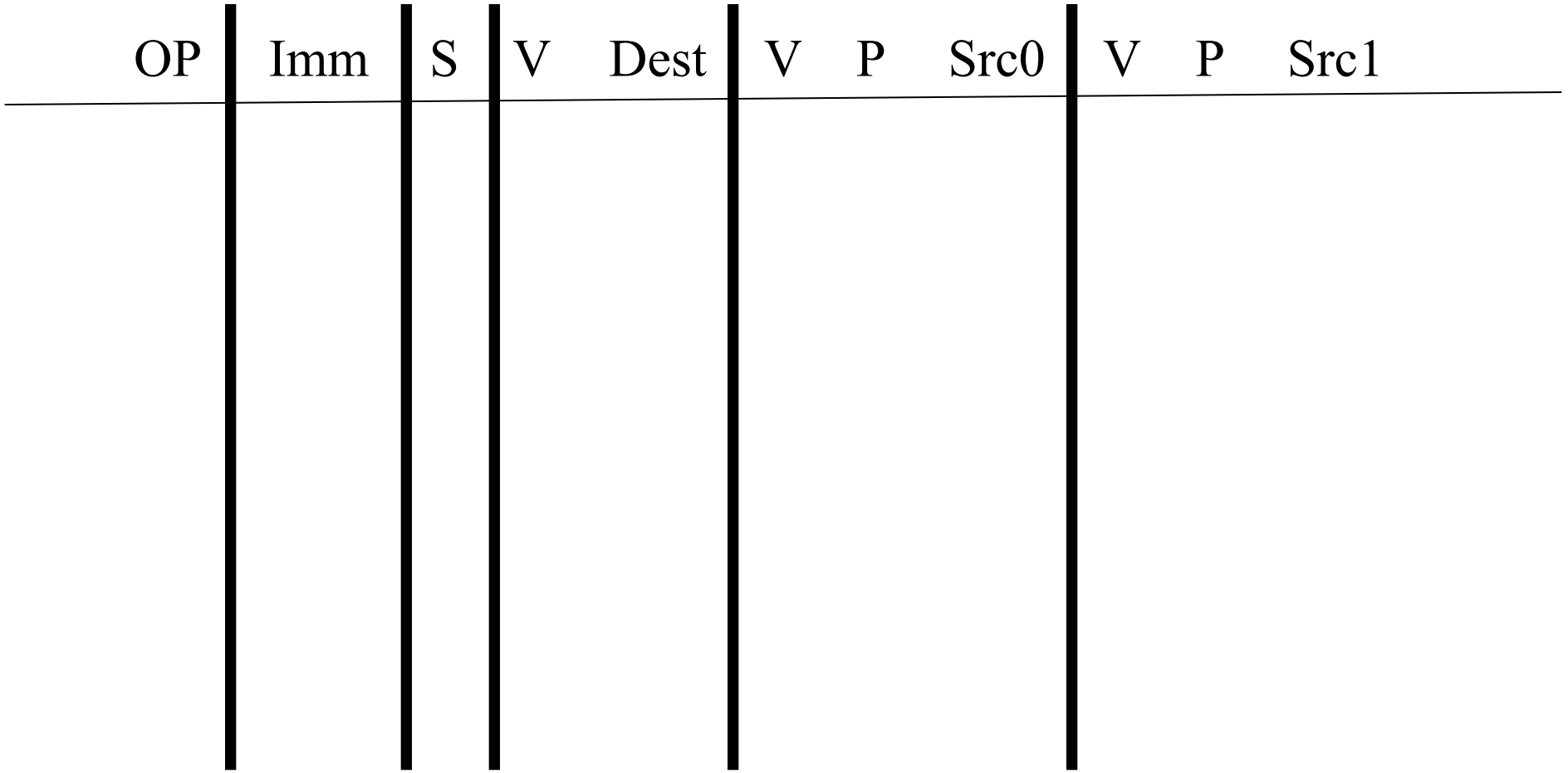
| | P | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| R1 | | | | | | |
| R2 | | | | | | |
| R3 | | | | | | |
| ... | | | | | | |
| R31 | | | | | | |

**P**: Pendente (Escrita a caminho)
**Data Avail.**: Onde está o dado no pipeline e em qual unidade funcional?

- Data Avail. Agora contém o **identificador da Unidade Funcional**;
- Um valor **não vazio na coluna zero** significa que a Unidade Funcional está na fase **write back**;
- Dados em Data Avail. **Deslocam para a direita**.


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 MUL R1, R2, R3 F D I Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1 F D I X0 W
2 MUL R5, R1, R4 F D i I Y0 Y1 Y2 Y3 W
3 MUL R7, R5, R6 F D i I Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1 F D i I X0 W
5 ADDIU R13,R12,1 F D i I X0 W
6 ADDIU R14,R12,2 F D i I X0 W
Em fase de espera no IQ
Hazard Estrutural

```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3 F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1     F  D  I  X0 W
2 MUL   R5, R1, R4       F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6          F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1              F  D  i  I  X0 W
5 ADDIU R13,R12,1                 F  D  i  I  X0 W
6 ADDIU R14,R12,2                    F  D  i        I  X0 W
```



```
                        0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3      F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1          F  D  I  X0 W
2 MUL   R5, R1, R4            F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6               F  D  i                 I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                   F  D  i  I  X0 W
5 ADDIU R13,R12,1                      F  D  i  I  X0 W
6 ADDIU R14,R12,2                         F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |

```
                        0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3      F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1          F  D  I  X0 W
2 MUL   R5, R1, R4            F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6            F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                F  D  i  I  X0 W
5 ADDIU R13,R12,1                   F  D  i  I  X0 W
6 ADDIU R14,R12,2                      F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |

```
                        0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3      F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1          F  D  I  X0 W
2 MUL   R5, R1, R4            F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6               F  D  i                 I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                F  D  i  I  X0 W
5 ADDIU R13,R12,1                   F  D  i  I  X0 W
6 ADDIU R14,R12,2                      F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 1 | R1 | 1 | 0 | R4 |

```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3 F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1     F  D  I  X0 W
2 MUL   R5, R1, R4       F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6          F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1           F  D  i  I  X0 W
5 ADDIU R13,R12,1           F  D  i  I  X0 W
6 ADDIU R14,R12,2              F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 1 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 1 | R5 | 1 | 0 | R6 |

```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3    F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1        F  D  I  X0 W
2 MUL   R5, R1, R4          F  D  i  I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6             F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                 F  D  i  I  X0 W
5 ADDIU R13,R12,1                    F  D  i  I  X0 W
6 ADDIU R14,R12,2                       F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 1 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 1 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |

```
                        0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3 F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1     F  D  I  X0 W
2 MUL   R5, R1, R4       F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6          F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1              F  D  i  I  X0 W
5 ADDIU R13,R12,1                 F  D  i  I  X0 W
6 ADDIU R14,R12,2                    F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 0 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 1 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |
| 5 | 1 | 0 | 1 | R13 | 1 | 1 | R12 | 0 | X | X |

```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3    F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1        F  D  I  X0 W
2 MUL   R5, R1, R4          F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6             F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                 F  D  i  I  X0 W
5 ADDIU R13,R12,1                    F  D  i  I  X0 W
6 ADDIU R14,R12,2                       F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 0 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 1 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |
| 5 | 1 | 0 | 1 | R13 | 1 | 1 | R12 | 0 | X | X |
| 6 | 2 | 0 | 1 | R14 | 1 | 1 | R12 | 0 | X | X |

```
                        0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3      F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1          F  D  I  X0 W
2 MUL   R5, R1, R4            F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6               F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                   F  D  i  I  X0 W
5 ADDIU R13,R12,1                      F  D  i  I  X0 W
6 ADDIU R14,R12,2                         F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 0 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 1 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |
| 5 | 1 | 0 | 1 | R13 | 1 | 0 | R12 | 0 | X | X |
| 6 | 2 | 0 | 1 | R14 | 1 | 0 | R12 | 0 | X | X |

```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3    F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1        F  D  I  X0 W
2 MUL   R5, R1, R4          F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6             F  D  i                 I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1              F  D  i  I  X0 W
5 ADDIU R13,R12,1                 F  D  i  I  X0 W
6 ADDIU R14,R12,2                    F  D  i     I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 0 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 1 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |
| 5 | 1 | 0 | 1 | R13 | 1 | 0 | R12 | 0 | X | X |
| 6 | 2 | 0 | 1 | R14 | 1 | 0 | R12 | 0 | X | X |

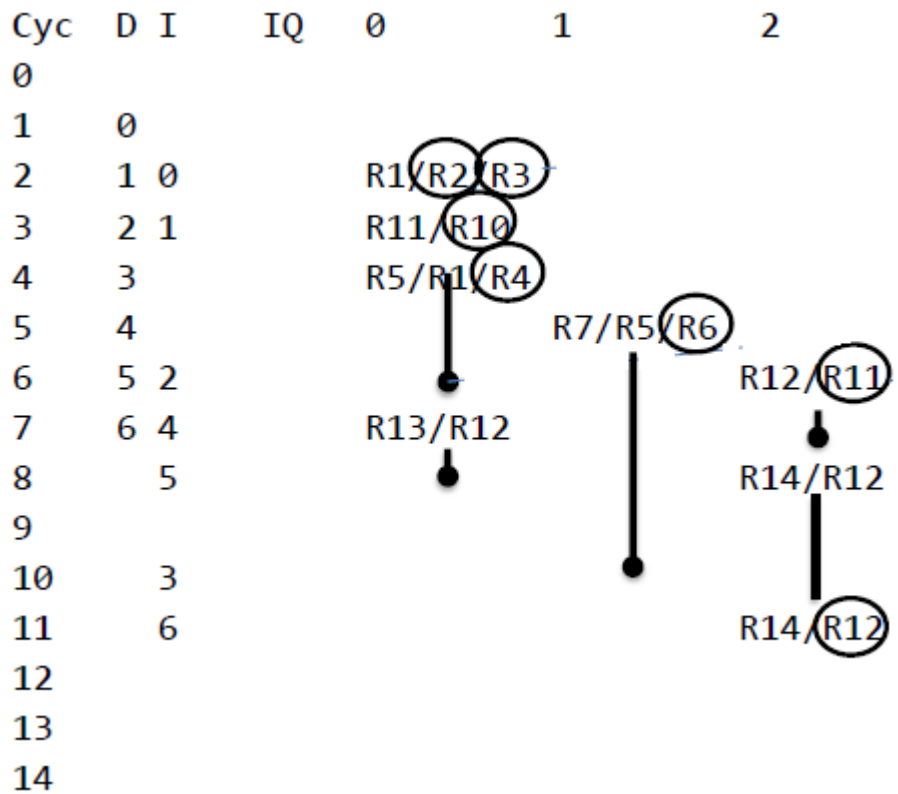
```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3    F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1        F  D  I  X0 W
2 MUL   R5, R1, R4          F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6             F  D  i                 I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                 F  D  i  I  X0 W
5 ADDIU R13,R12,1                    F  D  i  I  X0 W
6 ADDIU R14,R12,2                       F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 0 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 0 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |
| 5 | 1 | 0 | 1 | R13 | 1 | 0 | R12 | 0 | X | X |
| 6 | 2 | 0 | 1 | R14 | 1 | 0 | R12 | 0 | X | X |

```
                      0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3    F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1        F  D  I  X0 W
2 MUL   R5, R1, R4          F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6             F  D  i                 I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1                 F  D  i  I  X0 W
5 ADDIU R13,R12,1                    F  D  i  I  X0 W
6 ADDIU R14,R12,2                       F  D  i        I  X0 W
```

| OP | Imm | S | V | Dest | V | P | Src0 | V | P | Src1 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | 0 | 1 | R1 | 1 | 0 | R2 | 1 | 0 | R3 |
| 1 | 1 | 0 | 1 | R11 | 1 | 0 | R10 | 0 | X | X |
| 2 | X | 0 | 1 | R5 | 1 | 0 | R1 | 1 | 0 | R4 |
| 3 | X | 0 | 1 | R7 | 1 | 0 | R5 | 1 | 0 | R6 |
| 4 | 1 | 0 | 1 | R12 | 1 | 0 | R11 | 0 | X | X |
| 5 | 1 | 0 | 1 | R13 | 1 | 0 | R12 | 0 | X | X |
| 6 | 2 | 0 | 1 | R14 | 1 | 0 | R12 | 0 | X | X |

```
                    0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3  F  D  I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1      F  D  I  X0 W
2 MUL   R5, R1, R4        F  D  i     I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6           F  D  i              I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1               F  D  i  I  X0 W
5 ADDIU R13,R12,1                  F  D  i  I  X0 W
6 ADDIU R14,R12,2                     F  D  i        I  X0 W
```

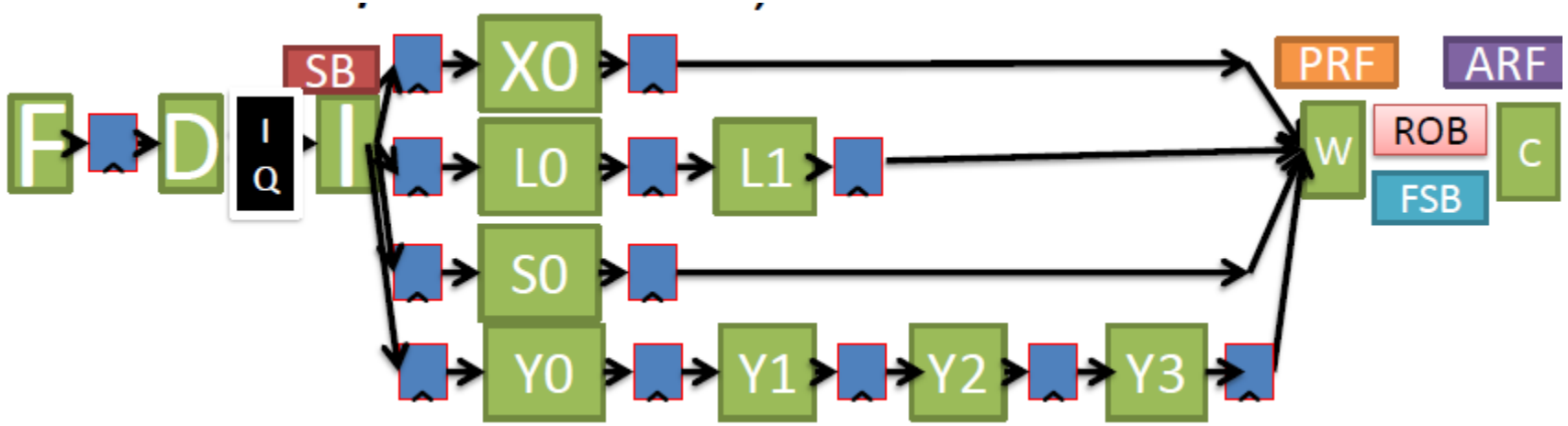


# Assuma todas instruções em IQ

```
                                0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15
0 MUL   R1, R2, R3 F  D  i              I  Y0 Y1 Y2 Y3 W
1 ADDIU R11,R10,1     F  D  i              I  X0 W
2 MUL   R5, R1, R4       F  D  i                    I  Y0 Y1 Y2 Y3 W
3 MUL   R7, R5, R6          F  D  i                          I  Y0 Y1 Y2 Y3 W
4 ADDIU R12,R11,1              F  D  i              I  X0 W
5 ADDIU R13,R12,1                 F  D  i                    I  X0 W
6 ADDIU R14,R12,2                    F  D  i                    I  X0 W
```

O desempenho melhora?

# Processador IO2I




| | | | | | |
|---|---|---|---|---|---|
| ARF | | | | | W |
| SB | | R/W | | W | |
| PRF | | R | | W | |
| ROB | R/W | | | W | R/W |
| FSB | | | | W | R/W |
| IQ | W | R/W | | | |

```
                    0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19
0 MUL   R1, R2, R3  F  D  I  Y0 Y1 Y2 Y3 W  C
1 ADDIU R11,R10,1      F  D  I  X0 W  r        C
2 MUL   R5, R1, R4        F  D  i     I  Y0 Y1 Y2 Y3 W  C
3 MUL   R7, R5, R6           F  D  i              I  Y0 Y1 Y2 Y3 W  C
4 ADDIU R12,R11,1               F  D  i  I  X0 W  r                    C
5 ADDIU R13,R12,1                  F  D  i  I  X0 W  r                    C
6 ADDIU R14,R12,2                     F  D  i        I  X0 W  r                 C
```

# E se pudermos disparar 2 ao mesmo tempo?

```
0 MUL   R1, R2, R3  F  D  I  Y0 Y1 Y2 Y3 W  C
1 ADDIU R11,R10,1      F  D  I  X0 W  r        C
2 MUL   R5, R1, R4        F  D  i     I  Y0 Y1 Y2 Y3 W  C
3 MUL   R7, R5, R6           F  D  i              I  Y0 Y1 Y2 Y3 W  C
4 ADDIU R12,R11,1               F  D  i  I  X0 W  r                    C
5 ADDIU R13,R12,1                  F  D  i  I  X0 W  r                    C
6 ADDIU R14,R12,2                     F  D  i     I  X0 W  r                 C
```

# Processador superescalar de 2 vias fora de ordem com 1 ALU

```
                    0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19
0 MUL   R1, R2, R3  F  D  I  Y0 Y1 Y2 Y3 W  C
1 ADDIU R11,R10,1   F  D  I  X0 W  r           C
2 MUL   R5, R1, R4     F  D  i        I  Y0 Y1 Y2 Y3 W  C
3 MUL   R7, R5, R6     F  D  i                  I  Y0 Y1 Y2 Y3 W  C
4 ADDIU R12,R11,1         F  D  I  X0 W  r                        C
5 ADDIU R13,R12,1         F  D  i  I  X0 W  r                        C
6 ADDIU R14,R12,2            F  D  i  I  X0 W  r                        C
```

# Agradecimento

David Wentzlaff  (Princeton University)