Realizing Circuits with Different Kinds of FFs

Choosing a Flipflop

R-S Clocked Latch:
- used as storage element in narrow width clocked systems
- its use is not recommended!
- however, fundamental building block of other flipflop types

J-K Flipflop:
- versatile building block
- can be used to implement D and T FFs
- usually requires least amount of logic to implement f(In,Q,Q+)
- but has two inputs with increased wiring complexity

- because of 1's catching, never use master/slave J-K FFs
- edge-triggered varieties exist

D Flipflop:
- minimizes wires, much preferred in VLSI technologies
- simplest design technique
- best choice for storage registers

T Flipflops:
- don't really exist, constructed from J-K FFs
- usually best choice for implementing counters

Preset and Clear inputs highly desirable!!

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Characteristic Equations:

R-S: $Q+ = S + \overline{R}\,Q$

D: $Q+ = D$

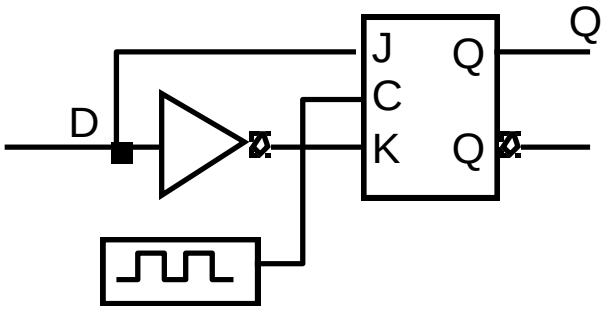
J-K: $Q+ = J\,\overline{Q} + \overline{K}\,Q$

T: $Q+ = T\,\overline{Q} + \overline{T}\,Q$

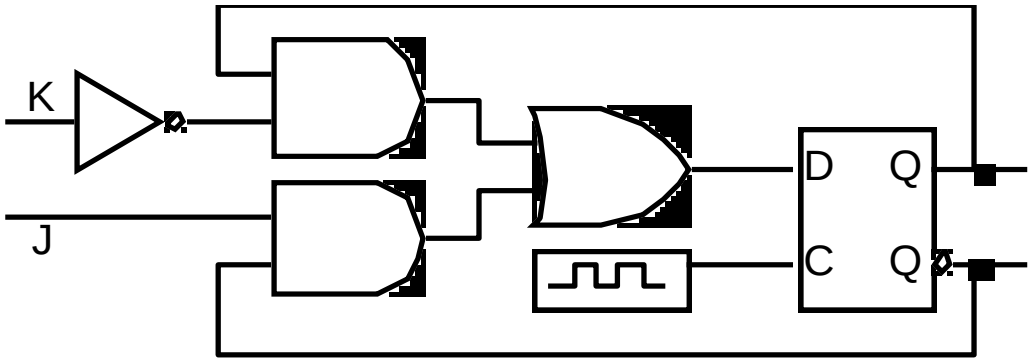
Derived from the K-maps
for $Q+ = f(\text{Inputs}, Q)$

E.g., J=K=0, then Q+ = Q
J=1, K=0, then Q+ = 1
J=0, K=1, then Q+ = 0
J=1, K=1, then Q+ = Q

Implementing One FF in Terms of Another



D implemented with J-K



J-K implemented with D

Activity

Characteristic Equations:

R-S: $Q+ = S + \overline{R}\,Q$

D: $Q+ = D$

J-K: $Q+ = J\,\overline{Q} + \overline{K}\,Q$

T: $Q+ = T\,\overline{Q} + \overline{T}\,Q$

- Excitation Tables: What are the necessary inputs to cause a particular kind of change in state?

Q	Q^+	R	S	J	K	T	D
0	0						
0	1						
1	0						
1	1						

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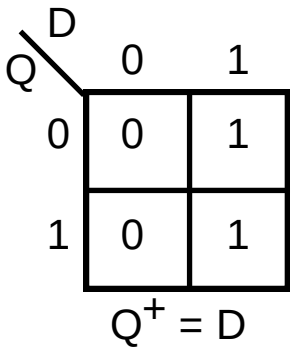
Design Procedure

Excitation Tables: What are the necessary inputs to cause a particular kind of change in state?

Q	Q^+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Implementing D FF with a J-K FF:

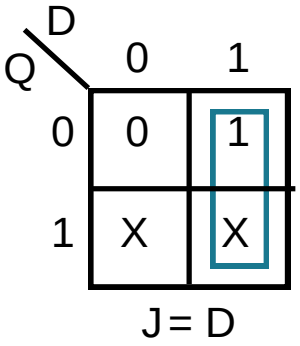
1) Start with K-map of Q+ = f(D, Q)

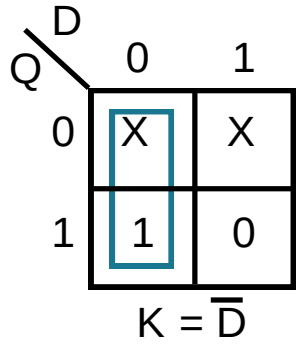


2) Create K-maps for J and K with same inputs (D, Q)

3) Fill in K-maps with appropriate values for J and K to cause the same state changes as in the original K-map

E.g., D = Q= 0, Q+ = 0
then J = 0, K = X





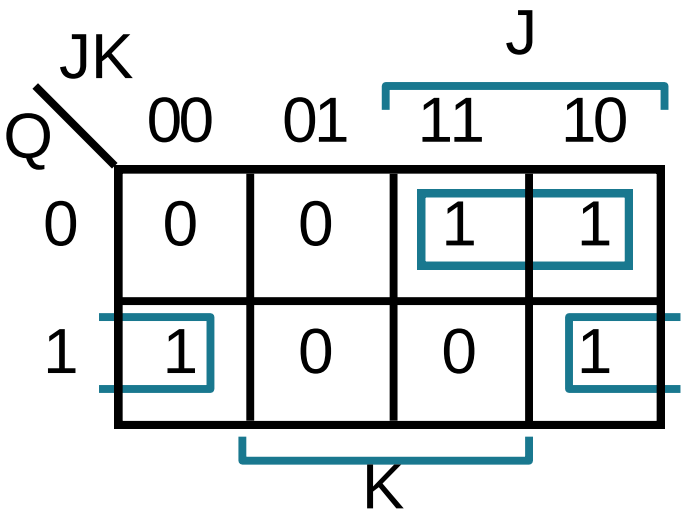
Realizing Circuits with Different Kinds of FFs

Design Procedure (Continued)

Implementing J-K FF with a D FF:

1) K-Map of Q+ = F(J, K, Q)

2,3) Revised K-map using D's excitation table
its the same! that is why design procedure with D FF is simple!



$$Q^+ = D = J\overline{Q} + \overline{K}Q$$

Resulting equation is the combinational logic input to D
to cause same behavior as J-K FF. Of course it is identical
to the characteristic equation for a J-K FF.