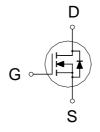
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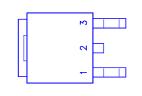
N-Channel Logic Level Enhancement Mode Field Effect Transistor

P5506BDG TO-252 Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	R _{DS(ON)}	I _D
60	55m	10A





1.GATE 2.DRAIN 3.SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST	SYMBOL	LIMITS	UNITS	
Drain-Source Voltage	V_{DS}	60	V	
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T _C = 25 °C		10	
Continuous Diain Current	T _C = 70 °C	I _D	8	Α
Pulsed Drain Current ¹	I _{DM}	32	1	
Dower Discinction	T _C = 25 °C	В	32	W
Power Dissipation	T _C = 70 °C	P _D	22	VV
Operating Junction & Storage Tem	T _j , T _{stg}	-55 to 150	°C	
Lead Temperature (1/16" from case	TL	275] [

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{ hetaJC}$		3	°C / W
Junction-to-Ambient	$R_{\scriptscriptstyle{ hetaJA}}$		75	°C/W

¹Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_c = 25 °C. Unless Otherwise Noted)

		, Offices Otherwise Noteu)		UNIT		
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	
		STATIC				
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.5	2.5	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0V$, $V_{GS} = \pm 20V$			±250	nA
		$V_{DS} = 48V, V_{GS} = 0V$			1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 40V, V_{GS} = 0V, T_{J} = 55 ^{\circ}C$			10	μΑ

²Duty cycle ≤ 1%

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On-State Drain Current ¹	I _{D(ON)}	$V_{DS} = 5V, V_{GS} = 10V$	32			Α
Drain-Source On-State		$V_{GS} = 4.5V, I_D = 8A$		59	75	
Resistance ¹	R _{DS(ON)}	$V_{GS} = 10V, I_D = 10A$		42	55	m
Forward Transconductance ¹	g fs	$V_{DS} = 10V, I_{D} = 10A$		14		S

DYNAMIC								
Input Capacitance	C _{iss}			650				
Output Capacitance	C _{oss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		80		pF		
Reverse Transfer Capacitance	C _{rss}			35				
Total Gate Charge ²	Q_g	\/ 0.5\/ \/ 10\/		12.5	18			
Gate-Source Charge ²	Q_{gs}	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V,$ $I_{D} = 4.5A$		2.4		nC		
Gate-Drain Charge ²	Q_{gd}	ID = 4.0A		2.6		iiC		
Turn-On Delay Time ²	t _{d(on)}			11	20			
Rise Time ²	t _r	$V_{DD} = 30V$		8	18			
Turn-Off Delay Time ²	t _{d(off)}	$I_D \cong 1A, V_{GS} = 10V, R_{GEN} = 6$		19	35	nS		
Fall Time ²	t _f	B , 60 - , 6EN -		6	15			
SOURCE-DRAIN	DIODE RA	ATINGS AND CHARACTERISTICS	S (T _C = 25	5 °C)				
Continuous Current	Is				1.3			
Pulsed Current ³	I _{SM}				2.6	Α		
Forward Voltage ¹	V_{SD}	$I_F = 1A$, $V_{GS} = 0V$			1	V		

¹Pulse test : Pulse Width ≤ 300 μ sec, Duty Cycle ≤ 2%.

REMARK: THE PRODUCT MARKED WITH "P5506BDG", DATE CODE or LOT

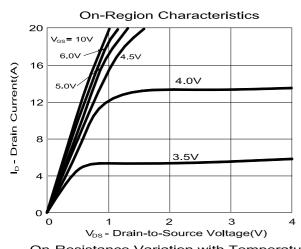
Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.

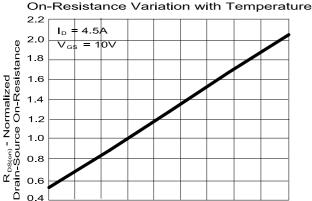
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

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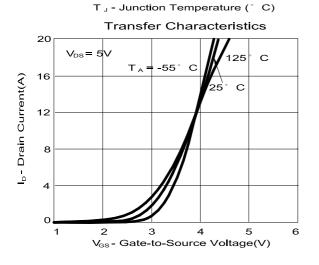
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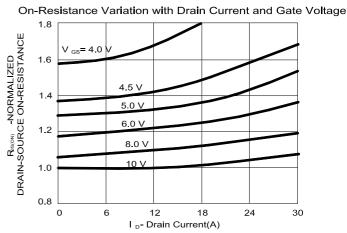


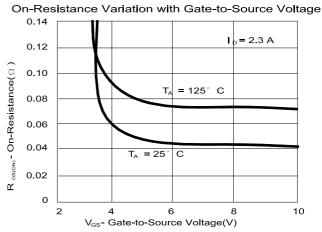


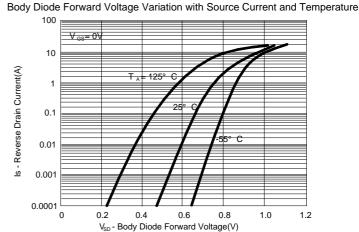
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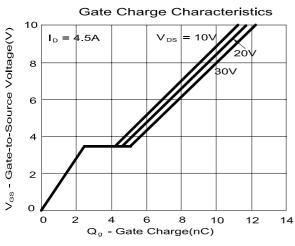


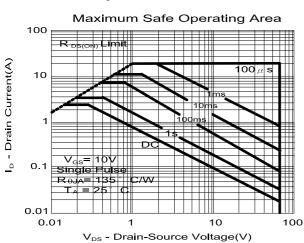


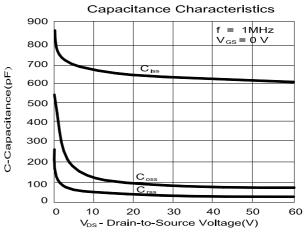


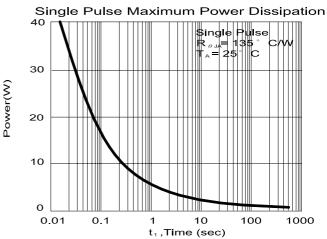
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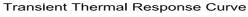
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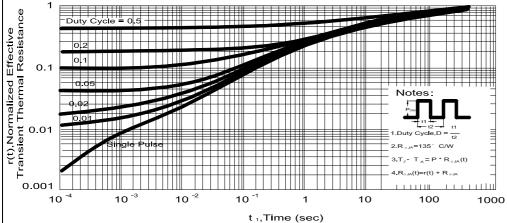












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TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimanaian	mm			
	Min.	Тур.	Max.	Dimension	Min.	Тур.	Max.	
Α	9.35		10.4	Н	0.89		2.03	
В	2.2		2.4	1	6.35		6.80	
С	0.45		0.6	J	5.2		5.5	
D	0.89		1.5	K	0.6		1	
Е	0.45		0.69	L	0.5		0.9	
F	0.03		0.23	М	3.96	4.57	5.18	
G	5.2		6.2	N				

