Homework #3 Chapter 4

Exercises: 5, 8, 9, 12, 15, 16, 18, 19, 21, 22, 24, 25, 30

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5. a) 23 bits. 21 to select the line and 2 more to select the addressable byte.
   b) 21 bits.

8. TODO

a)

Module 0	Module 1	Module 2	Module 3
0	4	8	12
1	5	9	13
2	6	10	14
3	7	11	15

b)

Module 0	Module 1	Module 2	Module 3
0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

9. 16 RAM chips are needed to provide a memory capacity of 4096 bytes.
   a) 8 bits
   b) 256 lines
   c) I'm not sure what this question is asking. I don't remember talking about decoders for memory.

12. a) $\frac{32\cancel{G} \times 64}{1\cancel{G} \times 16} = 32 \times \frac{64}{16} = 32 \times 4 = 128$ chips.
    b) $\frac{128}{4} = 32$ banks.
    c) 30 lines.
    d) $2^5 \times 2^{30} = 2^{35}$, 35 bits.
    e)

Chip Select	Address Select
00101	0010011010010000010011101001000
5 bits	30 bits

    f)

Chip Select	Address Select
0010011010010000010011101001000	00101
30 bits	5 bits

15. a) L: 0
H: $2^{20} - 1$

b) L: 0
H: $2^{19} - 1$

c) L: 0
H: $2^{18} - 1$

16. a) 256M = $2^8 \times 2^{20} = 2^{28}$ words. Each word is 2 bytes. $2^{28} \times 2 = 2^{29}$ bytes = 512M bytes.

b) If this RAM is byte addressable, you would need 29 bits for an address.

c) If this RAM is word addressable you would need 28 bits for an address.

18. e.
There are 32 (2^5) chips and 64 (2^6) locations on each chip.

19.

Fetch: Load the PC into the MAR; fetch the instruction and place it into the IR; increment PC by 1;

Decode: Store the right 12 bits into the MAR; decode the left 4 bits for the opcode.

Execute: Execute instruction

21. MARIE can 16 bits data but MARIE's memory is limited to 4096 address locations, so the MAR only needs to be 12 bits

22. 1108
3109
9106
3109
2108
7000
3108
9103
0023
0001

24. a) 1108
3109
210B
A000
6000
2109
7000
00FC
000E
0108
0000

b)

symbol	location
A	108
B	109
C	10A
D	10B
Start	100

c) 0108

25. a) 1209
320A
420B
220C
8800
9208
C20C
A000
7000
0200
0009
0001
0000

b)

symbol	location
Addr	20C
Base	209
Begin	200
Done	208
Loop	202
Offs	20A
One	20B

c) 208

30.

```
        ORG     100
If,     Load    X
        Subt    Y
        Skipcond 800
        Jump    LessEq
Else,   Load    X
        Subt    Z
        Skipcond 400
        Jump    Elif
        Load    Z
        Add     One
        Store   Z
        Jump    Fin
LessEq, Load    Y
        Add     One
        Store   Y
        Jump    Fin
Elif,   Load    Y
        Subt    One
        Store   Y
Fin,    Halt
-------------------------
X,      Dec     VAL
Y,      Dec     VAL
Z,      Dec     VAL
1One,   Dec     1
```