注意：斜体的页码表示数字，表格和文本框; 以“e”开头的页码是指在线资料。

0, 8, 22. See also LOW, FALSE 另见LOW、FALSE

1, 8, 22. See also HIGH, TRUE 另见HIGH、TRUE  
32-bit datapath, 386: 32位数据通道  
32-bit instructions, 329: 32位指令  
64-bit architecture, 360: 64位架构  
74xx series logic, 533.e1–533.e5: 74xx系列逻辑电路  
 parts,器件  
 2:1 mux (74157), 533.e4：2:1多路选择器  
 3:8 decoder (74138), 533.e4：3:8解码器  
 4:1 mux (74153), 533.e4：4:1多路选择器  
 AND (7408), 533.e3：与门  
 AND3 (7411), 533.e3：3输入与门  
 AND4 (7421), 533.e3：4输入与门  
 counter (74161, 74163), 533.e4: 计数器  
 FLOP (7474), 533.e1, 533.e3：触发器  
 NAND (7400), 533.e3: 与非门  
 NOR (7402), 533.e3: 或非门  
 NOT (7404), 533.e1: 非门  
 OR (7432), 533.e3: 或门  
 register (74377), 533.e4: 寄存器  
 tristate buffer (74244), 533.e4: 三态缓冲器  
 XOR (7486), 533.e3: 异或门  
#define, 541.e5–541.e6   
#include, 541.e6–541.e7. See also Standard libraries另见标准库

A

ABI. See Application Binary Interface (ABI)：ABI. 请参阅应用程序二进制接口（ABI）  
Abstraction, 4–5:抽象  
 digital. See Digital abstraction数字，另见数字抽象  
Accumulator, 367: 累加器  
Acorn Computer Group, 296, 472：橡果计算机组  
Acorn RISC Machine, 350：橡果RISC机器  
Active low, 74–75低电平有效  
A/D conversion, 531.e31–531.e32: 模拟数字转换  
Ad hoc testing, 452：Ad hoc测试  
ADCs. See Analog/digital converters(ADCs)：ADCs。另见模拟/数字转换器（ADCs）  
ADD, 297，536  
Adders, 239 –246：加法器  
 carry propagate, 240:进位传播  
 carry-lookahead, 241:先行进位  
 full, 56, 240全  
 half, 240半  
 HDL for, 184, 200, 450:硬件描述语言  
 prefix, 243:前缀  
 ripple-carry, 240:行波进位  
Addition, 14 –15, 17 –18, 235, 239 –246, 297. See also Adders加法，另见加法器  
 binary, 14–15:二进制  
 floating point, 259:浮点数

signed binary, 15–17:带符号二进制数  
Address. See also Memory地址，另见存储器  
 physical, 509–513 :物理  
 translation, 509–512 :转换  
 virtual, 508. See also Virtual memory :虚拟，另见虚拟内存  
Addressing modes, ARM, 336:寻址方式，ARM  
 base, 336:基址  
 immediate, 336 :立即数  
 PC-relative, 336:相对PC

register, 336：寄存器

Advanced High-performance Bus：先进的高性能总线  
 (AHB), 531.e54  
Advanced Micro Devices：(公司名称)  
 (AMD), 296

Advanced microarchitecture, 456–470:先进微结构

branch prediction. See Branch prediction:分支预测

deep pipelines. See Deep pipelines :深度流水线

heterogeneous multiprocessors. See Heterogeneous multiprocessors:异构多处理器

homogeneous multiprocessors.See Homogeneous multiprocessors:同构型多处理器

micro-operations. See Microoperations：微操作

multiprocessors. See Multiprocessors：多处理器

multithreading. See Multithreading :多线程

out-of-order processor. See Out-of-order processor:异步处理器

register renaming. See Register renaming:寄存器重命名

single instruction multiple data. See Single Instruction Multiple Data(SIMD):单指令多数据流

superscalar processor. See Superscalar processor:超标量处理器

Advanced Microcontroller Bus Architecture (AMBA), 531.e54：先进的微控制器总线架构

Advanced RISC Machines, 472先进RISC机器

AHB. See Advanced High-performance Bus (AHB)：另见先进的高性能总线

AHB-Lite bus, 531.e54–531.e55

Altera FPGA, 274–279:Altera现场可编程逻辑门阵列

ALU. See Arithmetic/logical unit (ALU):算术逻辑单元

ALU Decoder, 398–400:ALU译码器

ALUControl, 248–250, 392, 395

ALUOp, 398

ALUResult, 392–397

ALUSrc, 396

AMAT. See Average memory access time平均内存访问时间

AMBA. See Advanced Microcontroller Bus Architecture (AMBA) 先进的微控制器总线架构

AMD. See Advanced Micro Devices

AMD64, 368

Amdahl, Gene, 492

Amdahl’s Law, 492 Amdahl定律

American Standard Code for Information Interchange (ASCII), 315–316, 541.e8, 541.e27–541.e28美国信息交换标准码

Analog I/O, 531.e25–531.e32模拟I/O

A/D conversion, 531.e31–531.e32模/数转换

D/A conversion, 531.e25–531.e28数/模转换

Pulse-width modulation (PWM), 531.e28–531.e31 脉冲宽度调制

Analog-to-digital converters (ADCs), 531.e25, 531.e27, 531.e31–531.e32模拟数字转换器Analytical engine, 7, 8分析机

AND gate, 20 –22, 179与门

chips (7408, 7411, 7421), 533.e3 芯片

truth table, 20, 22真值表

using CMOS transistors, 32–33使用CMOS晶体管

AND, 303–304

AND-OR (AO) gate, 46与或门

Anode, 27阳极

Antidependence, 464 反相关

Application Binary Interface (ABI), 320 应用程序二进制接口

Application-specific integrated circuits(ASICs), 533.e9 专用集成电路

Architectural state, 338, 364体系机构状态

for ARM, 385–386 对于ARM

Architecture, 295 体系结构

assembly language, 296 汇编语言

instructions, 297–298 指令

operands, 298–303 操作数

compiling, assembling, and loading, 339 编译，组装和加载

assembling, 342–343 组装

compilation, 340–341 编译

linking, 343–344 链接

loading, 344–345 加载

memory map, 339–340 存储器映射

evolution of ARM architecture, 350 ARM体系结构的演变

64-bit architecture, 360 64位体系结构

digital signal processors (DSPs), 352–356 数字信号处理器

floating-point instructions, 357–358 浮点指令

power-saving and security instructions, 358 节电和安全指令

SIMD instructions, 358–360 SIMD指令

Thumb instruction set, 351–352 Thumb 指令集

machine language, 329 机器语言

addressing modes, 336 寻址方式

branch instructions, 334–335 分支指令

data-processing instructions, 329–333 数据处理指令

interpreting, 336–337 解读

memory instructions, 333–334 存储器指令

stored program, 337–338 存储程序

odds and ends, 345 什物

exceptions, 347–350 异常

loading literals, 345–346 加载文字

NOP, 346

programming, 303 程序设计

branching, 308–309 分支

conditional statements, 309–312 条件语句

condition flags, 306–308 条件标志

function calls, 317–329 函数调用

getting loopy, 312–313 变成循环

logical and arithmetic instructions, 303–306 逻辑和算术指令

memory, 313–317 存储器

x86 architecture, 360 x86体系结构

big picture, 368 主要部分

instruction encoding, 364–367 指令编码

instructions, 364 指令

operands, 362–363 操作数

peculiarities, 367–368 特性

registers, 362 寄存器

status flags, 363–364 状态标志

Arguments, 317–319, 541.e15 参数

pass by reference, 541.e22按引用传递

pass by value, 541.e22按值传递

Arithmetic算术

ARM instructions, 303–306 ARM指令

circuits, 239–255 电路

C operators,541.e11–541.e13 C运算符

HDL operators, 185 HDL运算符

Arithmetic/logical unit (ALU), 248–251, 392算术逻辑单元

implementation of, 249 实现

in processor, 392–430 在处理器中

ARM architecture, evolution of, 296, 350 ARM架构，演变

64-bit architecture, 360 64位体系结构

digital signal processing (DSP) instructions, 352–356 数字信号处理（DSP）指令

floating-point instructions, 357–358 浮点指令

power-saving and security instructions, 358 节电和安全指令

SIMD instructions, 358–360 SIMD指令

Thumb instruction set, 351–352 Thumb 指令集

ARM instructions, 295–369, 535–540 ARM指令

branch instructions, 308–309, 539 分支指令

condition flags, 306–308, 540 条件标志

data-processing instructions, 303–306, 535–537 数据处理指令

logical instructions, 303–304 逻辑指令

multiply instructions, 305–306, 537 乘法指令

shift instructions, 304–305 移位指令

formats 格式

addressing modes, 336 寻址方式

branch instructions, 334 分支指令

data-processing instructions, 329–333 数据处理指令

interpreting, 336–337 解读

memory instructions, 333–335 存储器指令

stored program, 337–338 存储程序

instruction set, 295 指令集

memory instructions, 301–303, 313–317, 538 存储器指令

miscellaneous instructions, 345–346, 539 其它控制类指令

ARM Microcontroller Development Kit (MDK-ARM), 297 ARM微控制器开发套件

ARM microprocessor, 385 ARM微处理器

data memory, 385–388 数据内存

instruction memory, 385–388 指令内存

multicycle, 406–425 多周期

pipelined, 425–433 流水线

program counter, 385–388 程序计数器

register file, 385–388 寄存器文件

single-cycle, 390–406, 443–456 单周期

state elements of, 385–388 状态元素

ARM processors, 470 ARM处理器

ARM registers, 299–300 ARM寄存器

program counter, 308, 338, 386–387 程序计数器

register file, 386–387 寄存器文件

register set, 299–300 寄存器组

ARM single-cycle HDL, 443–456 ARM单周期HDL

building blocks, 449–452 构建块

controller, 443 控制器

datapath, 443 数据路径

testbench, 452–456 测试平台

ARM7, 472, 473

ARM9, 474

ARM9E, 472

ARMv3 architecture, 472 ARMv3架构

ARMv4 instruction set, 295, 539 ARMv4指令集

ARMv7 instruction, 472 ARMv7指令

Arrays, 313–317, 541.e23–541.e29 数组

accessing, 313–317, 541.e23 访问

bytes and characters, 315–317, 541.e27–541.e29字节和字符

comparison or assignment of, 541.e28比较或赋值

declaration, 314–317, 541.e23声明

indexing, 314–317, 541.e23–541.e27索引

initialization, 541.e23–541.e24初始化

as input argument, 541.e24–541.e25作为输入参数

multi-dimension, 541.e26–541.e27 多维度

ASCII. See American Standard Code for Information Interchange美国信息交换标准码

ASICs. See Application-specific integrated circuits专用集成电路

ASR, 304

Assembler, 339, 541.e44 汇编器

Assembling, 342–343 组装

Assembly language, ARM, 295–350, 535–540 汇编语言，ARM

instructions, 297–350, 535–540: 指令

operands, 297–303: 操作数

translating high-level code to, 339–345 :转换高级语言代码为

translating machine language to, 337: 转换机器语言为

Assembly language, x86. See x86 汇编语言，另见x86

Associativity结合律

in Boolean algebra, 62, 63 在布尔代数

in caches, 493, 498–500 在缓存中

Astable circuits, 119: 非稳态电路

Asymmetric multiprocessors. See Heterogeneous multiprocessors: 非对称多处理器，另见异构多处理器

Asynchronous circuits, 120 –123:异步电路

Asynchronous resettable flip-flopsdefinition, 116:异步复位触发器定义

HDL, 194–196

Asynchronous serial link, 531.e17, 531.e17.. See also Universal Asynchronous Receiver Transmitter (UART) : 异步串联，另见通用异步收发器

AT Attachment (ATA), 531.e61–531.e62: AT附件

Average memory access time (AMAT), 491, 504:平均内存访问时间

B

B, 308–309, 334–336, 396–397

Babbage, Charles, 7

Banked registers, 348–349 分组寄存器

Base addressing, 336:基址寻址

Baud rate, 531.e17–531.e19:波特率

BCD. See Binary coded decimal: 二进制编码的十进制数

BCM2835, 531.e3, 531.e4–531.e5, 531.e8, 531.e9, 531.e19

timer, 531.e23 计时器

Behavioral modeling, 173–174 :行为建模

Benchmarks, 389:基准测试程序

BEQ, 309

Biased exponent, 257:偏置阶码

BIC (bit clear), 303–304 位清除

big.LITTLE, 469

Big-endian memory, 303:大端存储器

Big-endian order, 178 :大端顺序

Binary addition, 14 –15. See also Adders,Addition :二进制加法，另见加法器、加法

Binary coded decimal (BCD), 258:二进制编码的十进制数

Binary encoding, 125–126, 129–131:二进制编码

for divide-by-3 counter, 129–131:除以3计数器

for traffic light FSM, 125–126 :交通灯有限状态机

Binary numbers:二进数

signed, 15 –19:有符号

unsigned, 9 –11:无符号

Binary to decimal conversion, 10, 10 –11:二-十进制转换

Binary to hexadecimal conversion, 12:二-十六进制转换

Bipolar junction transistors, 26:双极性晶体管

Bipolar motor drive, 531.e50:双极电机驱动

Bipolar signaling, 531.e18:双极性信号

Bipolar stepper motor, 531.e51, 531.e52–531.e53:双极步进电机

AIRPAX LB82773-M1, 531.e51, 531.e51

direct drive current, 531.e52:直流驱动电流

Bistable element, 109:双稳态元件

Bit, 8:比特位

dirty, 506脏

least significant, 13, 14:最低有效

most significant, 13, 14:最高有效

sign, 16:有符号

use, 502:使用

valid, 484:有效

Bit cells, 264 –269:位元

DRAM, 266–267:动态随机存储器;

ROM, 268–270:只读存储器

SRAM, 267:静态随机存储器

Bit swizzling, 188:位交叉混合

Bitline, 264:位线

Bitwise operators, 177 –179:位运算符

Block, 493:块

Block offset, 500–501 :块偏移

Block size (b), 493, 500–501:块大小

Blocking and nonblocking assignments, 199 –200, 205–209:阻塞和非阻塞赋值

BLT. See Branch if less than (BLT) BLT。另见如果小于则分支（BLT）

BlueSMiRF silver module, 531.e42–531.e43, 531.e42 BlueSMiRF silver模块

Bluetooth wireless communication, 531.e42–531.e43蓝牙无线通信

BlueSMiRF silver module, 531.e42–531.e43 BlueSMiRF silver模块

classes, 531.e42:类别

BNE, 310

Boole, George, 8

Boolean algebra, 60 –66:布尔代数

axioms, 61:公理

equation simplification, 65 –66:等式简化

theorems, 61–64:定理

Boolean equations, 58 –60:布尔等式

product-of-sums form, 60:或与式

sum-of-products form, 58 –60:与或式

Boolean logic, 8. See also Boolean algebra, Logic gates:布尔逻辑，另见布尔代数、逻辑门

Boolean theorems, 61–64:布尔定理

associativity, 63:结合律

combining, 62:合并律

commutativity, 63 交换律

complements, 62 :互补定理

consensus, 62, 64:一致律

covering, 62:吸收律

De Morgan’s, 63 –64:德∙摩根定理

distributivity, 63:分布律

idempotency, 62:重叠定理

identity, 62:同一性定理

involution, 62:回旋定理

null element, 62:零元定理

Branch if less than (BLT), 334–335 小于则分支（BLT）

Branch instructions, 308–309 分支指令

ARM instructions, 539, 539 ARM指令

Branch misprediction penalty, 438, 459:分支预测错误惩罚

Branch prediction, 459–461:分支预测

Branch target address (BTA), 334–335:分支目标地址

Branch target buffer, 459:分支目标缓冲

Branching 308–309, 334–336 分支

conditional, 309:有条件

unconditional, 309:无条件

Breadboards, 533.e18–533.e19:电路试验板

BTA. See Branch target address(BTA):分支目标地址

Bubble, 20, 63 气泡

pushing, 63–64, 71 –73推

Buffers, 20 :缓冲

lack of, 117 :缺少

tristate, 74–75 :三态门

Bugs, 175: 程序错误

in C code, 541.e45–541.e49 :C代码

Bus, 56:总线

tristate, 75:三态

Bus interfaces, 531.e54–531.e57 总线接口

AHB-Lite, 531.e54–531.e55

memory and peripheral interface example, 531.e55–531.e57 存储器和外设接口示例

Bypassing, 432. See also Forwarding :绕过

Byte, 13 –14, 315–317. See also Character:字节，另见字符

least significant, 13 –14 :最低有效

most significant, 13 –14 :最高有效

Byte offset, 495 字节偏移

Byte-addressable memory, 301 –302:字节寻址存储器

big-endian, 302 –303 :大端

little-endian, 303 :小端

C

C programming, 623 –671 :C语言编程

common mistakes. See Common mistakes :常见错误

compiler. See Compiler, i\_Hlt414277118n C 编译器

conditional statements. See Conditional statements:条件语句

control-flow statements. See Control-flow statements:控制流语句

data types. See Data types:数据类型

function calls. See Function calls:函数调用

loops. See Loops:循环

operators. See Operators:操作符

running, 626:运行

simple program, 541.e3–541.e4:简单程序

standard libraries. See Standard libraries:标准库

variables. See Variables in C:变量

Caches, 489–508 :缓存

address fields, :地址域

block offset, 500–501:块偏移

byte offset, 495:字节偏移

set bits, 495:设置位

tag, 495:标签

advanced design, 503–507:先进设计

evolution of, in ARM, 507:演化，MIPS内

multiple level, 504:多层次

organizations, 502:组织方式

direct mapped, 494–498:直接映射

fully associative, 499–500:全关联

multi-way set associative, 498–499:多路组关联

parameters:参数

block, 493:块

block size, 493, 500–501 :块大小

capacity (C), 492–493:容量

degree of associativity (N), 499:关联度

number of sets (S), 493:集数目

performance of :性能

hit, 490–492:命中

hit rate, 491–492:命中率

miss, 480–492, 505:缺失

capacity, 505:容量

compulsory, 505:强制

conflict, 498, 505:冲突

penalty, 500:惩罚

miss rate, 491–492:缺失率

reducing, 505–506:降低

miss rate vs. cache parameters, 505–506 :缺失率与缓存参数

replacement policy, 502–503: 替换原则

status bits:状态位

dirty bit (D), 506：脏位

use bit (U), 502:使用位

valid bit (V), 496:有效位

write policy, 506–507 :写入策略

write-back, 506–507：回写

write-through, 506–507 ：透写

CAD. See Computer-aided design(CAD):计算机辅助设计

Callee, 317 被调用函数

Callee save rule, 324 被调用函数保存规则

Callee-saved registers, 323 被调用函数保存的寄存器

Caller save rule, 324 调用函数保存规则

Caller-saved registers, 329:调用函数保存的寄存器

Canonical form. See Sum-of-products(SOP) form, Product-of-sums(POS) form: 范式。另见与或式(SOP)、或与式(POS)

Capacitors, 28:电容

Capacity, of cache, 492–493:缓存容量

Capacity miss, 505:容量缺失

Carry propagate adder (CPA).See Carry-lookahead adder (CLA); Prefix adders; Ripple-carry adder:进位传播加法器，另见先行进位加法器、前缀加法器、行波进位加法器

Carry-lookahead adder (CLA), 241 –243, 242 :先行进位加法器

Case statement, in HDL, 201–203.See also Switch/case statement: case语句，另见switch/case语句

Casez, case?, in HDL, 205 casez、case?语句

Cathode, 27:阴极

Cathode ray tube (CRT), 531.e36. See also VGA(Video Graphics Array) monitor:阴极射线管，另见VGA（视频图形阵列）显示器

horizontal blanking interval, 531.e36:水平消隐间隔

vertical blanking interval, 531.e36:垂直消隐间隔

Character LCDs, 531.e33–531.e36字符LCD

Characters (char), 315–317, 541.e8, 541.e27 :字符

arrays. See also Strings数组，另见字符串

C type, 541.e27:C类型

Chips, 28 :芯片

multiprocessors, 468:多处理器

Chopper constant current drive, 531.e51：斩波恒流驱动

Circuits;电路

74xx series. See 74xx series logic：74xx系列，另见74xx系列逻辑电路

application-specific integrated(ASICs), 533.e9:专用集成电路

astable, 119:非稳态

asynchronous, 120, 122 –123:异步

combinational. See Combinational logic:组合，另见组合逻辑

definition of, 55 :定义

delay, 88 –92 :延迟

glitches in, 92–95 小故障

multiple-output, 68:多路输出

priority, 68 :优先级

sequential. See Sequential logic:时序，另见时序电路

synchronous, 122 –123:同步

synchronous sequential, 120 –123：同步时序电路

synthesized, 176, 179, 181：综合

timing, 88 –95, 141–151:时序

CISC. See Complex Instruction Set Computer(CISC) architectures:复杂指令集计算机（CISC）体系结构

CLBs. See Configurable logic blocks(CLBs):可配置逻辑块

Clock cycles per instruction (CPI), 390:每条指令的时钟周期

Clock period, 142, 390:时钟周期

Clock skew, 148 –151:时钟偏斜

Clustered multiprocessing, 470:集群多处理

cmd field, 330, 535, 537 cmd域

CMOS. See Complementary Metal-Oxide-Semiconductor Logic(CMOS): CMOS。另见互补金属氧化物半导体逻辑（CMOS）

CMP, 402

Combinational composition, 56 :组合电路构建

Combinational logic, 174 :组合逻辑

design, 55 –106 :设计

Boolean algebra, 60 –66:布尔代数

Boolean equations, 58 –60:布尔等式[解答：统一为此翻译]

building blocks, 83 –88, 239–255:构造部件

delays, 88 –92 :延时

don’t cares, 81 –82无关项

Karnaugh maps (K-maps), 75 –83:卡诺图

multilevel, 66 –73：多层

precedence, 58：优先级

timing, 88 –95：时序

two-level, 69：两层

X(contention). See Contention(X)：X(竞争)

X (don’t cares). See Don’t cares (X)：X(无关项)

Z(floating). See Floating (Z)：Z(悬空)

HDLs. See Hardware description languages(HDLs)：硬件描述语言

Combining theorem, 62:合并律

Command line arguments, 541.e44–541.e45:命令行参数

Comments注释

in ARM assembly, 297在ARM汇编语言

in C, 297–298, 541.e5 : C语言

in SystemVerilog, 180在SystemVerilog语言

in VHDL, 180在VHDL语言

Common mistakes in C, 541.e45–541.e49 :C语言常见错误

Comparators, 246 –248:比较器

Comparison比较

in hardware. See Comparators;Arithmetic/logical unit (ALU) 在硬件，另见比较器；算术逻辑单元ALU

processor performance, 424–425 处理器性能

using ALU, 250使用ALU

Compilation, in C, 339–345, 541.e4–541.e5, 541.e43–541.e44: C语言编译

Complementary Metal-Oxide-Semiconductor Logic (CMOS), 26 –34：互补金属氧化物半导体逻辑（CMOS）

Complements theorem, 62:互补定理

Complex instruction set computer (CISC)architectures, 298, 361, 458:复杂指令集计算机（CISC）体系结构

Complexity management, 4 –7:复杂度管理

digital abstraction, 4 –5:数字抽象

discipline, 5 –6:约束

hierarchy, 6–7:层次化

modularity, 6–7:模块化

regularity, 6–7:规整化

Compulsory miss, 505:强制缺失

Computer-aided design (CAD), 71, 129:计算机辅助设计

Concurrent signal assignment statement, 179, 183–184, 193, 200–206:并行信号赋值语句

cond field, 306–307, 330, 535 cond域

Condition flags, 306–308 条件标志

ARM instructions, 540, 540 ARM指令

Condition mnemonics, 307 条件助记符

Conditional assignment, 181 –182:条件赋值

Conditional branches, 308–309:条件分支

Conditional Logic, 398–400, 413–415 条件逻辑

Conditional operator, 181–182:条件运算符

Conditional signal assignments,181–182:条件信号赋值

Conditional statement, 309s条件语句

in ARM assembly 在MIPS汇编中

if, 309–310

if/else, 310–311

switch/case, 311–312

in C, 541.e17–541.e18:在C语言中

if, 541.e17–541.e18

if/else, 541.e17

switch/case, 541.e17–541.e18

in HDL, 194, 201 –205在HDL中

case, 201 –203

casez, case?, 205

if, if/else, 202 –205

Configurable logic blocks (CLBs), 275, 533.e7. . See also Logic elements(LEs):可配置逻辑块，另见逻辑元素

Conflict miss, 505:冲突缺失

Consensus theorem, 62, 64:一致律

Constants常数

in ARM assembly, 300–301. See also Immediates在ARM汇编中，另见立即数

in C, 541.e5–541.e6:在C中

Contamination delay, 88 –92. See also Short path :最小延迟，另见最短路径

Contention (X), 73–74 竞争

Context switching, 467:上下文切换

Continuous assignment statements, 179, 193, 200, 206 :连续赋值语句

Control hazards, 432, 437–440 :控制冲突

Control signals, 91, 249:控制信号

Control unit, 386. See also ALU decoder, Main decoder, :控制单元，另见ALU译码器，主解码器

of multicycle ARM processor, 413–423:多周期ARM 处理器

of pipelined ARM processor, 430 :流水线ARM 处理器

of single-cycle ARM processor, 397–401:单周期ARM 处理器

Control-flow statements:控制流语句

conditional statements. See Conditional statements:条件语句

loops. See Loops:循环

CoreMark, 389 CoreMark测试

Cortex-A7 and -A15, 475 Cortex-A7 和-A15, 475

Cortex-A9, 475

Counters, 260–261 计数器

divide-by-3, 130 除以3

Covering theorem, 62 吸收律

CPA. See Carry propagate adder (CPA) CPA。另见进位传播加法器

CPI. See Clock cycles per instruction, Cycles per instruction:每条指令的时钟周期

Critical path, 89–92, 402:最长路径

Cross-coupled inverters, 109, 110:交叉耦合反相器

bistable operation of, 110:双稳态运作

CRT. See Cathode ray tube(CRT):阴极射线管

Current Program Status Register (CPSR), 306, 324, 347 当前程序状态寄存器

Cycle time. See Clock period:周期时间，另见时钟周期

Cycles per instruction (CPI), 390, 424:每条指令的时钟周期

Cyclic paths, 120:回路

Cyclone IV FPGA, 275 –279：Cyclone IV现场可编程逻辑门阵列

D

D flip-flops. See flip-flops: D 触发器

D latch. See La\_Hlt414277505tches : D锁存器

D/A conversion, 531.e25–531.e28 :D / A转换

DACs. See Digital-to-analog converters(DACs):数字模拟转换器

DAQs. See Data Acquisition Systems(DAQs) 数据采集系统

Data Acquisition Systems (DAQs), 531.e62–531.e63:数据采集系统

myDAQ, 531.e62–531.e63

Data hazards, 432–436:数据冲突

HDL for, 455 硬件描述语言

Data memory, 387–388:数据存储

Data segment, 340:数据段

Data sheets, 533.e9–533.e14:数据手册

Data types, 541.e21–541.e35:数据类型

arrays. See Arrays：数组

characters. See Character (char) ：字符

dynamic memory allocation. See Dynamic memory allocation (malloc and free)：动态内存分配

linked list. See Linked list：链表

pointers. See Pointers:指针

strings. See Strings :字符串

structures. See Structures (struct) :结构

typedef, 541.e31–541.e32：typedef

Datapath:数据通路

multicycle ARM processor, 406–413:多周期ARM 处理器

B instruction, 412–413 B指令

LDR instruction, 407–410 LDR指令

STR instruction, 411–412 STR指令

pipelined ARM processor, 428–430:流水线ARM 处理器

single-cycle ARM processor, 390 :单周期ARM 处理器

B instruction, 396–397 B指令

LDR instruction, 391–394 LDR指令

STR instruction, 394–396 STR指令

Data-processing instructions, 536 数据处理指令

ARM instructions, 329–333, 396–397, 535–537 ARM指令

encodings, 536 编码

DC motors, 531.e43, 531.e44–531.e48 :直流电机

H-bridge, 531.e44, 531.e45 :H桥

shaft encoder, 531.e43–531.e44:轴角编码器

DC transfer characteristics, 24–26. See also Direct current (DC) transfer characteristics, Noise margins :直流传输特性 另见直流（DC）传输特性，噪音容限

DDR. See Double-data rate memory:DDR，另见双倍数据速率内存

De Morgan, Augustus, 63 德·摩根，奥古斯都

De Morgan’s theorem, 63–64:德·摩根定理

DE-9 cable, 531.e19 DE-9缓存

Decimal numbers, 9:十进制数

Decimal to binary conversion, 11:十进制-二进制转换

Decimal to hexadecimal conversion, 13:十进制-十六进制转换

Decode stage, 425:解码阶段

Decoders :解码器

definition of, 86–87 :定义

HDL for :硬件描述语言

behavioral, 202–203 :行为

parameterized, 219 :参数化

logic using, 87 –88 :逻辑使用

Seven-segment. See Seven-segment display decoder:七段显示译码器

Deep pipelines, 457 :深度流水线

Delaymicros function, 531.e24: Delaymicros函数

Delays, logic gates. See Propagation delay 延时

in HDL (simulation only), 188–189 在HDL中

DeleteUser function, 541.e33：DeleteUser函数

Dennard, Robert, 266

Destination register (rd or rt),393, 409 目的地寄存器

Device driver, 531.e3, 531.e6–531.e8设备驱动程序

Device under test (DUT), 220测试设备

Dhrystone, 389 测试程序

Dice, 28切块

Dielectric, 28电介质

Digital abstraction, 4 –5, 7 –9, 22 –26数字抽象

Digital circuits. See Logic数字电路

Digital signal processor (DSP), 352–356, 469 数字信号处理

Digital system implementation, 533.e1–533.e35数字系统实现

74xx series logic. See 74xx series logic :74xx系列逻辑电路

application-specific integrated circuits (ASICs), 533.e9专用集成电路

assembly of, 533.e17–533.e20 汇编语言

breadboards, 533.e18–533.e19电路试验板

data sheets,533.e18–533.e19数据手册

economics, 533.e33–533.e35经济学

logic families, 533.e15–533.e17逻辑电路系列

packaging, 533.e17–533.e20封装

printed circuit boards, 533.e19–533.e20印刷电路板

programmable logic, 533.e2–533.e9可编程逻辑

Digital-to-analog converters (DACs), 531.e25–531.e28数字模拟转换器

DIMM. See Dual inline memory module(DIMM)双列直插内存模块

Diodes, 27–28二极管

p-n junction, 28 p-n接面

DIPs. See Dual-inline packages (DIPs) 双列直插式封装

Direct current (DC) transfer characteristics, 24, 25直流电(DC)传输特性

Direct mapped cache, 494–498, 495直接映射缓存

Direct voltage drive, 531.e51直流电压驱动

Dirty bit (D), 506重写标志位

Discipline 约束

dynamic, 142–151. See also Timing analysis：动态，另见时序分析

static, 142 –151. See also Noise margins：静态，另见噪声容限

Discrete-valued variables, 7 离散数值变量

Distributivity theorem, 63分配律

Divide-by-3 counter 除以3计数器

design of, 129–131: 设计

HDL for, 210–211：HDL

Divider, 254–255 除法器

Division 除法

circuits, 253–254 电路

Do/while loops, in C, 541.e19–541.e20 :do/while 循环

Don’t care (X), 69, 81–83, 205: 无关项

Dopant atoms, 27掺杂原子

Double, C type, 541.e19–541.e20：浮点数

Double-data rate memory (DDR), 268, 531.e60–531.e61双数据速率内存

Double-precision formats, 258双精度格式

DRAM. See Dynamic random access memory (DRAM) 动态随机存储器

DSPs. See Digital signal processors(DSPs) 数字信号处理器

Dual inline memory module (DIMM), 531.e60双列直插内存模块

Dual-inline packages (DIPs), 28, 533.e1, 533.e17双列直插式封装

Dynamic branch predictors, 459动态分支预测

Dynamic data segment, 340动态数据段

Dynamic discipline, 142–151. See also Timing analysis动态约束，另见时序分析

Dynamic memory allocation (malloc, free) , 541.e32–541.e33动态内存分配

in ARM memory map, 340：在ARM 内存映射中

Dynamic power, 34动态功耗

Dynamic random access memory (DRAM), 266–267, 487–490, 519, 531.e58, 531.e60, 531.e61动态随机存储器

E

EasyPIO, 531.e6

Economics, 533.e33 经济

Edge-triggered flip-flop. See Flip-flops边沿触发触发器

EEPROM. See Electrically erasable programmable read only memory(EEPROM)电可擦除可编程只读存储器

EFLAGS register, 363：EFLAGS寄存器

Electrically erasable programmable read only memory (EEPROM), 270电可擦除可编程只读存储器

Embedded I/O (input/output) systems, 531.e3–531.e32 嵌入式I/O (输入/输出) 系统

analog I/O, 531.e25–531.e32 模拟I/O

A/D conversion, 531.e31–531.e3模/数转换

D/A conversion, 531.e31–531.e3数/模转换

digital I/O, 531.e31–531.e3数字I/O

general-purpose I/O (GPIO), 531.e31–531.e3通用I/O

interrupts, 531.e32 中断

LCDs. See Liquid Crystal Displays 液晶显示屏

microcontroller peripherals, 531.e32–531.e53单片机外围设备

motors. See Motors 电机

PIC32 microcontroller, 509 –513：PIC32单片机

serial I/O, 531.e11–531.e23. See also Serial I/O：串行I/O

timers, 531.e23–531.e24 计时器

VGA monitor. See VGA(Video Graphics Array) monitor VGA（视频图形阵列）显示器

Enabled flip-flops, 115 –116 使能触发器

Enabled registers, 196 –197. See also Flip-flops 使能寄存器

EOR (XOR), 303–304

EPROM. See Erasable programmable read only memory(EPROM) 可擦除可编程只读存储器

Equality comparator, 247 相等比较器

Equation minimization 等式最简化

using Boolean algebra, 65–66 使用布尔代数

using Karnaugh maps. See Karnaug maps(K-maps) 使用卡诺图

Erasable programmable read only memory (EPROM), 270, 533.e6 可擦除可编程只读存储器

Ethernet, 531.e61以太网

Exceptions, 346–350 异常

banked registers, 348–349 存储寄存器

exception-related instructions, 349–350 与异常有关的指示

exception vector table, 347–348 异常向量表

execution modes and privilege levels, 347 执行模式和权限级别

handler, 340, 349 处理程序

start-up, 350 启动

Execution time, 389执行时间

exit, 541.e41：exit

Extended instruction pointer (EIP), 362 扩展指令指针

ExtImm, 408

F

Factorial function call, 326 阶乘函数调用

stack during, 327 在栈

False, 8, 20, 35, 58, 60, 74, 111, 112, 113, 116, 124, 196 假

Fast Fourier Transform (FFT), 352 快速傅里叶变换

FDIV. See Floating-point division (FDIV) 浮点数除法

FFT. See Fast Fourier Transform (FFT) 快速傅里叶变换

Field programmable gate arrays (FPGAs), 274–279, 531.e14, 531.e38, 531.e63, 533.e7–533.e9 现场可编程逻辑门阵列

driving VGA cable, 531.e38 驱动VGA线

in SPI interface, 531.e13–531.e16 在SPI接口

File manipulation, in C, 541.e38–541.e40 C语言中文件操作

Finite state machines (FSMs), 123–141, 209–213, 413, 417 有限状态机（FSM）

complete multicycle control, 424 完整的多周期控制

deriving from circuit, 137–140 源于电路

divide-by-3 FSM, 129–131, 210–211 除以3FSM

factoring, 134–136, 136 分解

in HDL, 209–213 在HDL中

LE configuration for, 277–279 LE配置

Mealy FSM, 132–134 Mealy FSM

Moore FSM, 132–134 Moore FSM

snail/pattern recognizer FSM, 132–134, 212–213 蜗牛/模式识别FSM

state encodings, 129–131. See also Binary encoding, One-cold encoding, One-hot encoding 状态编码，另见二进制编码、独冷编码、独热编码

state transition diagram, 124, 125 状态转换图

traffic light FSM, 123–129 交通灯FSM

Fixed-point numbers, 255–256 定点数

Flags, 250 标志

Flash memory, 270. See also Solid state drives(SSD) 闪存，另见固态硬盘

Flip-flops, 114–118, 193–197. See also Registers 触发器，另见寄存器

back-to-back, 145, 152–157, 197. See also Synchronizer 背靠背，另见同步器

comparison with latches, 118 与锁存器比较

enabled, 115–116 使能

HDL for, 451. See also Registers: HDL，另见寄存器

metastable state of. See Metastability register, 114–115 亚稳态，另见亚稳态寄存器

resettable, 116 可重置

scannable, 262–263 可扫描

shift register, 261–263移位寄存器

transistor count, 114, 117 晶体管计数

transistor-level, 116–117 晶体管级

Float, C type, 541.e6–541.e9 C语言浮点数

print formats of, 541.e36–541.e37 打印格式

Floating output node, 117 浮点输出节点

Floating point division (FDIV) bug, 175 浮点数除法错误

Floating-gate transistor, 270. See also Flash memory 浮栅晶体管，另见闪存

Floating-point division (FDIV), 259 浮点数除法

Floating-point instructions, ARM, 346–347 ARM浮点数指令

Floating-point numbers, 256–258 浮点数

addition, 259 加法

formats, single- and double-precision, 258 格式，单精度与双精度

in programming. See Double, C type; Float, C type 在编程中

rounding, 259 四舍五入

special cases 特殊情况

infinity, 258 无穷大

NaN, 258：NaN

Floating-Point Status and Control Register (FPSCR), 358 浮点状态和控制寄存器

Floating-point unit (FPU), 259 浮点数单元

For loops, 312–313, 541.e20: for循环

Format conversion (atoi, atol, atof), 541.e41–541.e42 格式转换(atoi, atol, atof)

Forwarding, 432–435. See also Hazards 重定向。另见冲突

FPGAs. See Field programmable gate arrays(FPGAs) 现场可编程逻辑门阵列

FPU. See Floating-point unit(FPU) 浮点数单元

FPSCR. See Floating-Point Status and Control Register (FPSCR) 浮点状态和控制寄存器

Frequency shift keying (FSK), 531.e42 频移键控

and GFSK waveforms, 531.e42：GFSK波形

Front porch, 531.e37 前廊

FSK. See Frequency Shift Keying(FSK) 频移键控

FSMs. See Finite state machines(FSMs) 有限状态机

Full adder, 56, 182, 184, 200, 240 全加器

using always/process statement, 200 使用always/process语句

Fully associative cache, 499–500 全相联高速缓存

funct field, 330, 333: Funct域

Function calls, 317, 541.e15–541.e16 函数调用

additional arguments and local variables, 328–329 其他参数和局部变量

arguments, 319, 541.e15 参数

leaf, 324–326 叶子

multiple registers, loading and storing, 322 多个寄存器，加载和存储

naming conventions, 541.e16 命名惯例

nonleaf, 324–326 非叶子

preserved registers, 322–324 受保护寄存器

prototypes, 541.e16 原型

recursive, 326–328 递归

return, 318–319, 541.e15 返回

stack, use of, 320–322. See also Stack 栈

Furber, Steve, 473

Fuse-programmable ROM, 269–270 熔丝型可编程ROM

G

Gates 门

AND, 20, 22, 128 与

buffer, 20 缓冲

multiple-input, 21–22 多输入

NAND, 21, 31 与非

NOR, 21–22, 111, 128 或非

NOT, 20 非

OR, 21 或

transistor-level. See Transistors 晶体管级

XNOR, 21 同或

XOR, 21 异或

General-purpose I/O (GPIO), 531.e8–531.e11 通用IO（GPIO）

switches and LEDs example, 531.e8 开关与LED灯示例

Generate signal, 241, 243 生成信号

Genwaves function, 531.e27：Genwaves函数

Glitches, 92–95 毛刺

Global data segment, 340 全局数据段

GPIO. See General-purpose I/O(GPIO) 通用IO

Graphics accelerators, 469 图形加速器

Graphics processing unit (GPU), 460 图形处理单元

Gray, Frank, 76

Gray codes, 76 格雷码

Ground (GND), 22 接地

symbol for, 31 符号

H

Half adder, 240, 240 半加器

Hard disk, 490–491. See also Hard drive 硬盘

Hard drive, 490, 508, 496. See Solid state drive(SSD), Virtual memory 硬盘，另见固态硬盘、虚拟内存

Hardware description languages (HDLs). See also SystemVerilog, VHSIC Hardware Description Language (VHDL) 硬件描述语言，另见SystemVerilog、VHSIC硬件描述语言

2:1 multiplexer, 452 2：1多路复用器

adder, 450 加法器

capacity, 505 容量

combinational logic, 174, 198 组合逻辑

bitwise operators, 177–179 位操作

blocking and nonblocking assignments, 205–209 阻塞和非阻塞赋值

case statements, 201–202: case语句

conditional assignment, 181–182 条件赋值

delays, 188–189 延时

data memory, 455 数据内存

data types, 213–217 数据类型

history of, 174–175 历史

if statements, 202–205: if语句

internal variables, 182–184 内部变量

numbers, 185 数字

operators and precedence, 184–185 运算符和优先级

reduction operators, 180–181 缩减运算符

modules, 173–174 模块

parameterized modules, 217–220 参数化模块

processor building blocks, 449–452 处理器构建模块

register file, 450 寄存器文件

resettable flip-flop, 451 可复位触发器

resettable flip-flop with enable, 452 可使能的可复位触发器

sequential logic, 193–198, 209–213 时序逻辑

simulation and synthesis, 175–177 仿真与综合

single-cycle ARM processor, 443–456 单周期ARM 处理器

structural modeling, 190–193 结构建模

testbench, 220–224, 452–453 测试程序

top-level module, 454 顶级模块

Hardware handshaking, 531.e18 硬件握手

Hardware reduction, 70–71. See also Equation minimization 硬件减少，另见等式最简化

Hazard unit, 432–435 冲突单元

Hazards. See also Hazard unit 冲突，另见冲突单元

control hazards, 432, 437–440 控制冲突

data hazards, 432–436 数据冲突

pipelined processor, 431–441 流水线处理器

read after write (RAW), 431, 464 写入后读取（RAW）

solving 解决

control hazards, 437–440 控制冲突

forwarding, 432–434 重定向

stalls, 435–436 阻塞

write after read (WAR), 464 读取后写入（WAR）

write after write (WAW), 465 写入后写入（WAW）

H-bridge control, 531.e45：H桥控制

HDL. See Hardware description languages (HDLs), SystemVerilog, VHSIC Hardware Description Language (VHDL) ，HDL，另见硬件描述语言，SystemVerilog、VHSIC硬件描述语言

Heap, 340 堆

Heterogeneous multiprocessors, 469–470 异构多处理器

Hexadecimal numbers, 11–13 十六进制数

Hexadecimal to binary and decimal conversion, 11, 12 十六进制-二进制与十进制转换

Hierarchy, 6 层次化

HIGH, 23. See also 1, ON 高电平，另见1、开

High-level programming languages, 303, 541.e2 高级编程语言

compiling, assembling, and loading, 339–345 编译、汇编与载入

translating into assembly, 300 转换成汇编语言

High-performance microprocessors, 456 高性能微处理器

Hit, 490 命中

Hit rate, 491 命中率

Hold time constraint, 142–148 保持时间约束

with clock skew, 149–151 时钟偏移

Hold time violations, 145, 146, 147–148, 150–151 保持时间约束违反

Homogeneous multiprocessors, 468–469 同构多处理器

Hopper, Grace, 340

I

I/O. See Input/output (I/O) systems 输入/输出（I / O）系统

IA-32 architecture. See x86：IA-32体系结构，另见x86

IA-64, 368

ICs. See Integrated circuits (ICs) 集成电路

Idempotency theorem, 62 重叠定理

Identity theorem, 62 同一性定理

Idioms, 177 惯用语法

If statements: if语句

in ARM assembly, 309–310：ARM 汇编语言中

in C, 541.e17：C语言中

in HDL, 202–205：HDL中

If/else statements, 541.e17：if/else语句

in ARM assembly, 310–311：ARM汇编语言中

in C, 541.e17–541.e18：C语言中

in HDL, 202–205：HDL中

ILP. See Instruction level parallelism (ILP) 指令级并行

IM. See Instruction memory 指令存储器

imm8 field, 330-331 imm8域

imm12 field, 333 imm12域

imm24 field, 334 imm24域

Immediate addressing, 336 直接寻址

Immediate extension, 451 直接拓展

Immediates, 300–301, 330–332, 345–346. See also Constants 直接数，另见常数

Implicit leading one, 257 隐含前导位

Information, amount of, 8 信息量

Initializing 初始化

arrays in C, 541.e23–541.e24：C语言数组

variables in C, 541.e11：C语言变量

Input/Output (I/O) systems, 531.e1–531.e64 输入/输出系统

device driver, 531.e3, 531.e6–531.e8 设备驱动程序

embedded I/O systems. See Embedded I/O(input/output) systems 嵌入式输入/输出系统

I/O registers, 531.e3 I/O寄存器

memory-mapped I/O, 531.e1–531.e3 内存映射I/O

personal computer I/O systems. See Personal computer(PC) I/O systems 个人电脑I/O系统

Institute of Electrical and Electronics Engineers (IEEE), 257–258 电气电子工程师学会

Instruction encoding, x86, 364–367, 366 : x86指令编码

Instruction formats, ARM, 328, 328：ARM指令格式

addressing modes, 336 寻址方式

branch instructions, 334–335 分支指令

data-processing instructions, 329–333 数据处理指令

interpreting, 336–337 解读

memory instructions, 333–335 存储器指令

stored program, 337–338 存储程序

Instruction formats, x86, 364–367: x86指令格式

Instruction level parallelism (ILP), 465, 467, 468 指令级并行

Instruction memory, 387, 427, 455 指令存储器

Instruction register (IR), 407, 414 指令存储器

Instruction set, 295 指令集

for ARM, 386 对于ARM

Instruction set. See also Architecture 指令集，另见体系结构

Instructions, x86, 360–368: 指令，x86

Instructions, ARM, 295–360, 535–540 指令

branch instructions, 308–309, 539 分支指令

condition flags, 306–308, 540 条件标志

data-processing instructions, 535 数据处理指令

logical, 303–304, 536–537 逻辑

memory instructions, 301–303, 313–317, 333–334, 538 存储器指令

miscellaneous instructions, 539 其它控制类指令

multiply instructions, 305–306, 537 乘法指令

shift instructions, 304–305 移位指令

Instructions per cycle (IPC), 390 每周期指令数

Integrated circuits (ICs), 533.e17 集成电路

Intel. See x86

Intel processors, 360 Intel 处理器

Intel x86. See x86

Interrupts, 347, 531.e32 中断

Invalid logic level, 186 无效逻辑电平

Inverters, 20, 119, 178. See also NOT gate 反相器，另见非门

cross-coupled, 109, 110 交叉耦合

in HDL, 178, 199 在HDL中

An Investigation of the Laws of Thought (Boole), 8 《An Investigation of the Laws of Thought》(Boole著)

Involution theorem, 62 回旋定理

IOEs. See Input/output elements(IOEs) 输入/输出元素

IPC. See Instructions per cycle(IPC) 每周期指令数

IR. See Instruction register(IR) 指令寄存器

IR Write, 407, 414 IR写

J

Java, 303. See also Language：Java语言

K

Karnaugh, Maurice, 75

Karnaugh maps (K-maps), 75–84, 93–95, 126 卡诺图

logic minimization using, 77–83 用于逻辑最简化

prime implicants, 65, 77–81, 94–95 主蕴含式[麻烦改为“主蕴涵项”。]

seven-segment display decoder, 79–81 七段显示译码器

with “don’t cares,” 81–82 包含无关项

Kilobit (Kb/Kbit), 14：Kb

Kilobyte (KB), 14：KB

K-maps. See Karnaugh maps(K-maps) 卡诺图

L

LAB. See Logic array block(LAB) 逻辑阵列块

Land grid array, 531.e58 栅格阵列

Language. See also Instructions 编程语言，另见指令

assembly, 296–303 汇编

machine, 329–338 机器

mnemonic, 297 助记符

Last-in-first-out (LIFO) queue, 320. See also Stack 后进先出队列，另见栈

Latches, 111–113 锁存器

comparison with flip-flops, 109, 118 与触发器比较

D, 113, 120

SR, 111–113, 112

transistor-level, 116–117 晶体管级

Latency, 157–160, 425, 435 延时

Lattice, silicon, 27 晶格

LCDs. See Liquid crystal displays(LCDs) 液晶显示器

Leaf function, 324 叶子函数

Leakage current, 34 泄漏电流

Least recently used (LRU) replacement, 502–503 最近最少使用替换

two-way associative cache with, 502–503, 503 两路相联高速缓存

Least significant bit (lsb), 13, 14 最低有效位

Least significant byte (LSB), 13, 14, 301 最低有效字节

LEs. See Logic elements(LEs) 逻辑元素

Level-sensitive latch. See La\_Hlt414277542tches:D 电平敏感锁存器

LIFO. See Last-in-first-out(LIFO) queue 后进先出队列

Line options, compiler and command, 341–343, 541.e43–541.e45 编译器命令行选项

Linked list, 541.e33–541.e34 链表

Linker, 340–341 链接器

Linking, 339 链接

Linux, 531.e23–531.e24

Liquid crystal displays (LCDs),链接液晶显示屏

Literal, 58, 96 文字

Little-endian bus order in HDL, 178小端总线顺序

Little-endian memory addressing, 303 小端存储器寻址

Load register instruction (LDR), 301–302 加载寄存器指令

Loading literals, 345–346 加载文字

Loads, 344–345 加载

base addressing of, 336 基址寻址

Local variables, 328–329 局部变量

Locality, 488 局部性

Logic 逻辑

bubble pushing, 71–73 推气泡

combinational. See Combinational logic 组合逻辑

families, 25–26, 533.e15–533.e17, 533.e15, 533.e17 系列

gates. See Gates 门

hardware reduction, 70–71 硬件减少

multilevel. See Multilevel combinational logic 多级，另见多级组合逻辑

programmable, 533.e2–533.e9 可编程

sequential. See Sequential logic 时序逻辑

transistor-level. See Transistors 晶体管级

two-level, 69 二级

Logic array block (LAB), 276 逻辑阵列块

Logic arrays, 271–280. See also Field programmable gate arrays(FPGAs), Programmable logic arrays(PLAs) 逻辑阵列，另见现场可编程逻辑门阵列和可编程逻辑阵列

transistor-level implementation, 279–280 晶体管级实现

Logic elements (LEs), 275–279 逻辑元素

of Cyclone IV, 276–277

functions built using, 277–279 用于构建函数

Logic families, 25–26, 533.e15–533.e17, 533.e15, 533.e17 逻辑系列

compatibility of, 26 兼容性

logic levels of, 25 逻辑电平

specifications, 533.e15, 533.e17 规范说明

Logic gates, 533.e15, 533.e17 逻辑门

AND. See AND gate 与门

AND-OR (AO) gate, 46 与或门

with delays in HDL, 189 包含延时

multiple-input gates, 21–22 多输入门

NAND. See NAND gate 与非门

NOR. See NOR gate 或非门

Logic gates (Continued) 逻辑门（续）

NOT. See NOT gate 非门

OR. See OR gate 或门

OR-AND-INVERT (OAI) gate, 46 或与非(OAI)门

XNOR. See XNOR gate 同或门

XOR. See XOR gate 异或门

Logic simulation, 175–176 逻辑仿真

Logic synthesis, 176–177, 176 逻辑综合

Logical instructions, 303–304 逻辑指令

Logical shifter, 251 逻辑移位器

Lookup tables (LUTs), 270, 275–276 查找表

Loops, 312–313, 541.e19–541.e20 循环

in ARM assembly, 在ARM汇编语言中

for, 312–313

while, 312

in C, 在C语言中

do/while, 541.e19–541.e20

for, 541.e20

while, 541.e19

Lovelace, Ada, 338

LOW, 23. See also 0, FALSE 低电平，另见0、假

Low Voltage CMOS Logic (LVCMOS), 25 低电压CMOS逻辑

Low Voltage TTL Logic (LVTTL), 25 低电压TTL逻辑

LRU. See Least recently used replacement 最近最少使用替换

lsb. See Least significant bit 最低有效位

LSB. See Least significant byte 最低有效字节

LSL, 304

LSR, 304

LUTs. See Lookup tables(LUTs) 查找表

LVCMOS. See Low Voltage CMOS Logic(LVCMOS) 低电压CMOS逻辑

LVTTL. See Low Voltage TTL Logic(LVTTL) 低电压TTL逻辑

M

MAC. See Multiply-accumulate (MAC) 乘法累加

Machine code, See Machine language 机器代码，另见机器语言

Machine language, 329 机器语言

addressing modes, 336 寻址方式

branch instructions, 334–335 分支指令

data-processing instructions, 329–333 数据处理指令

interpreting, 336–337 解读

memory instructions, 333–335 存储器指令

stored program, 337–338, 338 存储程序

translating to assembly language, 337 翻译成汇编语言

Magnitude comparator, 247 数量比较器

Main decoder, 398–400, 400 主译码器

Main FSM, 413–423, 423 主FSM

main function in C, 541.e3：C语言中的main函数

Main memory, 489–491 主存储器

malloc function, 541.e32：Malloc函数

Mantissa, 257 尾数

Master-slave flip-flop, See Flip-flops 主-从触发器

Masuoka, Fujio, 270

math.h, C library, 541.e42–541.e43: C语言函数库

Max-delay constraint. See Setup time constraint 最大延时约束，另见建立时间约束

Maxterms, 58 最大项

MCUs. See Microcontroller units(MCUs) 微控制器单元

Mealy machines, 123, 123, 132–134 Mealy机器

state transition and output table, 134 状态转换和输出表

state transition diagrams, 133 状态转换图

timing diagrams for, 135 时序图

Mean time between failure (MTBF), 153–154平均故障间隔时间

Medium-scale integration (MSI) chips, 533.e2中等规模集成（MSI）芯片

Memory, 313. See also Memory arrays 存储器，另见存储器阵列

access time, 491 访问时间

　　addressing modes, 363　寻址模式

area and delay, 267–268　面积和延迟

big-endian, 302　大端

byte-addressable, 301–303　字节可寻址

HDL for, 272, 273, 455–456 硬件描述语言

hierarchy, 490　层次

little-endian, 303　小端

logic using, 270–271　逻辑

main, 490　主

operands in, 301–303　操作数

physical, 509　物理

ports, 265–266　端口

protection, 515. See also Virtual memory　保护，另见虚拟内存

types, 266–270　类型

DDR, 268 双倍数据速率

DRAM, 266–267 动态随机访问存储器

flash, 270　闪存

register file, 268　寄存器文件

ROM, 268–270 只读存储器

SRAM, 266 静态随机访问存储器

virtual, 490. See also Virtual memory　虚拟内存

Memory address computation, 419 内存地址计算

data flow during, 419 数据流

Memory and peripheral interface, 531.e55–531.e57 存储器和外设接口

Memory arrays, 264–271.See also Memory 存储器阵列，另见存储器

bit cell, 264–270 位元

HDL for, 272, 273, 455–456

logic using, 270–271 逻辑

organization, 264–265 组成

Memory hierarchy, 490–491 存储器层次

Memory instructions, 301–303, 313–317, 333–334, 391–394 存储器指令

encodings, 333–334, 538 编码

Memory interface, 487–488 存储器接口

Memory map, ARM339–340, 531.e2 内存映射

Memory performance. See Average Memory Access Time(AMAT) 存储器性能，另见平均内存访问时间

Memory protection, 515 存储器保护

Memory systems, 487 存储器系统

ARM, 507–508

performance analysis, 491–492 性能分析

x86, 531.e3

Memory-mapped I/O, 531.e1–531.e3, 531.e7 内存映射I/O

address decoder, 531.e1, 531.e2 地址译码器

communicating with I/O devices, 531.e2 与I/O设备通信

hardware, 531.e2, 531.e2, 531.e3 硬件

MemtoReg, 396, 397

Metal-oxide-semiconductor field effect transistors (MOSFETs), 26 金属氧化物半导体场效应晶体管

switch models of, 30 开关模型

Metastability, 151–157 亚稳态

metastable state, 110, 151 亚稳态

resolution time, 151–152, 154–157 解析时间

synchronizers, 152–154 同步器

Microarchitecture, 296, 385, 388–389. See also Architecture 微结构，另见体系结构

advanced. See Advanced microarchitecture 先进微结构

architectural state. See Architectural state 架构状态

description of, 385–389 描述

design process, 386–388 设计流程

evolution of, 470–476 演化

HDL representation, 443–456: HDL表示

generic building blocks, 449–452 通用构建块

single-cycle processor, 444–449 单周期处理器

testbench, 452–456 测试平台

multicycle processor. See Multicycle ARM processor 多周期处理器，另见多周期ARM处理器

performance analysis, 389–390. See also Performance analysis 性能分析

pipelined processor. See Pipelined ARM processor 流水线处理器，另见流水线ARM处理器

real-world perspective, 470–476 现实的角度

single-cycle processor. See Single-cycle ARM processor单周期处理器，另见单周期ARM处理器

Microcontroller, 531.e3, 531.e25 微控制器

Microcontroller peripherals, 531.e32–531.e53 微控制器外围设备

Bluetooth wireless communication, 531.e42–531.e43 蓝牙无线通信

character LCD, 531.e33–531.e36 字符LCD

control, 531.e35–531.e36 控制

parallel interface, 531.e33 并行接口

motor control, 531.e43–531.e53 电机控制

VGA monitor, 531.e36–531.e42: VGA显示器

Microcontroller units (MCUs), 531.e3 微控制器单元

Micro-operations (micro-ops), 458–459 微操作

designers, 456 设计者

high-performance, 456 高性能

Microprocessors, 3, 13, 295 微处理器

architectural state of, 338 架构状态

Millions of instructions per second, 425 每秒百万指令

Min-delay constraint. See Hold time constraint 最小延时约束，另见保持时间约束

Minterms, 58 最小项

Miss, 490–492, 505 缺失

capacity, 505 容量

compulsory, 505 强制

conflict, 498, 505 冲突

Miss penalty, 500 缺失惩罚

Miss rate, 491–492 缺失率

and access times, 492 访问次数

Misses 缺失

cache, 490 缓存

capacity, 505容量

compulsory, 505 强制

conflict, 505 冲突

page fault, 509–510 页面失效

ModR/M byte, 366 ModR / M字节

Modularity, 6 模块化

Modules, in HDL

behavioral and structural, 173–174 模块，在HDL行为模型和结构模型

parameterized modules, 217–220 参数化模块

Moore, Gordon, 30

Moore machines, 123, 132: Moore机

state transition and output table, 134 状态转换和输出表

state transition diagrams, 133 状态转换图

timing diagrams for, 135 时序图

Moore’s law, 30 摩尔定律

MOS transistors. See Metal-oxide semiconductor field effect transistors(MOSFETs) 金属氧化物半导体场效应晶体管

MOSFET. See Metal-oxide semiconductor field effect transistors(MOSFETs) 金属氧化物半导体场效应晶体管

Most significant bit (msb), 13, 14 最高有效位

Most significant byte (MSB), 13, 14, 301, 302 最高有效字节

Motors 电机

DC, 531.e43, 531.e44–531.e47 直流

H-bridge, 531.e45–531.e46, 531.e45, 531.e46：H桥

servo, 531.e44, 531.e48–531.e49 伺服

stepper, 531.e44, 531.e49–531.e53 步进

MOV, 301

MPSSE. See Multi-Protocol Synchronous Serial Engine(MPSSE) 多协议同步串行引擎

msb. See Most significant bit(msb) 最高有效位

MSB. See Most significant byte(MSB) 最高有效字节

MSI chips. See Medium-scale integration(MSI) chips 中等规模集成

MTBF. See Mean time between failure(MTBF) 平均故障间隔时间

Multicycle ARM processor, 406 多周期ARM处理器

control, 413–421 控制

datapath, 407–413 数据路径

B instruction, 412–413 B指令

data-processing instructions, 412 数据处理指令

LDR instruction, 407–410 LDR 指令

STR instruction, 411–412 STR 指令

performance, 421–425 性能

Multicycle microarchitectures, 388 多周期微架构

Multilevel combinational logic, 69–73. See also Logic 多级组合逻辑，另见逻辑

Multilevel page tables, 516–518 多级页表

Multiple-output circuit, 68–69 多输出电路

Multiplexers, 83–86 多路选择器

definition of, 83–84 定义

HDL for：HDL

behavioral model of, 181–183 行为模型

parameterized N-bit, 218–219 参数化N位

structural model of, 190–193 结构模型

logic using, 84–86 逻辑

symbol and truth table, 83 符号和真值表

Multiplicand, 252–253 被乘数

Multiplication. See Multiplier 乘法，另见乘法器

Multiplier, 252–253 乘法器

HDL for, 253: HDL

Multiply instructions, 305–306, 537, 537 乘法指令

Multiply and multiply-accumulate 乘法和乘法累加

instructions, 355–356 指令

Multiply-accumulate (MAC), 352, 356 乘法累加

Multiprocessors, 468–470 多处理器

chip, 468 芯片

heterogeneous, 469–470 异构

homogeneous, 468 同构

Multi-Protocol Synchronous Serial Engine (MPSSE), 531.e63 多协议同步串行引擎

Multithreaded processor, 467 多线程处理器

Multithreading, 467–468 多线程

Mux. See Multiplexers 多路选择器

myDAQ, 531.e62–531.e63

N

NAND (7400), 533.e3 与非（7400）

NAND gate, 21 与非门

CMOS, 31–32

Nested if/else statement, 311, 541.e18 嵌套if/else语句

Newton computer, 472

Nibbles, 13–14 半字节

nMOS transistors, 28–31, 29–30：nMOS晶体管

Noise margins, 23–26, 23 噪声容限

calculating, 23–24 计算

Nonarchitectural state, 386, 388 非架构状态

Nonblocking and blocking assignments, 199–200, 205–209 非阻塞与阻塞赋值

Nonleaf function calls, 324–326 非叶子函数调用

Nonpreserved registers, 322–323, 326 不受保护寄存器

NOP, 346, 431

NOR gate, 21–22, 63, 533.e3 或非门

chip (7402), 533.e3 芯片

CMOS, 32

pseudo-nMOS logic, 33 伪nMOS逻辑

truth table, 22 真值表

Not a number (NaN), 258

NOT gate, 20 非门

chip (7404), 533.e3 芯片

CMOS, 31

Noyce, Robert, 26

Null element theorem, 62 零元定理

Number conversion 数字转换

binary to decimal, 10–11 二进制-十进制

binary to hexadecimal, 12 二进制-十六进制

decimal to binary, 11, 13 十进制-二进制

decimal to hexadecimal, 13 十进制-十六进制

hexadecimal to binary and decimal, 11, 12 十六进制-二进制和十进制

taking the two’s complement, 16 取2的补码

Number systems, 9–19 数字系统

binary, 9–11, 10–11 二进制

comparison of, 18–19, 19 比较

estimating powers of two, 14 估算2的次方

fixed-point, 255, 255–256 定点数

floating-point, 256–259 浮点数

addition, 259, 260 加法

special cases, 258 特殊情况

hexadecimal, 11–13, 12 十六进制

negative and positive, 15 负数和正数

sign/magnitude, 15–16 符号/大小

signed, 15 有符号数

two's complement, 16–18 2的补

unsigned, 9–11 无符号数

O

Odds and ends, 345 什物

exceptions, 346–350 异常

loading literals, 345–346 加载文字

NOP, 346

OFF, 26, 30 关

Offset, 302, 392, 408 偏移

Offset indexing, ARM, 314 偏移索引

ON, 26, 30 开

One-bit dynamic branch predictor, 460 一位动态分支预测

One-cold encoding, 130 独冷编码

One-hot encoding, 129–131 独热编码

One-time programmable (OTP), 533.e2 一次性可编程（OTP）

op field, 330 op域

Opcode, See op field 操作码，另见op域

Operands 操作数

ARM, 298

constants/immediates, 300–301 常数/直接数

memory, 301–303 存储器

registers, 299 寄存器

register set, 300 寄存器组

x86, 362–363, 363

Operation code. See op field 操作代码，另见op域

Operators 运算符

in C, 541.e11–541.e14 在C语言中

in HDL, 177–185 在HDL中

bitwise, 177–181 位操作

precedence, 185 优先级

reduction, 180–181 缩减

table of, 185 表

ternary, 181–182 三元

OR gate, 21 或门

OR-AND-INVERT (OAI) gate, 46 或与非(OAI)门

ORR (OR), 303–304 或

OTP. See One-time programmable(OTP) 一次性可编程

Out-of-order execution, 466 乱序执行

Out-of-order processor, 463–465 乱序处理器

Output dependence, 465 输出依赖

Overflow 溢出

with addition, 15 加法

detection, 250–251 检测

Oxide, 28 氧化物

P

Packages, chips, 533.e17–533.e18 封装，芯片

Page fault, 509: 页面失效

Page number, 511: 页码

Page offset, 511：页偏移

Page table, 510–513: 页表

Pages, 509：页

Paging, 516：分页

Parallel I/O, 531.e11: 并行I/O

Parallelism, 157–160：并行

Parity gate. See XOR gate：奇偶校验门，另见异或门

Partial products, 252：部分乘积

Pass by reference, 541.e22: 按引用传递

Pass by value, 541.e22: 按数值传递

Pass gate. See Transmission gates 传输门

PC. See Program counter: 程序计数器

PC Logic, 400 PC逻辑

PCB. See Printed circuit boards (PCBs): 印刷电路板

PCI. See Peripheral Component Interconnect: 外围组件互连

PCI express (PCIe), 531.e60

PC-relative addressing, 335, 336: PC相对寻址

PCSrc, 394, 395–396, 440

PCWrite, 410

Perfect induction, proving theorems using, 64–65 完全归纳法，证明定理

Performance analysis, 389–390. See also Average Memory Access Time：性能分析，另见平均内存访问时间

multi-cycle ARM processor, 422–424：多周期ARM 处理器

pipelined ARM processor, 425–428: 流水线ARM 处理器

processor comparison, 424: 处理器比较

single-cycle ARM processor, 402: 单周期ARM 处理器

Performance Analysis, 389–390. See also Average Memory Access Time (AMAT) 性能分析，另见平均内存访问时间

Peripheral Component Interconnect (PCI), 531.e59–531.e60: 外围组件互连

Peripherals devices. See Input/output(I/O) systems：外围设备，另见输入/输出系统

Personal computer (PC). See x86：个人电脑

Personal computer (PC) I/O systems, 531.e57–531.e64：个人电脑I/O系统

data acquisition systems, 531.e62–531.e63: 数据采集系统

DDR3 memory, 531.e60–531.e61: DDR3内存

networking, 531.e61: 联网

PCI, 531.e59–531.e60: 外围组件互连

SATA, 531.e61–531.e62：SATA

USB, 531.e59, 531.e63–531.e64：USB

Phase locked loop (PLL), 531.e39：锁相环路

Physical memory, 509：物理内存

Physical page number (PPN), 511: 物理页码

Physical pages, 509: 物理页

Pipelined ARM processor, 425–428：流水线MIPS处理器

abstract view of, 427：抽象视图

control unit, 430 控制单元

datapath, 428–429：数据通路

description, 425–428 描述

hazards, 431–441 冲突

performance analysis, 441–443: 性能分析

throughput, 426：吞吐量

Pipelined microarchitecture. See Pipelined ARM processor 流水线微体系结构。另见流水线ARM 处理器

Pipelining, 158–160：流水线

PLAs. See Programmable logic arrays(PLAs)：可编程逻辑阵列

Plastic leaded chip carriers (PLCCs), 533.e17：塑封引线芯片载体

Platters, 508 盘片

PLCCs. See Plastic leaded chip carriers(PLCCs): 塑封引线芯片载体

PLDs. See Programmable logic devices(PLDs)：可编程逻辑器件

PLL. See Phase locked loop (PLL)：锁相环路

pMOS transistors, 28–31, 29：pMOS晶体管

Pointers, 541.e21–541.e23, 541.e25, 541.e28, 541.e30, 541.e32 指针

POS. See Product-of-sums(POS) form：POS，另见或与式

Positive edge-triggered flip-flop, 114：正边沿触发触发器

Power consumption, 34–35: 能量消耗

Power-saving and security instructions, 358 节电和安全指令

PPN. See Physical page number (PPN)：物理页码

Prefix adders, 243–245, 244：前缀加法器

Prefix tree, 245：前缀树

Pre-indexed addressing, ARM, 314 预索引寻址

Preserved registers, 322–324, 323: 受保护寄存器

Prime implicants, 65, 77：主蕴涵项

Printed circuit boards (PCBs), 533.e19–533.e20：印刷电路板

printf, 541.e35–541.e37

Priority 优先级

circuit, 68–69 电路

encoder, 102–103, 105 编码器

Procedure calls. See Function calls: 过程调用，另见函数调用

Processor performance comparison, 442: 处理器性能比较

multicycle ARM processor, 424: 多周期ARM 处理器

pipelined ARM processor, 442: 流水线ARM 处理器

single-cycle processor, 405:单周期处理器

Processor-memory gap, 489处理器-存储器差距

Product-of-sums (POS) form, 60：或与式

Program counter (PC), 308, 338, 387, 394: 程序计数器

Programmable logic arrays (PLAs), 67, 272–274, 533.e6–533.e7: 可编程序逻辑阵列

transistor-level implementation, 280: 晶体管级实现

Programmable logic devices (PLDs), 533.e6: 可编程逻辑器件

Programmable read only memories (PROMs), 269, 271, 533.e2–533.e6: 可编程只读存储器

Programming 编程

in ARM, 303 在ARM中

arrays. See Arrays 数组

branching. See Branching 分支

in C. See C programming：C语言编程

conditional statements, 309–312 条件语句

condition flags, 306–308 条件标志

constants. See Constants, Immediates 常数，另见直接数

function calls. See Functions 函数调用，另见函数

getting loopy, 312–313 变成循环

logical and arithmetic instructions, 303–306 逻辑和算术指令

loops. See Loops 循环

memory, 313–317 存储器

shift instructions, 304–305 移位指令

PROMs. See Programmable read only memories(PROMs): 可编程只读存储器

Propagate signal, 241:传播信号

Propagation delay, 88–92. See also Critical path: 传输延迟，另见关键路径

Pseudoinstructions, 346：伪指令

Pseudo-nMOS logic, 33–34, 33：伪nMOS逻辑

NOR gate, 33 或非门

ROMs and PLAs, 279–280：ROM和PLA

Pulse-Width Modulation (PWM), 531.e28–531.e31 脉宽调制(PWM)

analog output with, 531.e30–531.e31 模拟输出

duty cycle, 531.e28 占空比

signal, 531.e28 信号

PWM. See Pulse-Width Modulation(PWM) 脉宽调制

Q

Quiescent supply current, 34：静态电源电流

R

Race conditions, 119–120, 120: 竞争条件

rand, 541.e40–541.e41

Random access memory (RAM), 266–268, 271, 272：随机存取存储器

Raspberry Pi, 531.e3–531.e4, 531.e5, 531.e6, 531.e32, 531.e48–531.e49

RAW hazard. See Read after write (RAW) hazard RAW 冲突。另见写入后读取（RAW）冲突

Rd field, 330 Rd域

Read after write (RAW) hazards, 431, 464. See also Hazards：写入后读取(RAW)冲突

Read only memory (ROM), 266, 268–270：只读存储器

transistor-level implementation, 279–280：晶体管级实现

Read/write head, 508：读/写头

ReadData bus, 393, 394 ReadData总线

Receiver gate, 22: 接收门

Recursive function calls, 326–328: 递归函数调用

Reduced instruction set computer (RISC) architecture, 298, 458: 精简指令集计算机(RISC)体系结构

Reduction operators, 180–181：缩减运算符

Register file (RF)：寄存器文件

ARM register descriptions, 299: ARM寄存器描述

HDL for, 449

in pipelined ARM processor (write on falling edge), 428 在流水线ARM处理器中（下降沿写入）

schematic, 268 电路图

use in ARM processor, 387 在ARM处理器中使用

Register renaming, 465–467：寄存器重命名

Register set, 300. See also Register file (RF) 寄存器组，另见寄存器文件

Registers. See ARM registers;Flip-flops; x86 registers：寄存器，另见ARM 寄存器；触发器；x86寄存器

loading and storing, 322 加载和存储

preserved and nonpreserved, 322–324 受保护的和非受保护的

RegSrc, 402

Regularity, 6：规整化

RegWrite, 393, 433

Replacement policies, 516：替换策略

Resettable flip-flops, 116：复位触发器

Resettable registers, 194–196：复位寄存器

Resolution time, 151–152. See also Metastability：解析时间。另见亚稳态

derivation of, 154–157 来源

Return value, 317 返回值

RF. See Register file(RF)：寄存器文件

Ring oscillator, 119, 119：环形振荡器

Ripple-carry adder, 240, 240–241, 243：行波进位加法器

RISC architecture. See Reduced instruction set computer (RISC) architecture RISC 架构。另见精简指令集计算机（RISC）架构

Rising edge, 88：上升沿

Rm field, 330 Rm域

Rn field, 330 Rn域

ROM. See Read only memory (ROM): 只读存储器

ROR, 304

rot field, 330-331 rot域

Rotations per minute (RPM), 531.e44:每分钟转数(RPM)

Rotators, 251–252: 旋转器

Rounding modes, 259: 舍入模式

RPM. See Rotations per minute (RPM): 每分钟转数

RS-232, 531.e18

S

Sampling, 141: 采样

Sampling rate, 531.e25：采样率

SATA. See Serial ATA (SATA)：SATA，另见串行ATA

Saturated arithmetic, 353 饱和算术

Scalar processor, 461–463, 460：标量处理器

Scan chains, 262–263：扫描链

scanf, 541.e38

Scannable flip-flop, 262–263：可扫描触发器

Schematics, rules of drawing, 31, 67：电路图，绘图规则

SCK. See Serial Clock (SCK)：串行时钟

SDI. See Serial Data In (SDI): 串行数据输入

SDO. See Serial Data Out (SDO): 串行数据输出

SDRAM. See Synchronous dynamic random access memory (SDRAM): 同步动态随机存取存储器

Segment descriptor, 367: 段描述符

Segmentation, 367: 分段

Selected signal assignment statements, 182：选择信号赋值语句

Semiconductors, 27半导体

industry, sales, 3 工业，销售

Sequencing overhead, 143–144, 149, 160, 442测序开销

Sequential building blocks. See Sequential logic 时序逻辑构建模块，另见时序逻辑

Sequential logic, 109–161, 259–263：时序逻辑

counters, 260 计数器

finite state machines. See Finite state machines (FSMs) 有限状态机

flip-flops, 114–118. Also see Registers 触发器，另见寄存器

latches, 111–113 锁存器

D, 113

SR, 111–113

registers. See Registers 寄存器

shift registers, 261–263 移位寄存器

timing of. See Timing Analysis 时序，另见时序分析

Serial ATA (SATA), 531.e62：串行ATA

Serial Clock (SCK), 531.e12：串行时钟

Serial communication, with PC, 531.e20 串行通信，与PC

Serial Data In (SDI), 531.e12 串行数据输入

Serial Data Out (SDO), 531.e12串行数据输出

Serial I/O, 531.e11–531.e23串行I/O

SPI. See Serial peripheral interface(SPI): 串行外设接口

UART. See Universal Asynchronous Receiver Transmitter (UART): 通用异步收发器

Serial Peripheral Interface (SPI), 531.e11, 531.e12–531.e17: 串行外设接口

connection between PI and FPGA, 531.e14: PI与FPGA连接

ports 端口

Serial Clock (SCK), 531.e12 串行时钟

Serial Data In (SDI), 531.e12 串行数据输入

Serial Data Out (SDO), 531.e12 串行数据输出

register fields in, 531.e13 寄存器域

slave circuitry and timing, 531.e15 从电路与时序

waveforms, 531.e12 波形

Servo motor, 531.e44, 531.e48–531.e49:伺服电机

Set bits, 495: 设置位

Setup time constraint, 142, 145–147 建立时间约束

with clock skew, 148–150 包含时钟偏移

Seven-segment display decoder, 79–82 七段显示译码器

with don’t cares, 82–83 包含无关项

HDL for, 201–202

Shaft encoder, 531.e43, 531.e47–531.e48, 531.e48: 轴角编码器

Shift instructions, 304–305, 305: 移位指令

Shift registers, 261–263: 移位寄存器

Shifters, 251–252: 移位器

Short path, 89–92: 最短路径

Sign bit, 16: 符号位

Sign extension, 18: 符号扩展

Sign/magnitude numbers, 15–16, 255 带符号的原码

Signed binary numbers, 15–19：有符号二进制数

Signed multiplier, 217：有符号乘法器

Silicon dioxide (SiO2), 28：二氧化硅

Silicon lattice, 27: 硅晶格

SIMD. See Single instruction multiple data(SIMD): SIMD，另见单指令多数据

SIMD instructions, 358–360 SIMD 指令

simple function, 318 simple 函数

Simple programmable logic devices (SPLDs), 274：简单可编程逻辑器件

Simulation waveforms, 176：仿真波形

with delays, 189 包含延时

Single instruction multiple data (SIMD), 460, 472 单指令多数据(SIMD)

Single-cycle ARM processor, 390, 444: 单周期MIPS处理器

Conditional Logic, 447–448 条件逻辑

control, 397–401 控制

controller, 445 控制器

datapath, 390, 448–449 数据通路

B instruction, 396–397 B指令

data-processing instructions, 395–396 数据处理指令

LDR instruction, 391–394 LDR指令

STR instruction, 394–396 STR指令

Decoder, 446 译码器

instructions, 402 指令

performance, 402–405 性能

Single-cycle microarchitecture, 388 单周期微架构

Single-precision formats, 258. See also Floating-point numbers：单精度格式，另见浮点数

Skew. See Clock skew：偏斜，另见时钟偏斜

Slash notation, 56：斜线记法

Slave latch, 114. See also Flip-flops 从锁存器，另见触发器

Small-scale integration (SSI) chips, 533.e2小规模集成芯片

Solid state drive (SSD), 490. See also Flash memory, Hard drive：固态硬盘，另见闪存，硬盘

SOP. See Sum-of-products (SOP) form ：SOP，另见与或式

Spatial locality, 488, 500–502：空间局部性

Spatial parallelism, 157–158：空间并行

SPEC, 389

SPECINT2000, 424

SPI. See Serial Peripheral Interface (SPI)：串行外设接口

Spinstepper function, 557：Spinstepper函数

Squashing, 465 挤压

SR latches, 111–113, 112：SR锁存器

SRAM. See Static random access memory (SRAM)：静态随机存取存储器

srand, 541.e40–541.e41

Src2 field, 330, 333 Src2域

SSI chips. See Small-scale integration(SSI) chips 小规模集成芯片

Stack, 320–329. See also Function calls 栈，另见函数调用

during recursive function call, 320–329 在递归函数调用中

preserved registers, 322–324 受保护寄存器

stack frame, 322, 328 栈帧

stack pointer (SP), 320 栈指针

storing additional arguments on, 328–329 存储额外参数

storing local variables on, 328–329 存储局部变量

Stalls, 435–436. See also Hazards 阻塞，另见冲突

Standard libraries, 541.e35–541.e43：标准程序库

math, 541.e42–541.e43

stdio, 541.e35–541.e40

file manipulation, 541.e38–541.e40 文件操作

printf, 541.e35–541.e37

scanf, 541.e38

stdlib, 541.e40–541.e42

exit, 541.e41

format conversion (atoi, atol, atof), 541.e41–541.e42 格式转换(atoi, atol, atof)

rand, srand, 541.e40–541.e41

string, 541.e43

State encodings, FSM, 129–131, 134. See also Binary encoding, One-cold encoding, One-hot encoding : FSM状态编码，另见二进制编码、独冷编码、独热编码

State machine circuit. See Finite state machines (FSMs)：状态机电路，另见有限状态机

State variables, 109：状态变量

Static branch prediction, 459：静态分支预测

Static discipline, 24–26：静态约束

Static power, 34：静态功耗

Static random access memory (SRAM), 266, 267, 519: 静态随机存取存储器

Status flags, 363. See also Condition flags: 状态标志。另见条件标志

stdio.h, C library, 541.e35–541.e40. See also Standard libraries: stdio.h，C函数库，另见标准函数库

stdlib.h, C library, 541.e40–541.e42. See also Standard libraries: stdlib.h，C函数库，另见标准函数库

Stepper motors, 531.e44, 531.e49–531.e53 步进电机

bipolar stepper motor, 531.e49, 531.e50–531.e52 双极步进电机

half-step drive, 531.e50, 531.e51 半步驱动

two-phase-on drive, 531.e50, 531.e51 两相驱动

wave drive, 531.e52–531.e53 波驱动

Stored program, 337–338 存储程序

STR, 394–396

string.h, C library, 541.e43: string.h，C函数库

Strings, 316–317, 541.e28–541.e29. See also Characters (char) 字符串，另见字符（char）

Structural modeling, 173–174, 190–193: 结构建模

Structures (struct), 541.e29–541.e31：结构体(struct)

SUB, 297

Substrate, 28–29：衬底

Subtraction, 17, 246, 297: 减法

Subtractor, 246–247: 减法器

Sum-of-products (SOP) form, 58–60 与或式

Superscalar processor, 461–463：超标量处理器

Supervisor call (SVC) instruction, 349 主管呼叫（SVC）指令

Supply voltage, 22. See also VDD 电源电压，另见VDD

SVC. See Supervisor call (SVC) instruction SVC。另见主管呼叫（SVC）指令

Swap space, 516：交换空间

Switch/case statements ：Switch / case语句

in ARM assembly, 317 在ARM 汇编中

in C, 541.e17–541.e18在C语言中

in HDL. See case statement, in HDL 在HDL中，另见case语句

Symbol table, 342, 343 符号表

Symmetric multiprocessing (SMP), 468. See also Homogeneous multiprocessors: 对称多处理，另见同构多处理器

Synchronizers, 152–154, 152–153: 同步器

Synchronous circuits, 122–123: 同步电路

Synchronous dynamic random access memory (SDRAM), 268同步动态随机存取存储器(SDRAM)

DDR, 268 双倍数据速率

Synchronous logic, design, 119–123：同步逻辑设计

Synchronous resettable flip-flops, 116：同步复位触发器

Synchronous sequential circuits, 120–123, 122. See also Finite state machines (FSMs)：同步时序电路，另见有限状态机

timing specification. See Timing analysis：时序规范，另见时序分析

Synergistic processor elements (SPEs), 457：协同处理器元素(SPE)

Synergistic Processor Unit (SPU) ISA, 458：协同处理器单元(SPU) ISA

SystemVerilog, 173–225. See also Hardware description languages(HDLs): SystemVerilog，另见硬件描述语言

accessing parts of busses, 188, 192 访问总线部件

bad synchronizer with blocking assignments, 209 使用阻塞赋值的错误的同步器

bit swizzling, 188 位交叉混合

blocking and nonblocking assignment, 199–200, 205–208 阻塞和非阻塞赋值

case statements, 201–202, 205：case语句

combinational logic using, 177–193, 198–208, 217–220 组合逻辑

comments, 180 注释

conditional assignment, 181–182 条件语句

data types, 213–217 数据类型

decoders, 202–203, 219 译码器

delays (in simulation), 189 延时（在仿真中）

divide-by-3 FSM, 210–211 除以3 FSM

finite state machines (FSMs), 209–213 : 有限状态机

Mealy FSM, 213

Moore FSM, 210, 212

full adder, 184 全加器

using always/process, 200 使用always/process

using nonblocking assignments, 208 使用非阻塞赋值

history of, 175 历史

if statements, 202–205：if语句

internal signals, 182–184 内部信号

inverters, 178, 199 反相器

latches, 198 锁存器

logic gates, 177–179:逻辑门

multiplexers, 181–183, 190–193, 218–219: 多路选择器

multiplier, 217：乘法器

numbers, 185–186 数字

operators, 185 运算符

parameterized modules, 217–220：参数化模块

N:2N decoder, 219：N:2N 译码器

N-bit multiplexers, 218–219：N位多路选择器

N-input AND gate, 220：N输入与门

priority circuit, 204: 优先级电路

using don’t cares, 205 使用无关项

reduction operators, 180–181 缩减运算符

registers, 193–197 寄存器

enabled, 196 使能

resettable, 194–196 复位

sequential logic using, 193–198, 209–213 时序逻辑

seven-segment display decoder, 201七段显示译码器

simulation and synthesis, 175–177仿真和综合

structural models, 190–193 结构模型

synchronizer, 197 同步器

testbench, 220–224 测试程序

self-checking, 222 自测试

simple, 221 简单

with test vector file, 223–224带测试向量

tristate buffer, 187 三态缓冲

truth tables with undefined and floating inputs, 187, 188 未定义和浮空输入的真值表

z’s and x’s, 186–188, 205：z和x

T

Tag, 495 标签

Taking the two’s complement, 16–17 取2的补码

Temporal locality, 488, 493–494, 497, 502：时间局部性

Temporal parallelism, 158–159：时间并行

Temporary registers, 299：临时寄存器

Ternary operators, 181, 541.e13：三元运算符

Testbenches, HDLs, 220–224 测试程序，HDL

self-checking, 221–222自测试

simple, 220–221简单

with testvectors, 222–224带测试向量

Text Segment, 340, 344文本段

Thin Quad Flat Pack (TQFP), 533.e17：薄型四方扁平封装(TQFP)

Thread level parallelism (TLP), 467：线程级并行

Threshold voltage, 29：阈值电压

Throughput, 157–160, 388, 425, 468：吞吐量

Thumb instruction set, 351–352 Thumb 指令集

Timers, 531.e23–531.e24 计时器

Timing 时序

of combinational logic, 88–95 组合逻辑

delay. See Contamination delay; Propagation delay 延迟，另见最小延迟；传输延迟

glitches. See Glitches 毛刺

of sequential logic, 141–157 时序逻辑

analysis. See Timing analysis 分析，另见时序分析

clock skew. See Clock skew 时钟偏移

dynamic discipline, 141–142 动态约束

metastability. See Metastability 亚稳态

resolution time. See Resolution time 解析时间

system timing. See Timing analysis 系统时序，另见时序分析

Timing analysis, 141–151: 时序分析

calculating cycle time. See Setup time constraint 计算周期时间，另见建立时间约束

with clock skew. See Clock skew 带有时钟偏移。另见时钟偏移

hold time constraint. See Hold time constraint保持时间约束

max-delay constraint. See Setup time constraint最大延时约束，另见建立时间约束

min-delay constraint. See Hold time constraint最小延时约束，另见保持时间约束

multicycle processor, 424 多周期处理器

pipelined processor, 441 流水线处理器

setup time constraint. See Setup time constraint建立时间约束

single-cycle processor, 405单周期处理器

TLB. See Translation lookaside buffer(TLB)：地址转换后备缓冲

TLP. See Thread level parallelism (TLP) 线程级并行

Transistors, 26–34：晶体管

bipolar, 26 双极

CMOS, 26–33

gates made from, 31–34 门

latches and flip-flops, 116–117 锁存器和触发器

MOSFETs, 26

Transistors (Continued) 晶体管（续）

nMOS, 28–34, 29–33

pMOS, 28–34, 29–33

pseudo-nMOS, 33–34伪nMOS

ROMs and PLAs, 279–280：ROM和PLA

transmission gate, 33

Transistor-Transistor Logic (TTL), 25–26, 533.e15–533.e16: 晶体管－晶体管逻辑

Translating and starting a program, 339: 转换和开始执行程序

Translation lookaside buffer (TLB), 514–515: 地址转换后备缓冲

Transmission Control Protocol and: 传输控制协议

Internet Protocol (TCP/IP), 531.e61

Transmission gates, 33: 传输门

Transmission lines, 533.e20–533.e33：传输线

characteristic impedance (Z0), 533.e30–533.e31：特性阻抗(Z0)

derivation of, 533.e30–533.e31来源

matched termination, 533.e22–533.e24：匹配终端

mismatched termination, 533.e25–533.e28不匹配终端

open termination, 533.e24–533.e25开路终端

reflection coefficient (kr), 533.e31–533.e32反射系数(kr)

derivation of, 533.e31–533.e32来源

series and parallel terminations, 533.e28–533.e30 串联和并联终端

short termination, 533.e25 短路终端

when to use, 533.e28 何时使用

Transparent latch. See Latches: D：透明锁存器，另见锁存器：D

Traps, 347：自陷

Tristate buffer, 74–75, 187：三态缓冲器

HDL for, 186–187

multiplexer built using, 84–85, 91–93 用于构建多路选择器

Truth tables, 20真值表

ALU decoder, 399, 404：ALU译码器

with don’t cares, 69, 81–83, 205带无关项

multiplexer, 83多路选择器

seven-segment display decoder, 79七段显示译码器

SR latch, 111, 112：SR锁存器

with undefined and floating inputs, 187–188带未定义和浮空输入

TSOP. See Thin small outline package(TSOP): 薄型小尺寸封装

TTL. See Transistor-Transistor Logic(TTL): 晶体管-晶体管逻辑

Two’s complement numbers, 16–18：2的补码

Two-bit dynamic branch predictor, 460: 双位动态分支预测

Two-cycle latency of LDR, 435：lw的两周期延时

Two-level logic, 69: 双电平逻辑

typedef, 541.e31–541.e32

U

UART. See Universal Asynchronous Receiver Transmitter(UART): UART，另见通用异步收发器

Unconditional branches, 308, 309: 无条件分支

Undefined instruction exception, 347：未定义指令异常

Unicode, 315

Unit under test (UUT), 220: 被测单元(UUT)

Unity gain points, 24单位增益点

Universal Asynchronous Receiver Transmitter (UART), 531.e17–531.e23：通用异步收发器(UART),

hardware handshaking, 531.e18 硬件握手

Universal Serial Bus (USB), 270, 531.e18, 531.e59：通用串行总线(USB)

USB 1.0, 531.e59

USB 2.0, 531.e59

USB 3.0, 531.e59

Unsigned multiplier, 217, 252–253：无符号乘法器

Unsigned numbers, 18：无符号数

Upton, Eben, 531.e4

USB. See Universal Serial Bus(USB)：USB，另见通用串行总线

USB links, 531.e63–531.e64：USB链接

FTDI, 531.e63

UM232H module, 531.e64: UM232H模块

Use bit (U), 502使用位(U)

V

Valid bit (V), 496：有效位(V)

Variables in C, 541.e7–541.e11：C语言中的变量

global and local, 541.e9–541.e10 全局和局部

initializing, 541.e11 初始化

primitive data types, 541.e8–541.e9 基本数据类型

VCC, 23. See also Supply voltage, VDD：VCC，另见电源电压、VDD

VDD, 22, 23. See also Supply voltage：VDD，另见电源电压

Vector processor, 460：向量处理器

Verilog. See SystemVerilog：Verilog，另见SystemVerilog

Very High Speed Integrated Circuits (VHSIC), 175. See also VHSIC Hardware Description Language

(VHDL)：VHSIC ，另见VHSIC硬件描述语言（VHDL）

VGA (Video Graphics Array) monitor, 531.e36–531.e42：VGA（视频图形阵列）显示器

connector pinout, 531.e37 接口引脚

driver for, 531.e39–531.e42 驱动程序

VHDL. See VHSIC Hardware Description Language(VHDL): VHDL，另见VHSIC硬件描述语言

VHSIC. See Very High Speed Integrated Circuits(VHSIC): VHSIC

VHSIC Hardware Description Language (VHDL), 173–175: VHSIC硬件描述语言(VHDL)

accessing parts of busses, 188, 192 访问总线部件

bad synchronizer with blocking assignments, 209 使用阻塞赋值的错误的同步器

bit swizzling, 188 位交叉混合

blocking and nonblocking assignment, 199–200, 205–208 阻塞和非阻塞赋值

case statements, 201–202, 205：case语句

combinational logic using, 177–193, 198–208, 217–220 组合逻辑

comments, 180 注释

conditional assignment, 181–182 条件语句

data types, 213–217 数据类型

decoders, 202–203, 219 译码器

delays (in simulation), 189 延时（在仿真中）

divide-by-3 FSM, 210–211 除以3 FSM

finite state machines (FSMs), 209–213 : 有限状态机

Mealy FSM, 213

Moore FSM, 210, 212

full adder, 184 全加器

using always/process, 200 使用always/process

using nonblocking assignments, 208 使用非阻塞赋值

history of, 175 历史

if statements, 202：if语句

internal signals, 182–184 内部信号

inverters, 178, 199 反相器

latches, 198 锁存器

logic gates, 177–179:逻辑门

multiplexers, 181–183, 190–193, 218–219: 多路选择器

multiplier, 217：乘法器

numbers, 185–186 数字

operators, 185 运算符

parameterized modules, 217–220：参数化模块

N:2N decoder, 219：N:2N 译码器

N-bit multiplexers, 218–219：N位多路选择器

N-input AND gate, 220：N输入与门

priority circuit, 204: 优先级电路

reduction operators, 180–181 缩减运算符

using don’t cares, 205 使用无关项

reduction operators, 180–181 缩减运算符

registers, 193–197 寄存器

enabled, 196 使能

resettable, 194–196 复位

sequential logic using, 193–198, 209–213 时序逻辑

seven-segment display decoder, 201七段显示译码器

simulation and synthesis, 175–177仿真和综合

structural models, 190–193 结构模型

synchronizer, 197 同步器

testbench, 220–224 测试程序

self-checking, 222 自测试

simple, 221 简单

with test vector file, 223–224带测试向量

tristate buffer, 187 三态缓冲

truth tables with undefined and floating inputs, 187, 188 未定义和浮空输入的真值表

z’s and x’s, 186–188, 205：z和x

Video Graphics Array (VGA). See VGA(Video Graphics Array) monitor视频图形阵列(VGA)，另见VGA（视频图形阵列）显示器

Virtual address, 509 虚拟地址

space, 515:空间

Virtual memory, 490, 508–518：虚拟内存

address translation, 509–512地址转换

cache terms comparison, 510 缓存术语比较

memory protection, 515 内存保护

multilevel page tables, 516–518多级页表

page fault, 509–510 页面失效

page number, 511 页码

page offset, 511 页偏移

pages, 509 页

page table, 512–513 页表

replacement policies, 516 替换策略

translation lookaside buffer (TLB), 514–515 地址转换后备缓冲

write policy, 506–507写策略

Virtual page number (VPN), 512: 虚拟页码(VPN)

Virtual pages, 509: 虚拟页

VSS, 23

W

Wafers, 28硅片

Wait for event (WFE) instruction, 358 等待事件（WFE）指令

Wait for interrupt (WFI) instruction, 358 等待中断（WFI）指令

Wall, Larry, 20

WAR hazard. See Write after read (WAR) hazard：WAR冲突，另见读取后写入（WAR）冲突

WAW hazard. See Write after write (WAW) hazard：WAW冲突，另见写入后写入（WAW）冲突

Weak pull-up, 33弱上拉

Weird number, 18怪异数

WFE. See Wait for event (WFE) instruction 等待事件（WFE）指令

WFI. See Wait for interrupt (WFI) instruction 等待中断（WFI）指令

while loops, 312, 541.e19：while循环

White space, 180空格

Whitmore, Georgiana, 7

Wi-Fi, 531.e61

Wilson, Sophie, 472

Wire, 67：导线

Wireless communication, Bluetooth, 531.e42–531.e43 无线通信，蓝牙

Wordline, 264字线

Write after read (WAR) hazard, 464. See also Hazards读取后写入（WAR）冲突，另见冲突

Write after write (WAW) hazard, 464–465 写入后写入（WAW）冲突

Write policy, 506–507 写策略

write-back, 506–507写回

write-through, 506–507 写直达

X

X. See Contention(x), Don’t care(X)：X，另见竞争、无关项

x86

architecture, 360–368, 362 体系结构

big picture, 368 主要部分

branch conditions, 366分支条件

instruction encoding, 364–367 指令编码

instructions, 364–367 指令

memory addressing modes, 363 内存寻址模式

operands, 362–363操作数

peculiarities, 368 特点

registers, 362 寄存器

status flags, 350状态标志

Xilinx FPGA, 275

XNOR gate, 21–22: 同或门

XOR gate, 21: 异或门

Z

Z. See Floating：Z，另见浮空