

5 4 3 2 1

Cyborg-N/V/L 14/15 TGL-U & Watchmen 14N TGL-U Schematic

2021-01-07
REV : A00

DY : None Installed

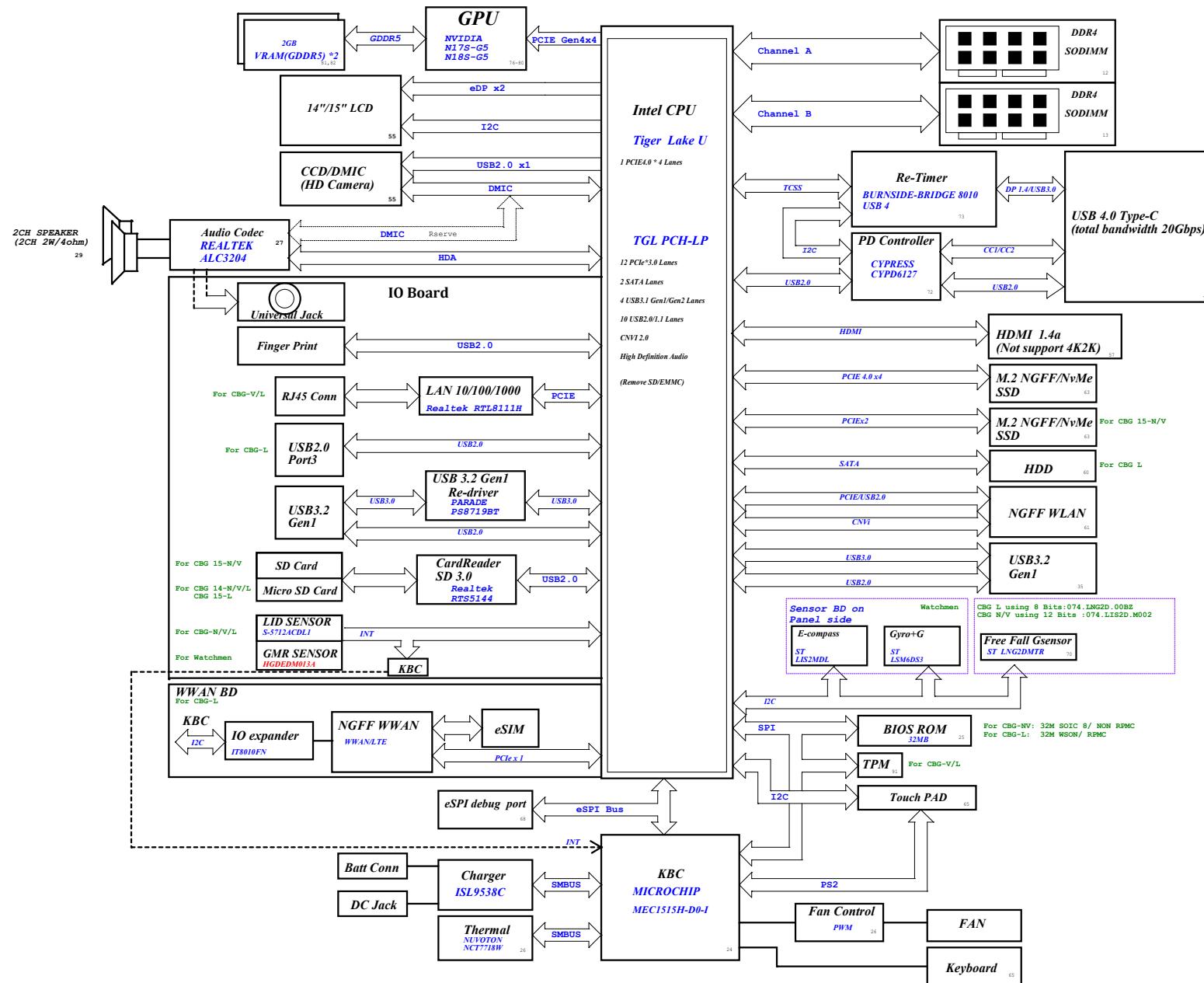
UMA: Unified Memory Architecture

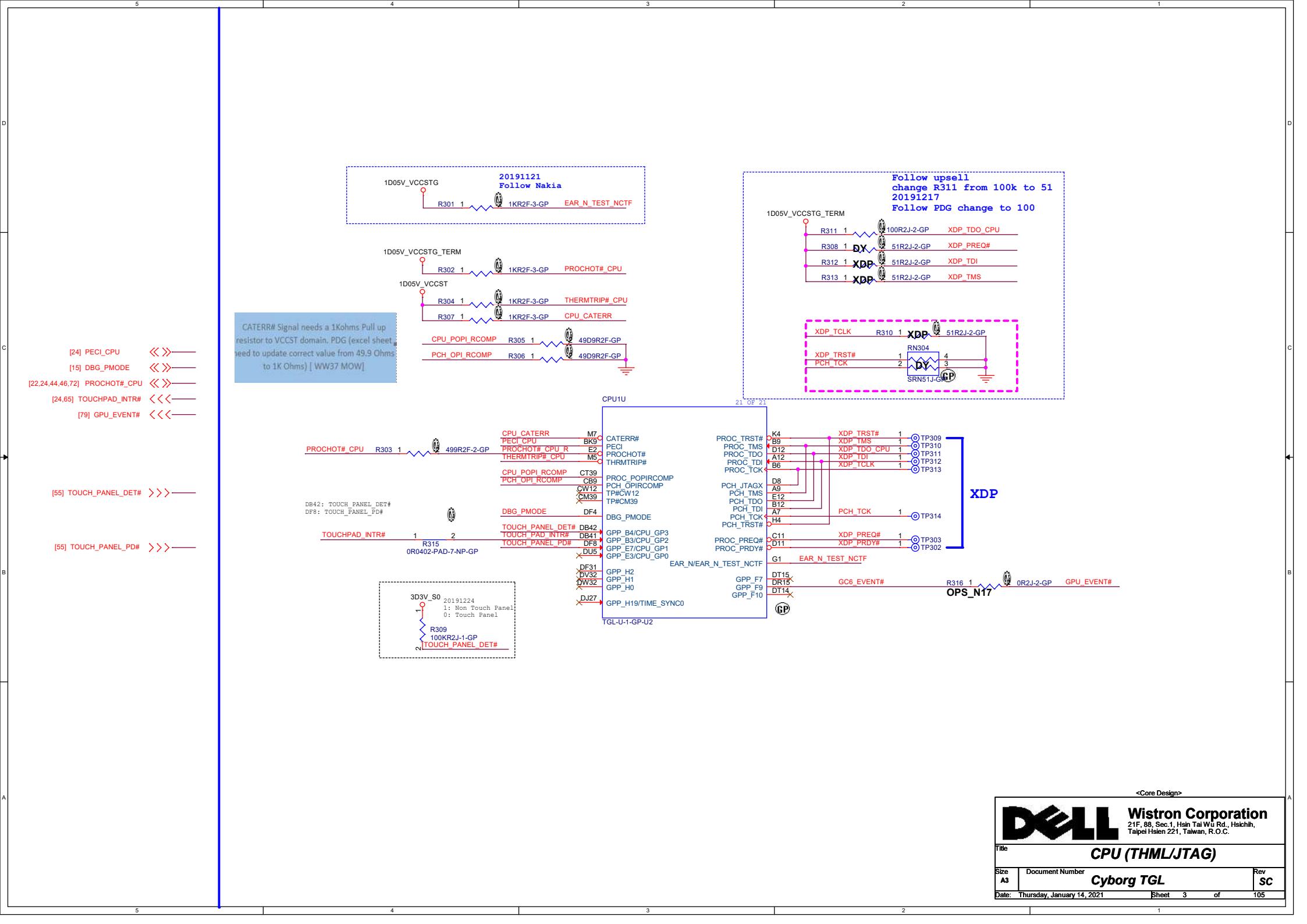
OPS: Optimal Playable Settings

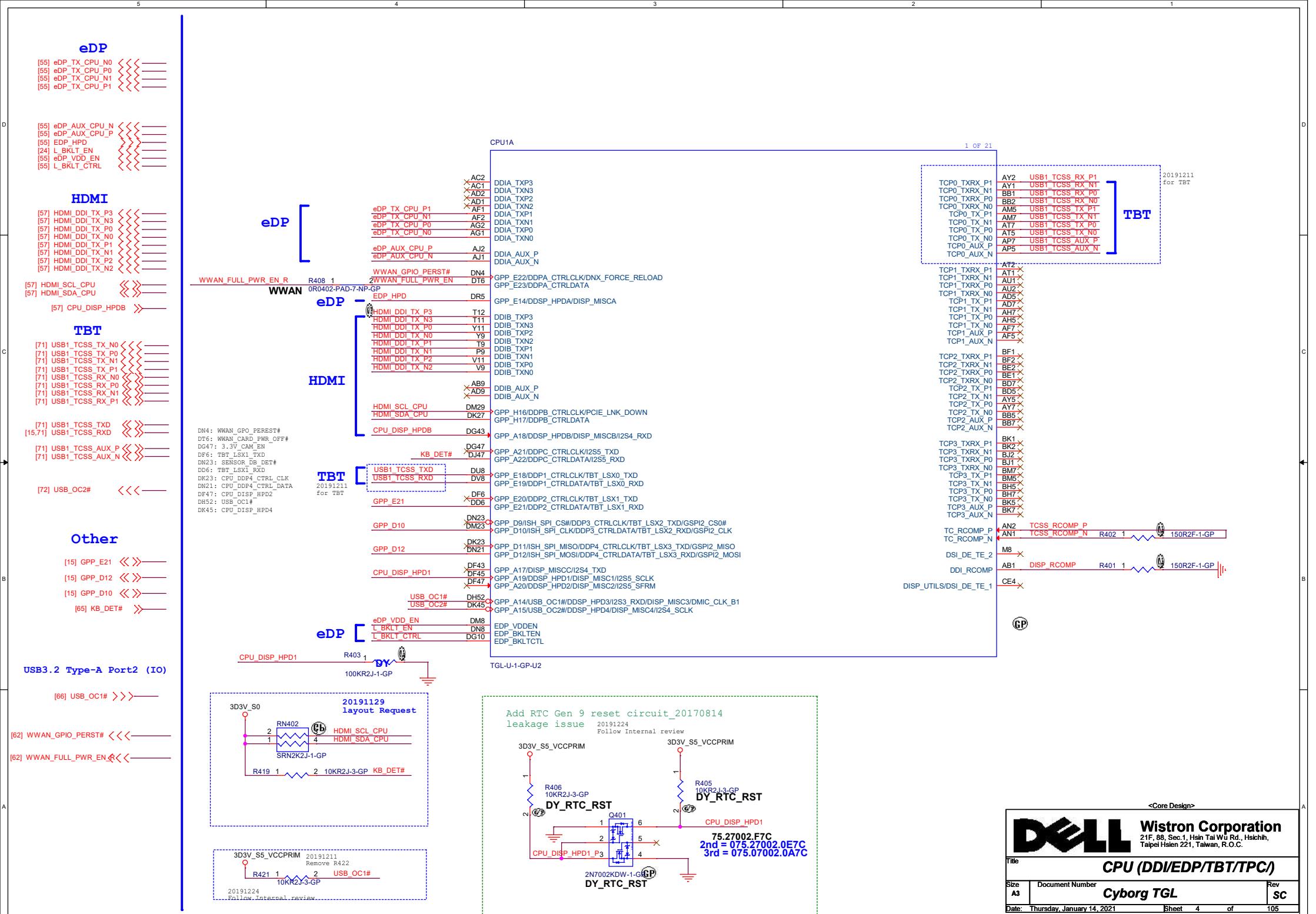
<Core Design>

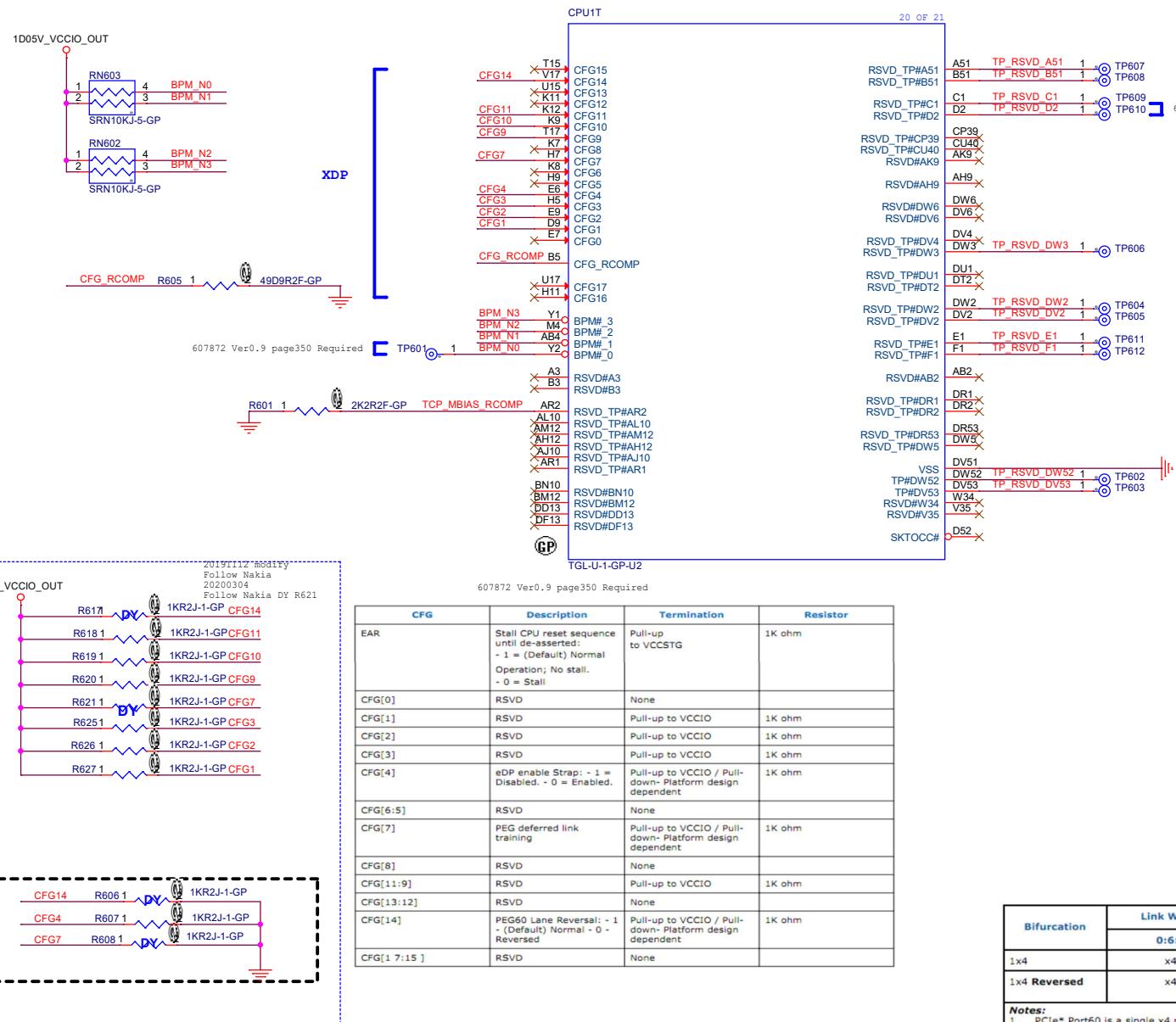
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		Cover Page
Size A4	Document Number	Rev SC
	Cyborg TGL	Date: Thursday, January 14, 2021
	Sheet 1 of 105	

Cyborg N/V/L & Watchmen 14 TGL Block Diagram









CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

Bifurcation	Link Width	CFG Signals	Lanes			
			0	1	2	3
1x4	x4	0	0	1	2	3
1x4 Reversed	x4	1	3	2	1	0

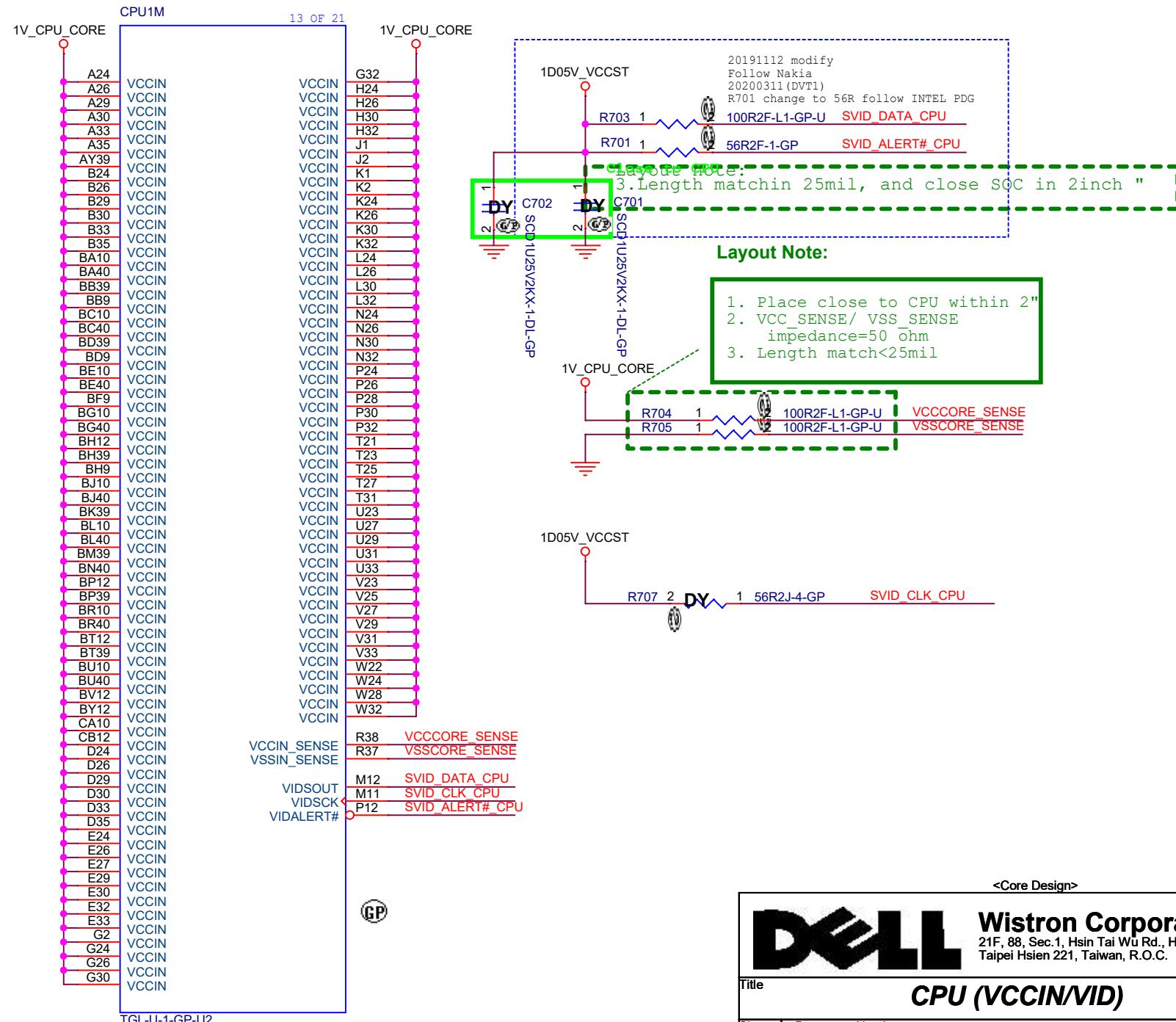
Notes:

- PCIe® Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable.

Notes:

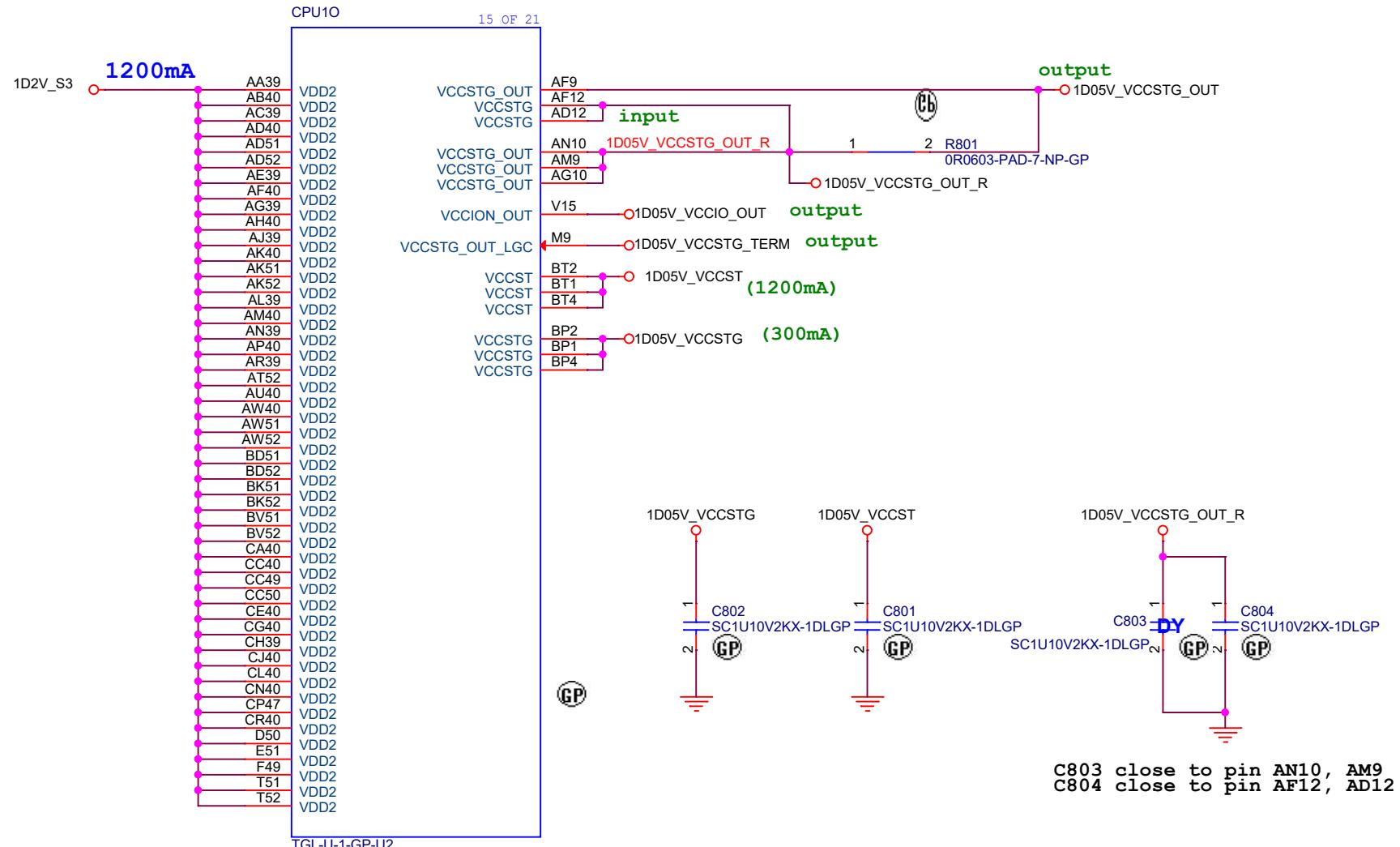
1. PCIe® Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable.

[46] VCCCORE_SENSE <<<—
 [46] VSSCORE_SENSE <<<—
 [46] SVID_ALERT#_CPU <<<—
 [46] SVID_CLK_CPU <<<—
 [46] SVID_DATA_CPU <>>—



<Core Design>

Main Func = CPU

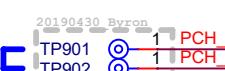


Lack of VCCPLL_OC / VCC1P8A / VCCPLL

<Core Design>

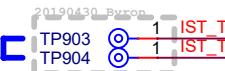
DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (VDDQ/VCC/VCCST/VCCSTG)
Size	Document Number
A4	Cyborg TGL
Rev	SC
Date: Thursday, January 14, 2021	Sheet 8 of 105

607872 Ver0.9 page350 Optional

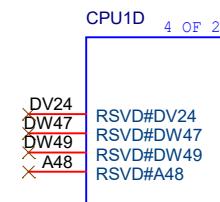
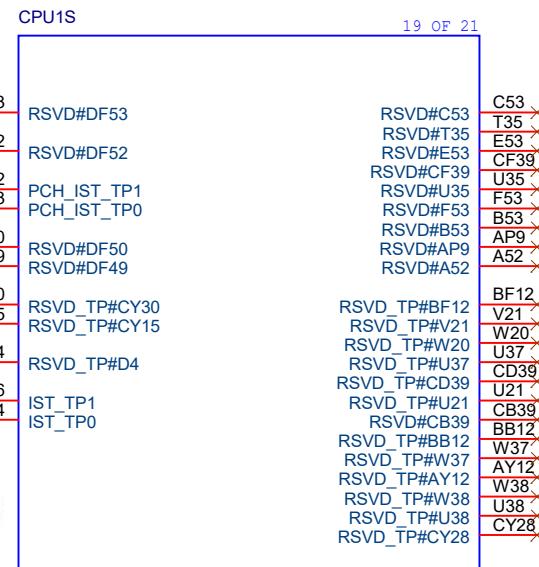


20190430 Byron

607872 Ver0.9 page350 recommend



20190430 Byron



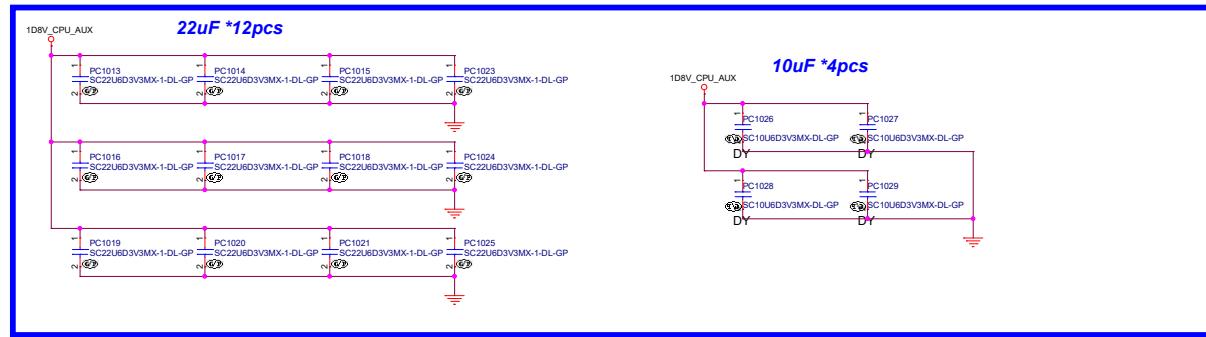
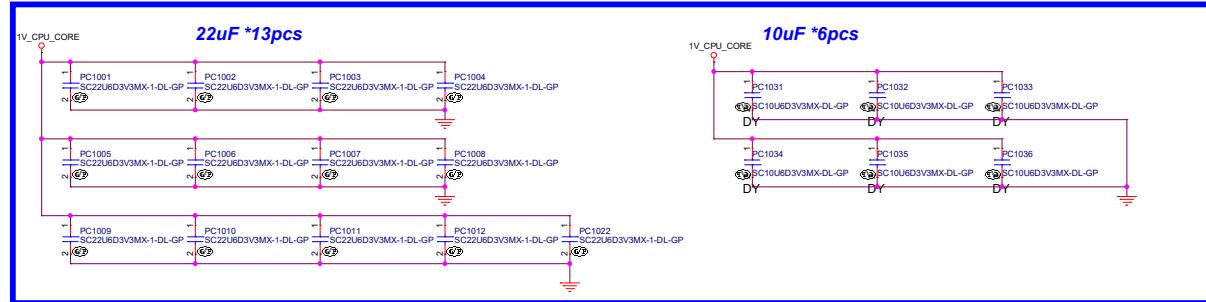
(GP)

<Core Design>

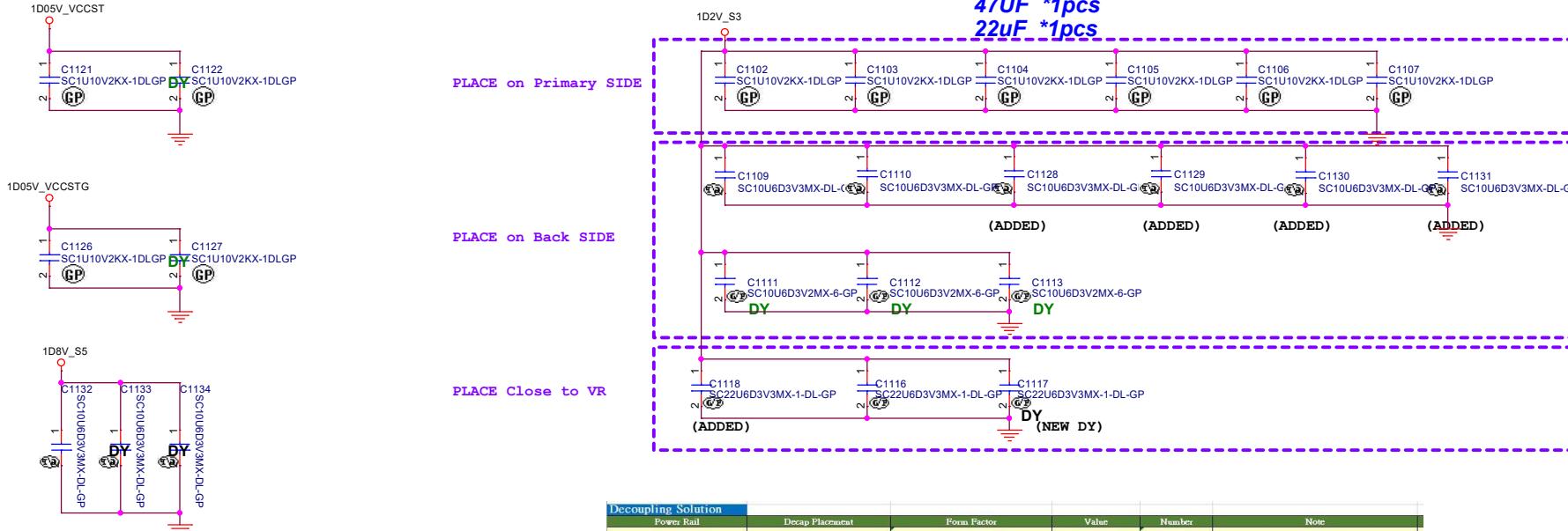


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	
CPU (RSVD)	
Size A4	Document Number
Cyborg TGL	
Rev SC	
Date: Thursday, January 14, 2021	Sheet 9 of 105

Main Func = CPU

Main Func = CPU

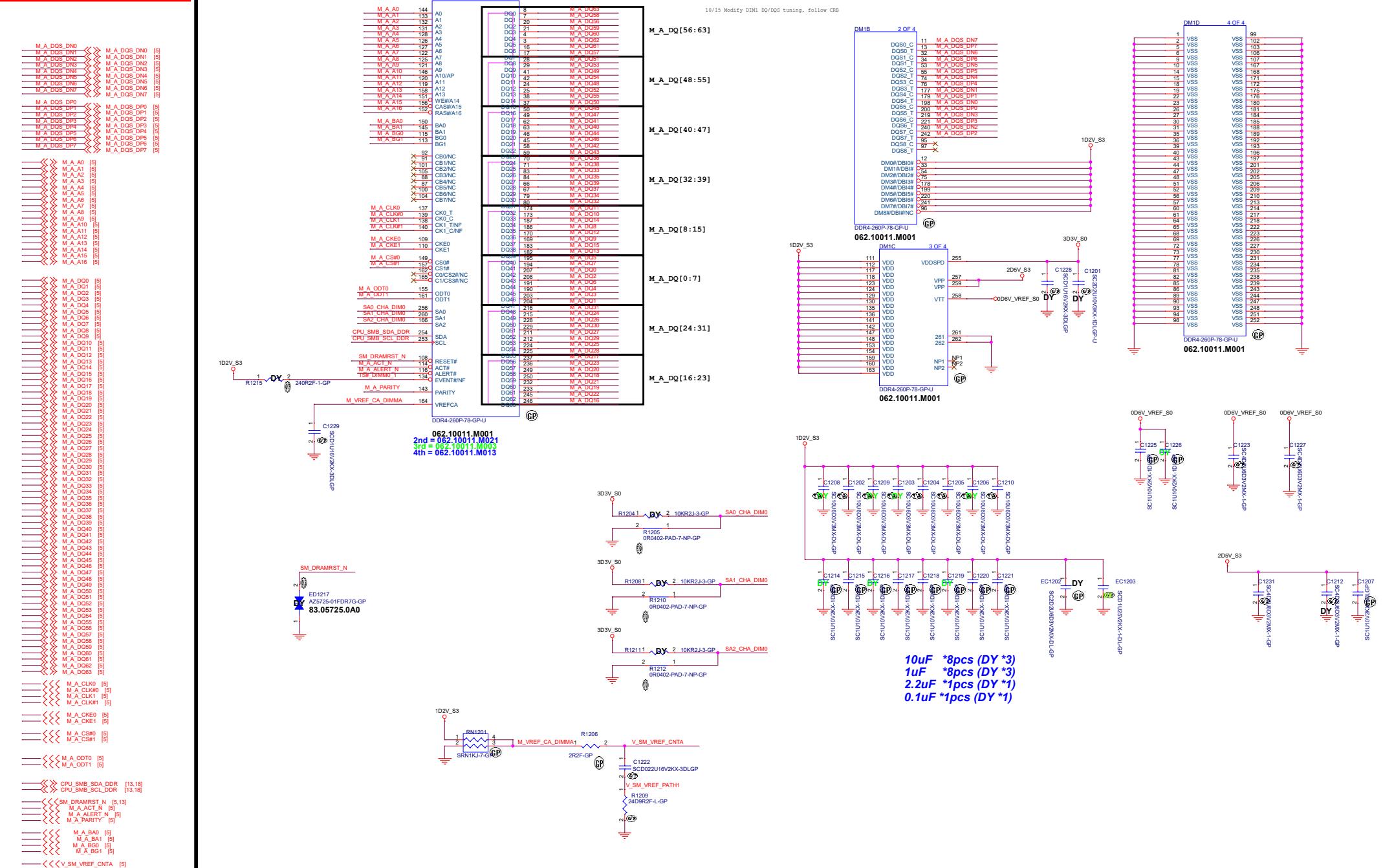


1uF *6pcs
10uF *6pcs
47uF *1pcs
22uF *1pcs

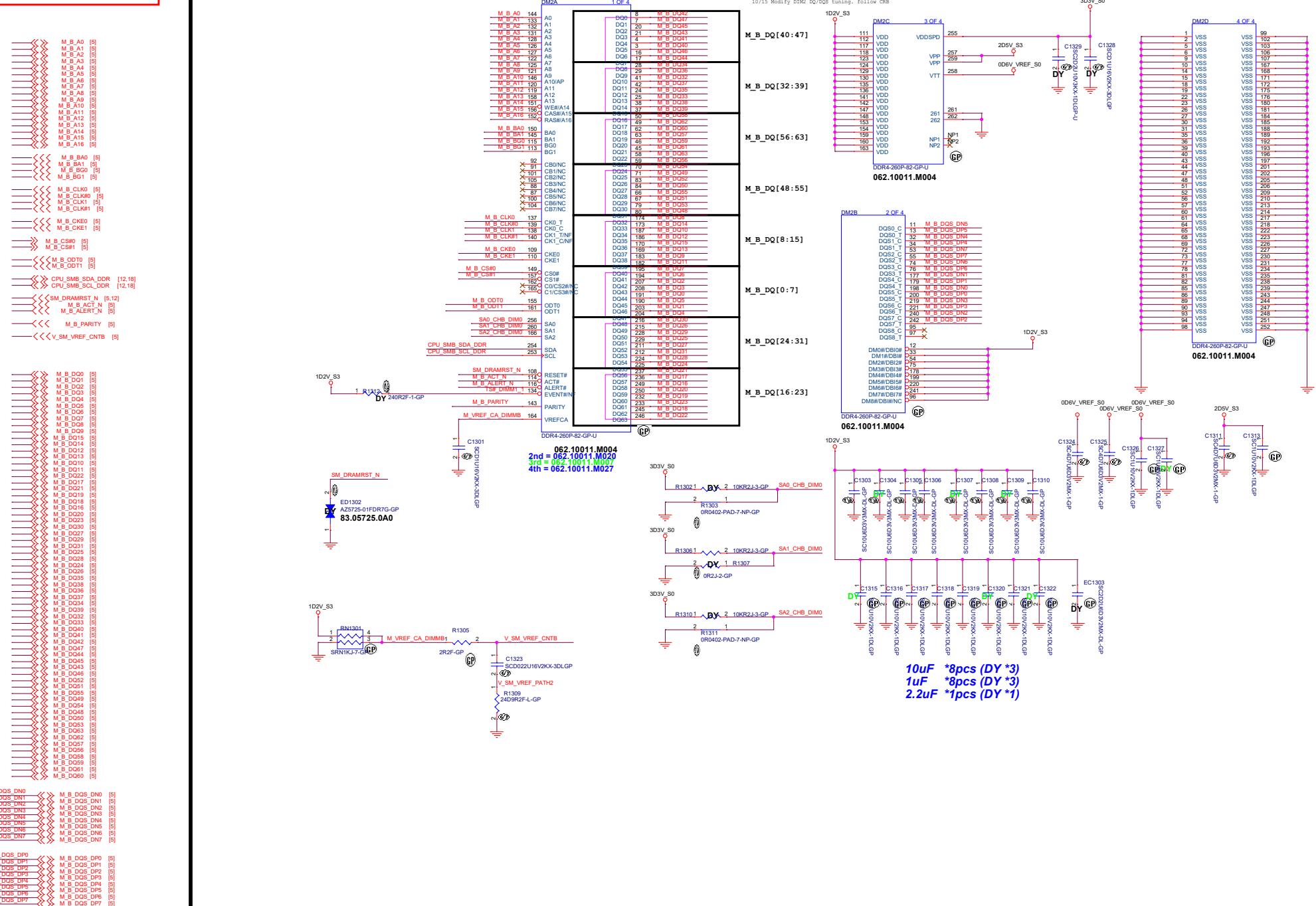
Decoupling Solution					
Power Rail	Decap Placement	Form Factor	Value	Number	Note
VODDD2	Secondary Side	0402	10uF	8	Place on the back side of the SOC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitors such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	Primary Side	0603	47uF	2	Place them as close to the VR as possible. 2 caps should be staggered.
		0402	1uF	8	Place on the primary side, as close as possible to the vias that connect to the outer row of SOC pins. Use wide traces to connect the capacitor pins to the vias. Maximize to put at least 1 via down near the outer Vdd2 BGA and 1 via down near the cap pads.

<Core Design>

Main Func = MEMORY



Main Func = MEMORY



D

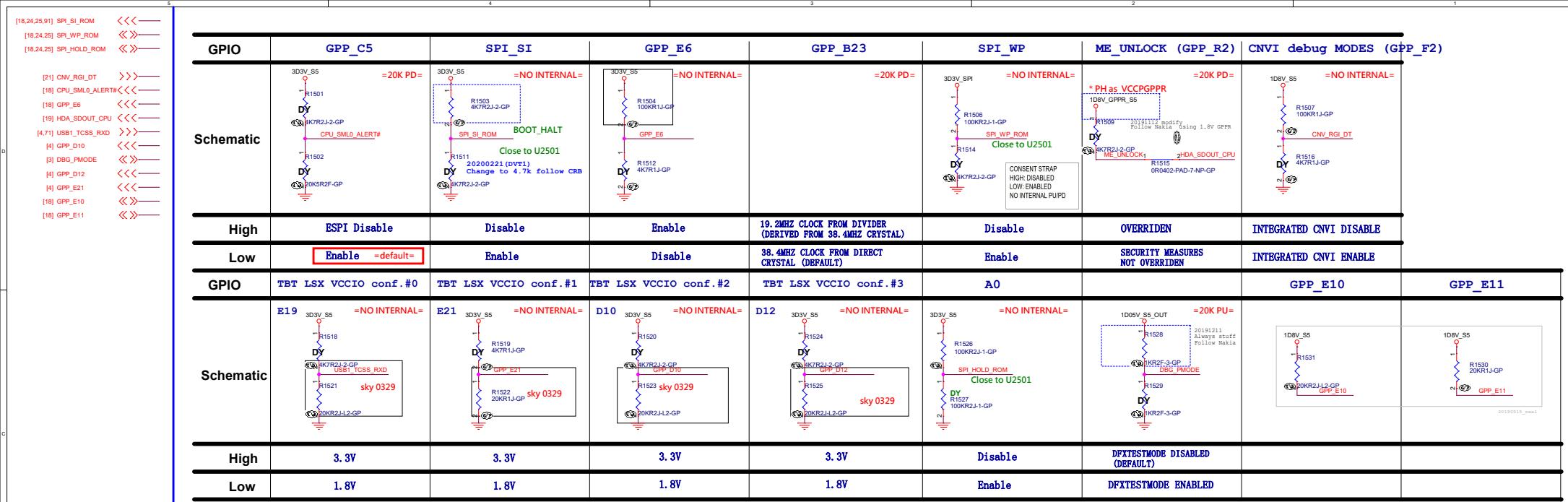
C

B

A

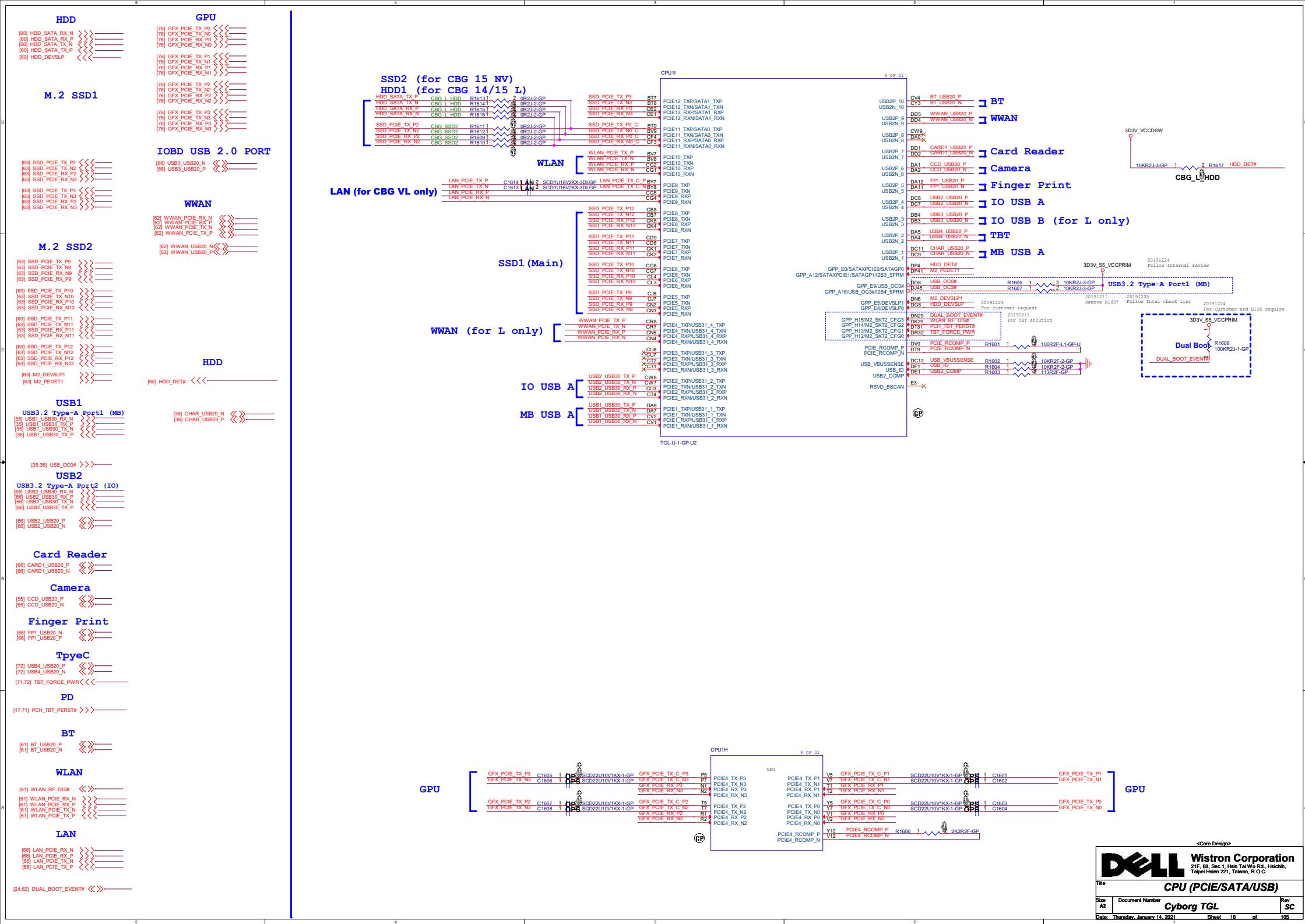
<Core Design>

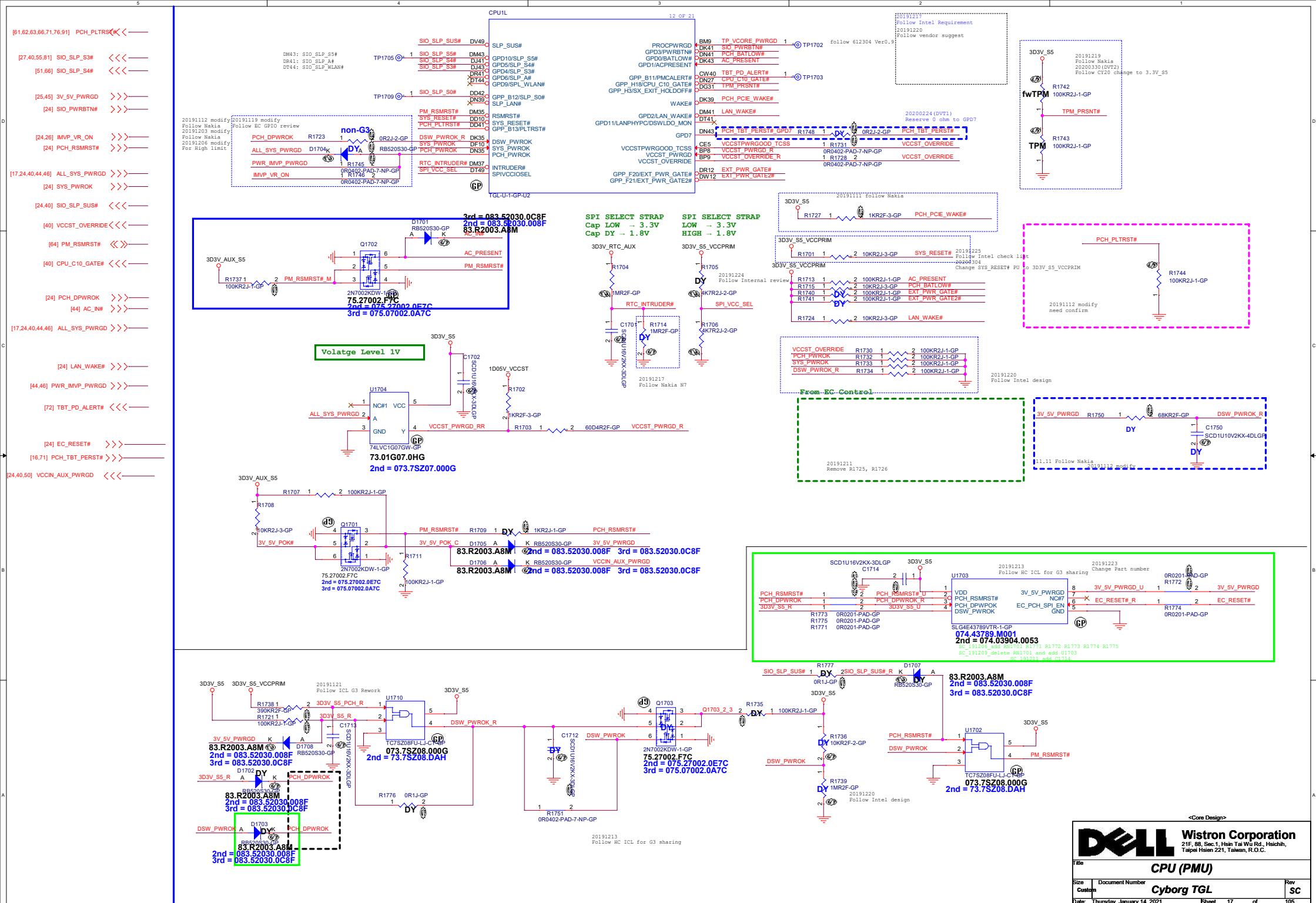
 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DDR (RSVD) (DDR4-CHA1)	
Size A4	Document Number Cyborg TGL
Rev SC	
Date: Thursday, January 14, 2021 Sheet 14 of 105	

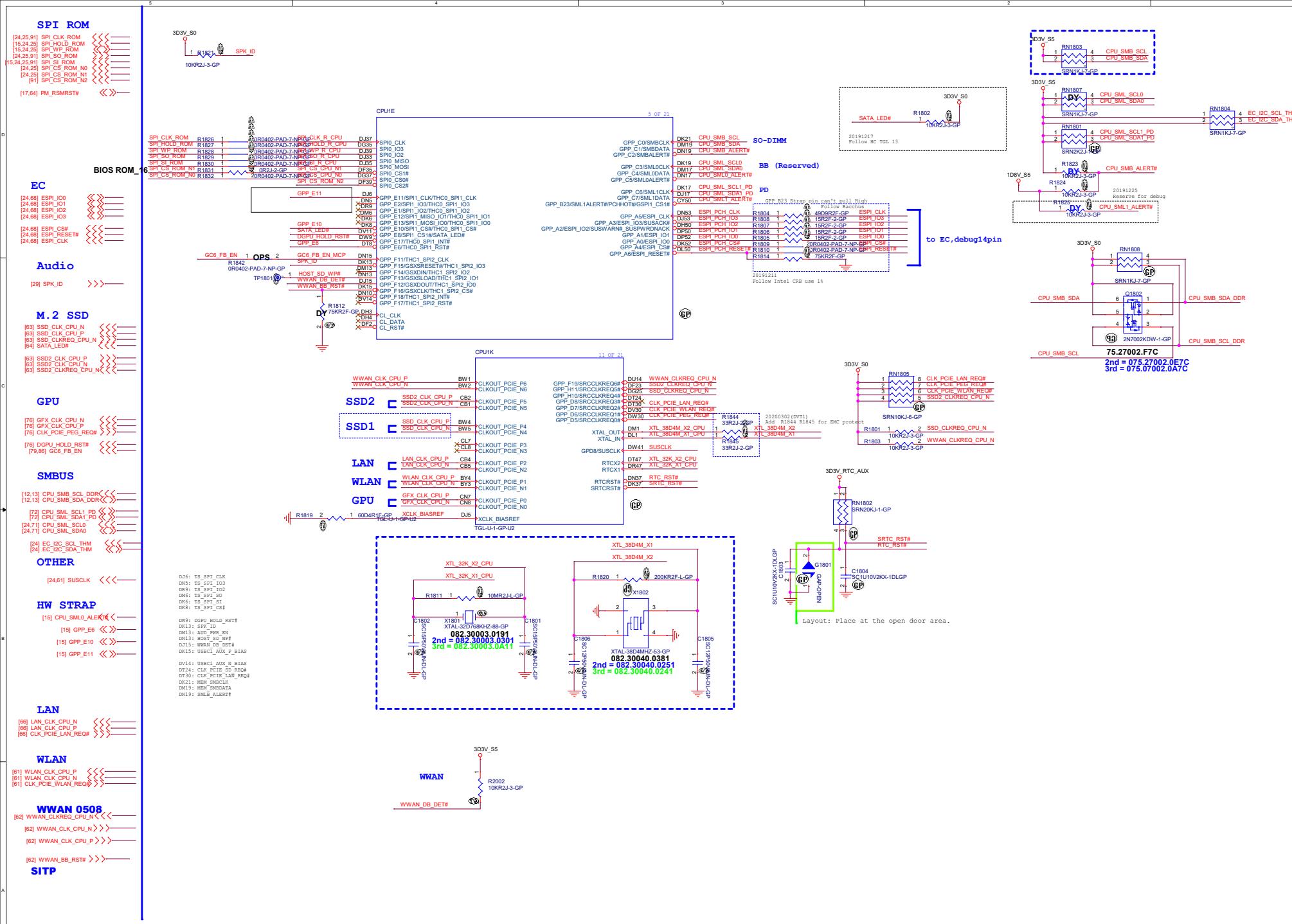


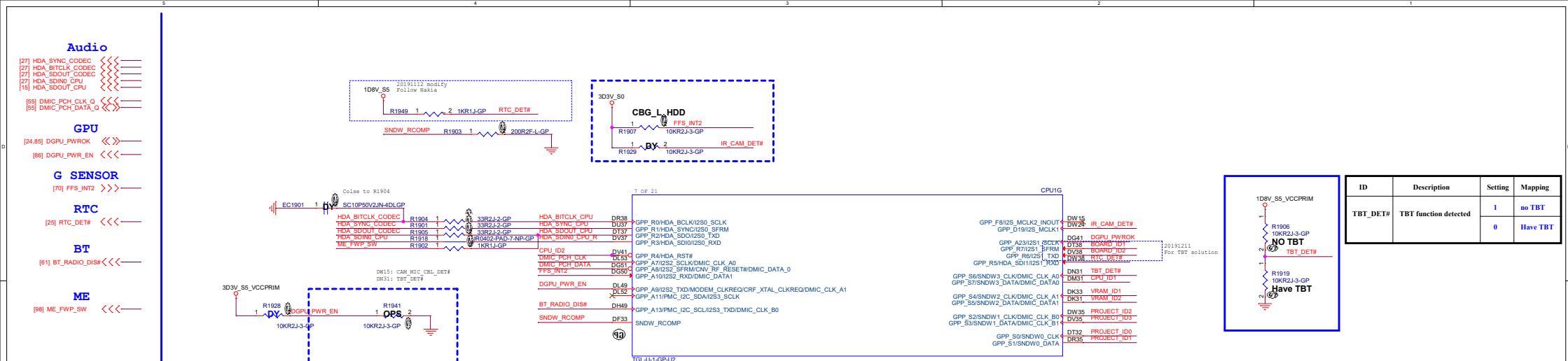
Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD	JTAG QOT DISABLE HIGH: JTAG QOT DISABLED LOW: JTAG QOT ENABLED NO INTERNAL PUPD	CPU/NVIC CLOCK FREE HIGH: 19.2MHz CLOCK FROM DIVIDER (DERIVED FROM 38.4MHz CRYSTAL) LOW: 38.4MHz CLOCK FROM DIRECT CRYSTAL USE AND WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDDEN LOW: SECURITY MEASURES NOT OVERRIDDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW> INTEGRATED CNVI ENABLE HIGH> INTEGRATED CNVI DISABLE NO INTERNAL PUPD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD
TBT LSX #1	TBT LSX #2	TBT LSX #3	A0	GPP_E10	GPP_E11		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD				





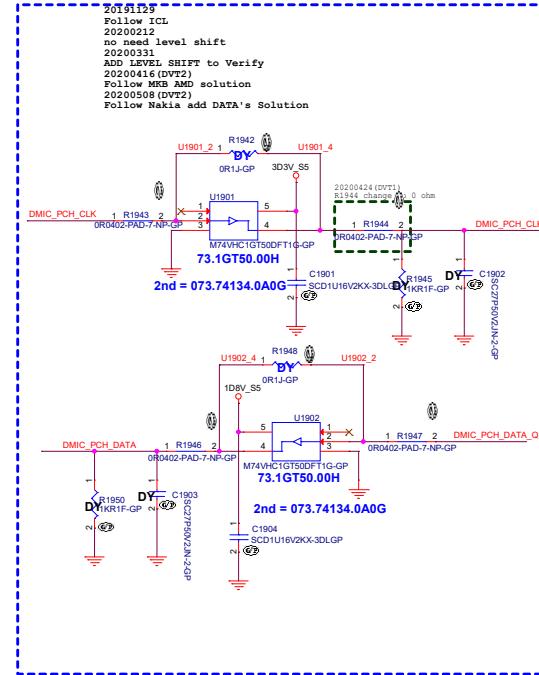




ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	no TBT
		0	Have TBT

For SITH

[55] IR_CAM_DET#>>>



The diagram illustrates the Project entities and their associations:

- Project ID [3:2]** (represented by a blue box):
 - Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> PROJECT_ID [3:2]
 - 1D8V_SS_VCCPRIM (1:0) -> PROJECT_ID [1:0]
 - 1D8V_SS_VCCPRIM (1:0) -> CBG_L / CBG_NV / WM_N (1:0)
- Project Type** (represented by a green box):
 - Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> Project Type (1:1)
- Project Series** (represented by a red box):
 - Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> Project Series (1:1)

Project ID [1:0] (represented by a yellow box):

- Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> Project ID [1:0] (1:0)
 - 1D8V_SS_VCCPRIM (1:0) -> CBG_L / CBG_NV / WM_N (1:0)

CBG L / CBG NV / WM N (represented by a purple box):

- Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> CBG L / CBG NV / WM N (1:0)
 - 1D8V_SS_VCCPRIM (1:0) -> CBG_NV / WM_N (1:0)

Inspiron/Vostro (represented by a grey box):

- Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> Inspiron/Vostro (1:0)
 - Inspiron/Vostro (1:0) -> PROJECT_ID_03 (1:0)
 - Inspiron/Vostro (1:0) -> Latitude (1:0)

Vostro (represented by a grey box):

- Associations:
 - Inspiron/Vostro (1:0) -> Vostro (1:0)
 - Vostro (1:0) -> PROJECT_ID_02 (1:0)

Latitude (represented by a grey box):

- Associations:
 - Inspiron/Vostro (1:0) -> Latitude (1:0)
 - Latitude (1:0) -> PROJECT_ID_01 (1:0)

CBG L (represented by a grey box):

- Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> CBG L (1:0)

CBG NV / WM N (represented by a grey box):

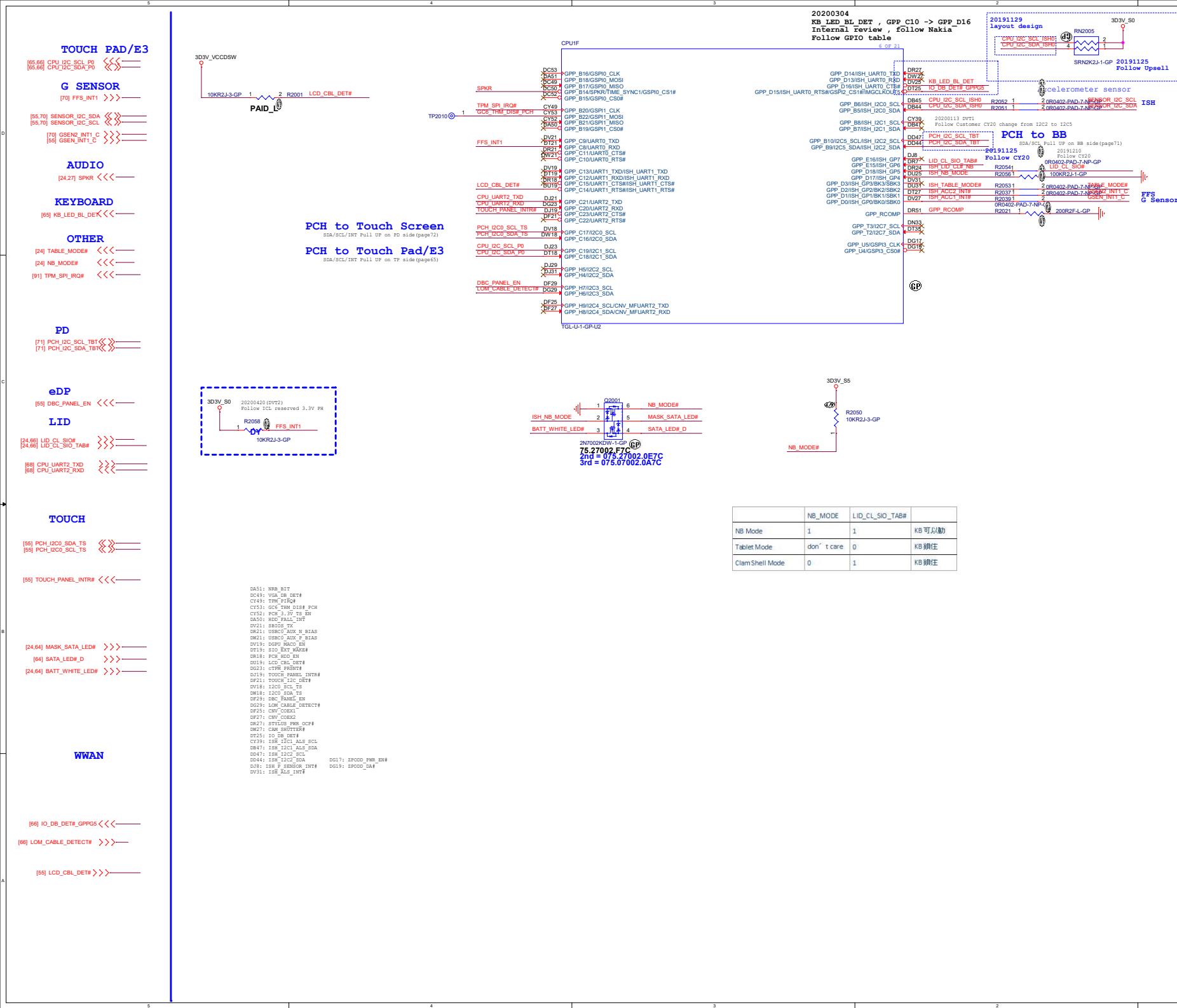
- Associations:
 - 1D8V_SS_VCCPRIM (1:0) -> CBG_NV / WM_N (1:0)

PROJECT_ID_03, **PROJECT_ID_02**, **PROJECT_ID_01**, and **PROJECT_ID_00** are represented by red boxes.

ID	Description	Setting	Mapping	ID	Description	Setting	Mapping
R1908 OPS_N18 ④ 10KR1J-GP ④ BOARD_ID2 R1911 OPS_N17 ④ 10KR1J-GP 	BOARD_ID2	GPU type detected	1 N18S	BOARD_ID1	NVL Size detected	1 14 in	BOARD_ID1
			0 N17S				0 15 in

CY19 VRAM ID Mapping table			
ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

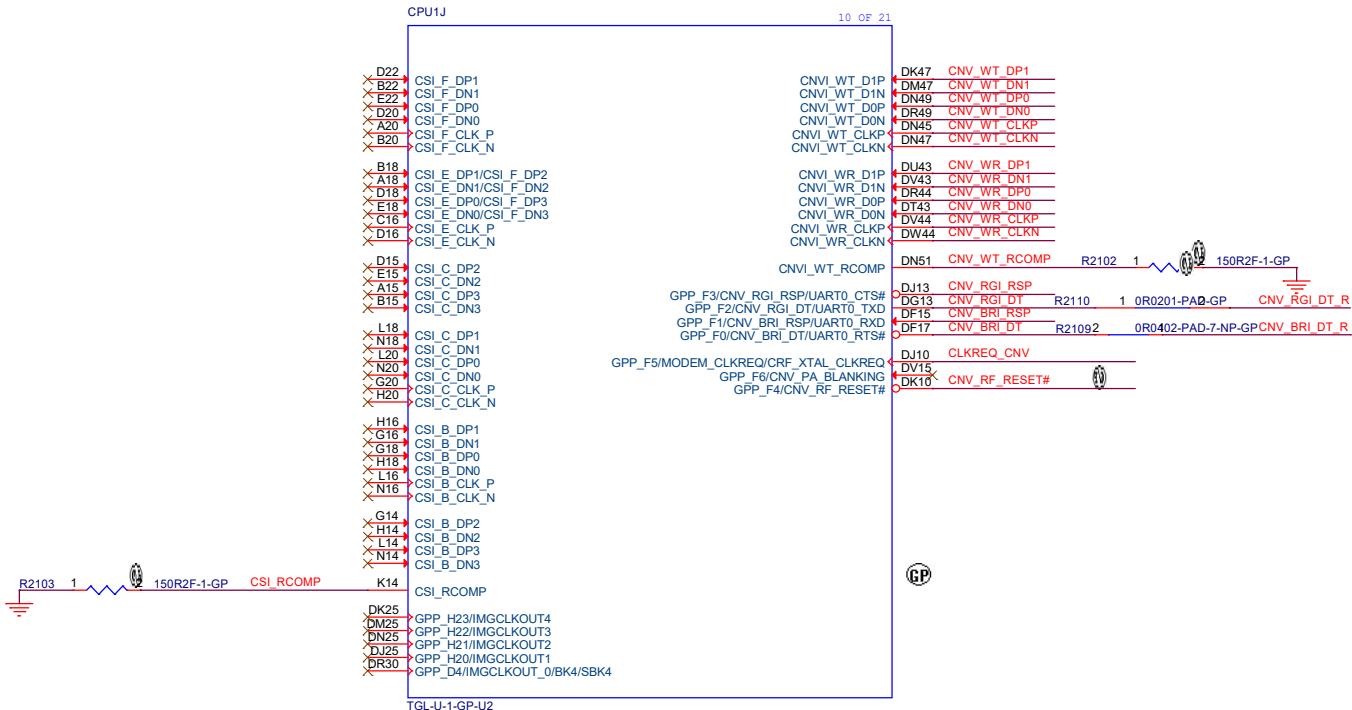
CY19 CPU ID Mapping table			
ID	Description	Setting	Mapping
CPU_ID[2:1]	CPU type Select	11	TGL-H35 Re-flash
		10	TGL-H35
		01	TGL-UP3 Re-flash
		00	TGL-UP3



Main Func = PCH

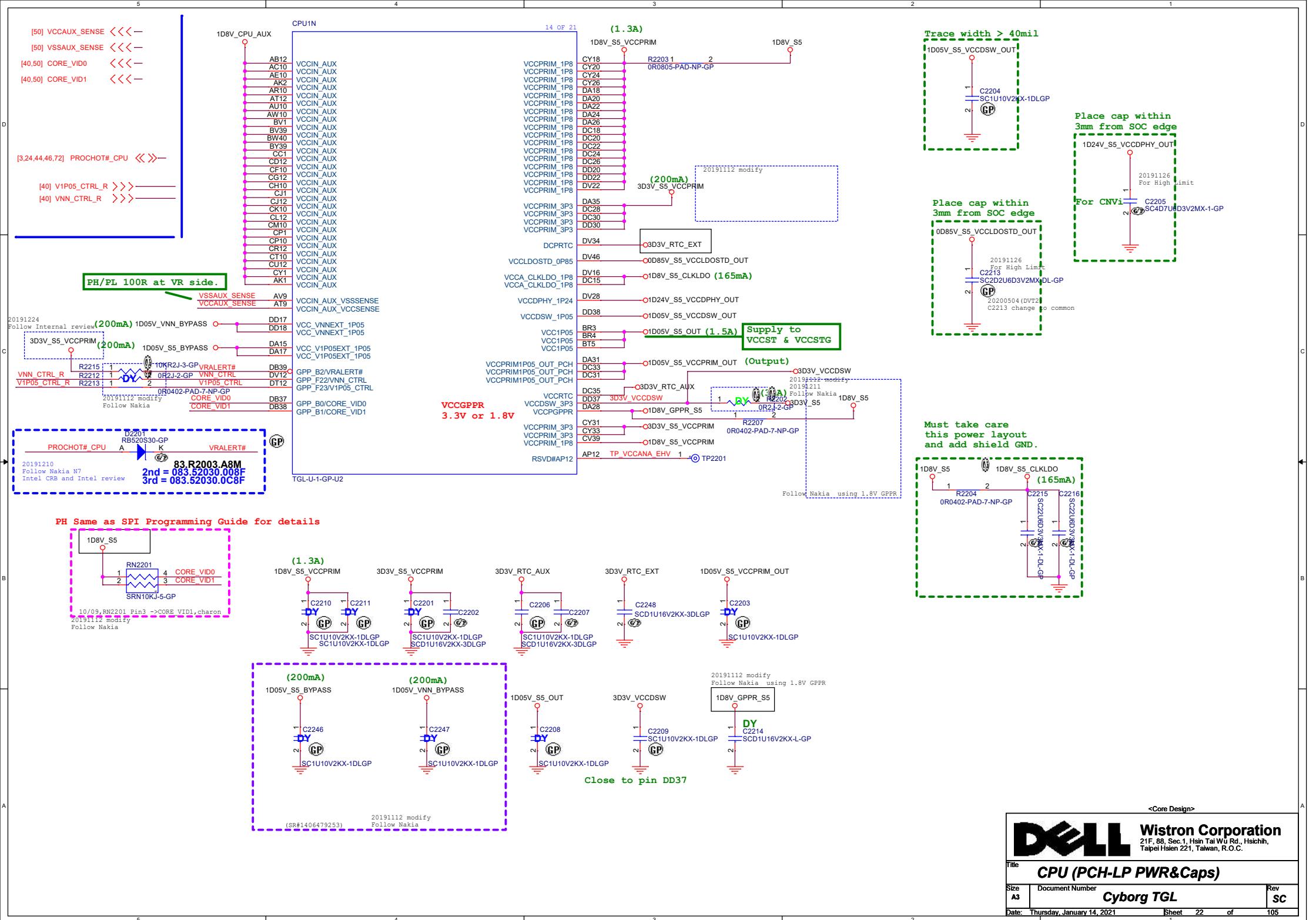
[61] CNV_WR_DN0
 [61] CNV_WR_DP0
 [61] CNV_WR_DN1
 [61] CNV_WR_DP1
 [61] CNV_WR_CLKP
 [61] CNV_WR_CLKN
 [61] CNV_WT_DN0
 [61] CNV_WT_DP0
 [61] CNV_WT_DN1
 [61] CNV_WT_DP1
 [61] CNV_WT_CLKP
 [61] CNV_WT_CLKN
 [61] CNV_BRI_RSP
 [15] CNV_RGI_DT
 [61] CNV_RGI_DT_R
 [61] CNV_BRI_DT_R
 [61] CNV_RGI_RSP

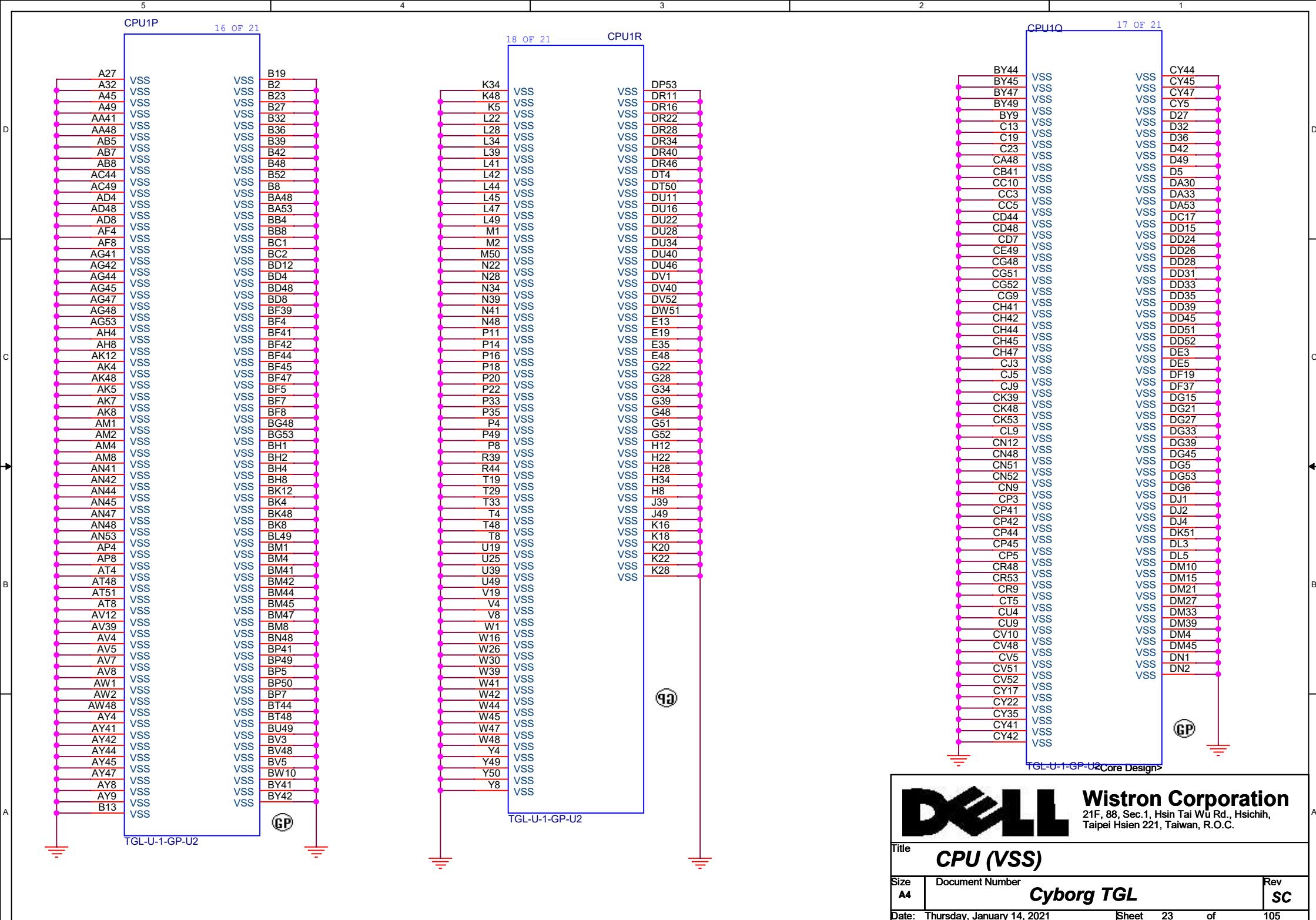
[61] CNV_RF_RESET# <<<
 [61] CLKREQ_CNV <<<

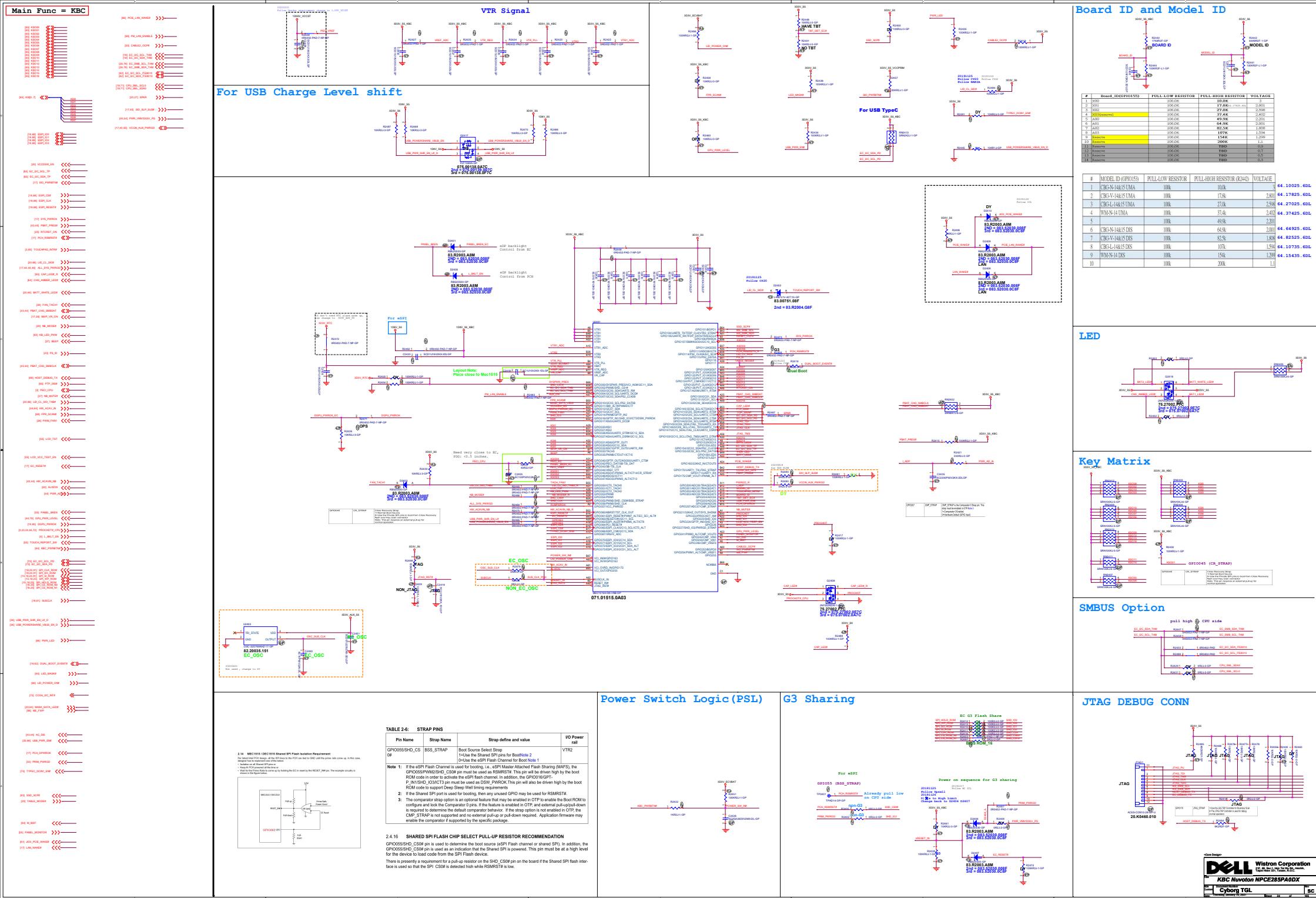


<Core Design>

DELL		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<Core Design>		
Title		
Size A3	Document Number	Rev SC
Cyborg TGL		
Date: Thursday, January 14, 2021	Sheet 21	of 105

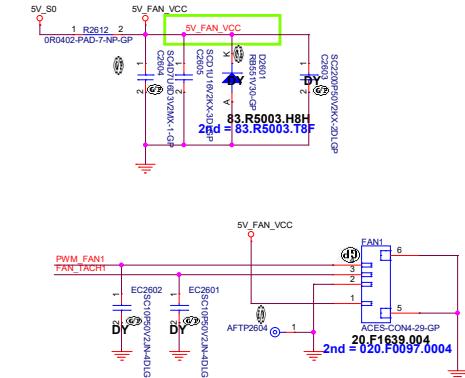






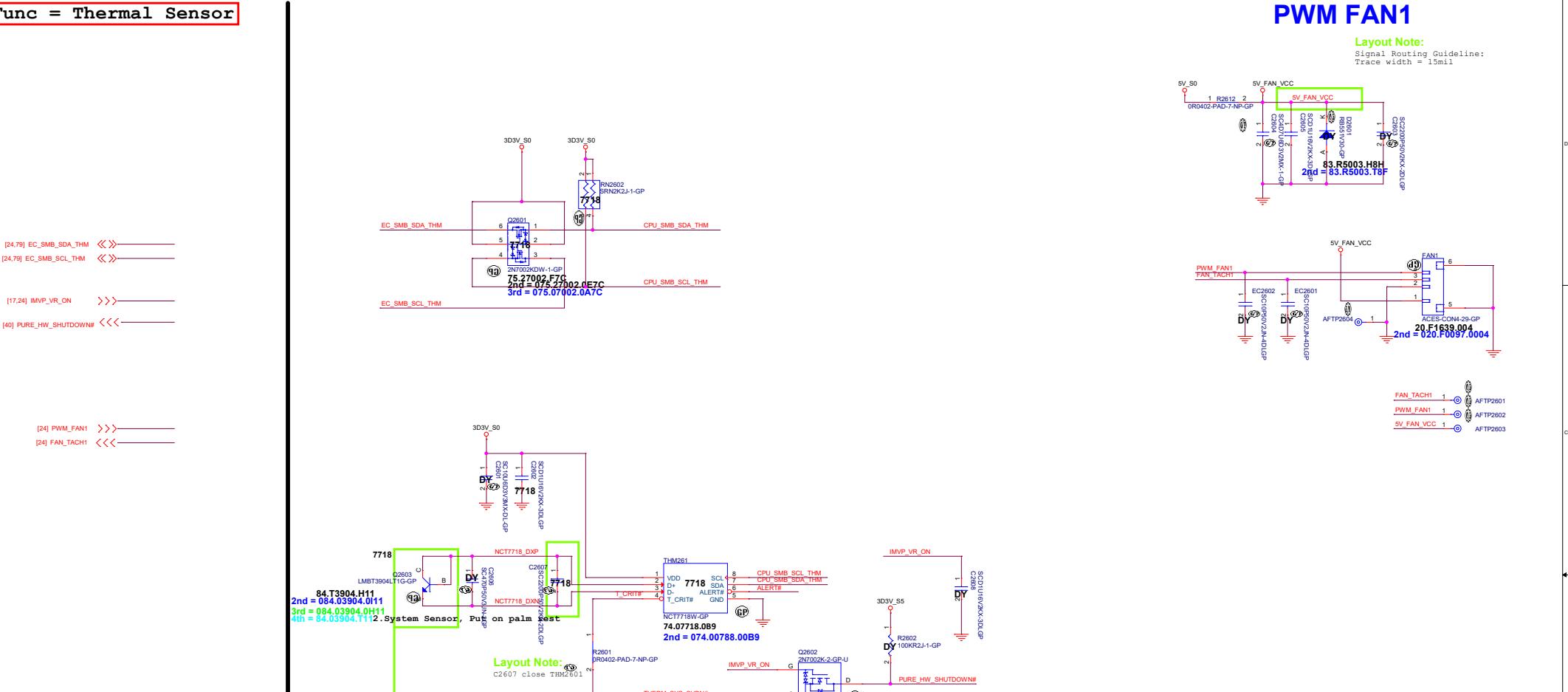
PWM FAN1

Layout Note:
Signal Routing Guideline:
Trace width = 15mil



FAN_TACH1 1 AFTP2601
PWM_FAN1 1 AFTP2602
5V_FAN_VCC 1 AFTP2603

Main Func = Thermal Sensor



Layout Note:

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
2KΩ	77	87	97	107	117
7.5KΩ	79	89	99	109	119
10.5KΩ	81	91	101	111	121
14KΩ	83	93	103	113	123
18.7KΩ	85	95	105	115	125

<Core Design>

Main Func = Audio

[19] HDA_SDIN0_CPU <<<
[19] HDA_SDOUT_CODEC >>>
[19] HDA_SYNC_CODEC >>>
[19] HDA_BITCLK_CODEC >>>

[29] AUD_SPK_R+ <<<
[29] AUD_SPK_R- <<<
[29] AUD_SPK_L+ <<<
[29] AUD_SPK_L- <<<

[24] NB_Muteff >>>
[20,24] SPKR >>>
[24] BEEP >>>
[66] AUD_SENSE >>>

[29] LINE1_VREF0 <<<
[29] MIC2_VREF0 <<<

[29] AUD_HPI_JACK_L <<<
[29] AUD_HPI_JACK_R <<<

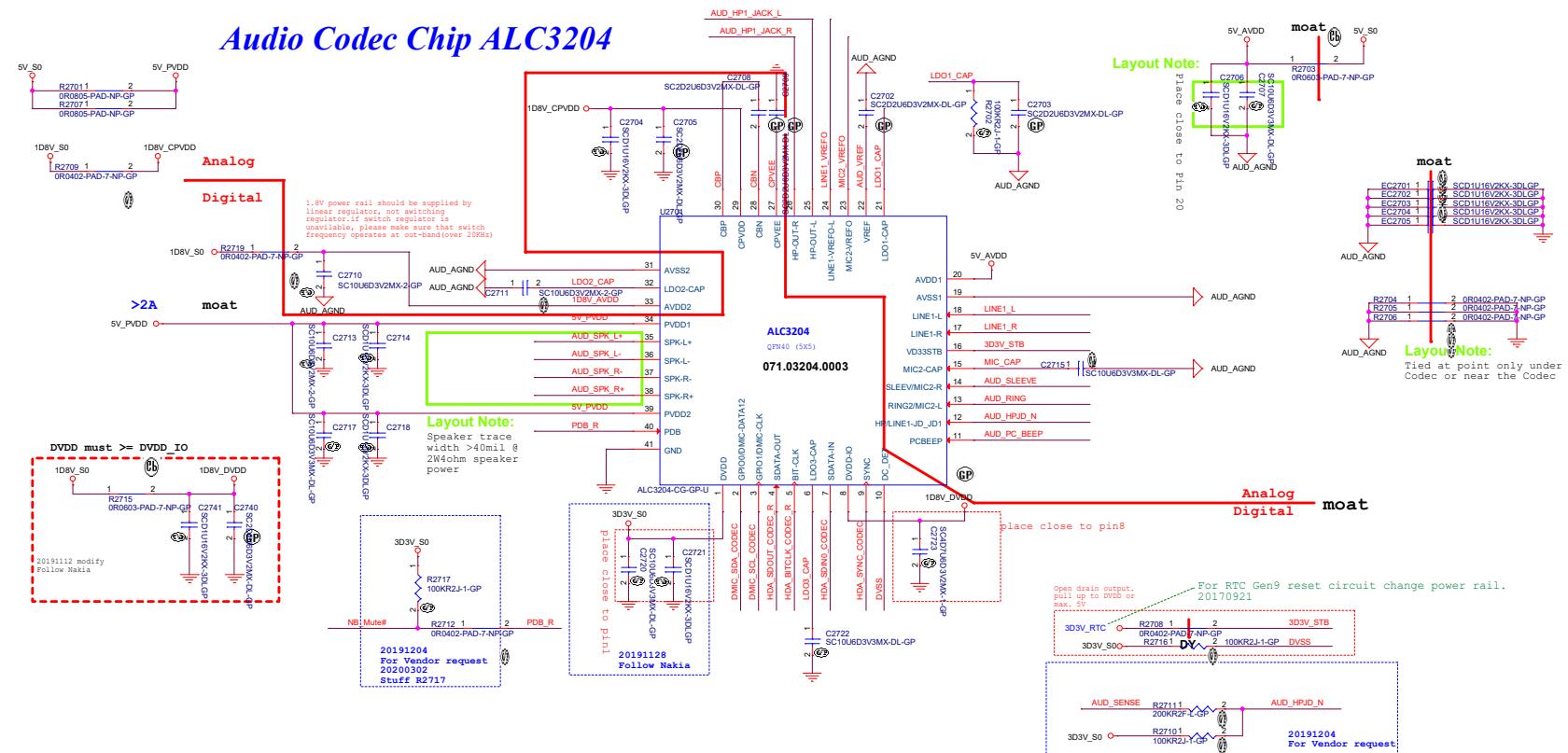
[29] LINE1_L >>>
[29] LINE1_R >>>

[29,66] AUD_SLEEVE <<<
[29,66] AUD_RING <<<

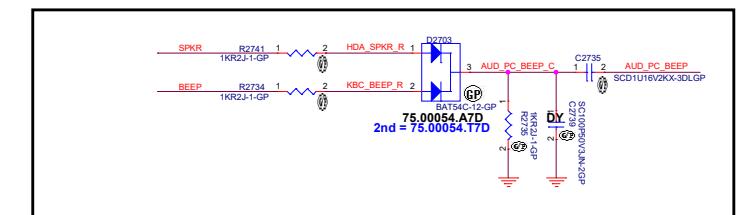
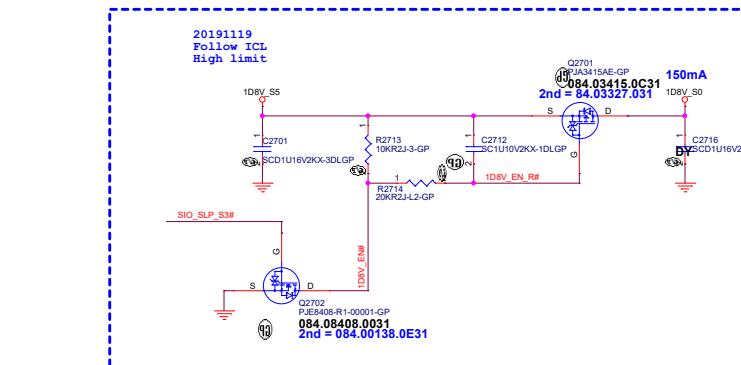
[55] DMC_SCL_CODEC <<<
[55] DMC_SDA_CODEC <<<

[17,40,55,81] SIO_SLP_S3M >>>
[81] 1D8V_EN# >>>

Audio Codec Chip ALC3204



Azalia I/F EMI



(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size
A4

Document Number

Rev
SC

Cyborg TGL

Date: Thursday, January 14, 2021

Sheet 28 of 105

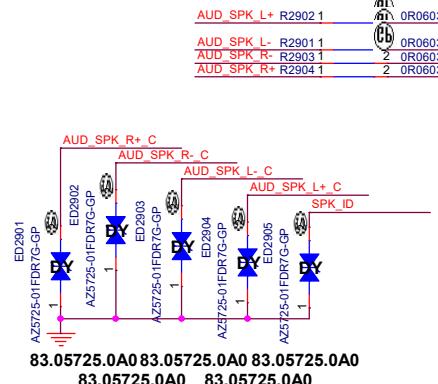
Main Func = Audio

[27] AUD_SPK_R+ >>> _____
 [27] AUD_SPK_R- >>> _____
 [27] AUD_SPK_L- >>> _____
 [27] AUD_SPK_L+ >>> _____

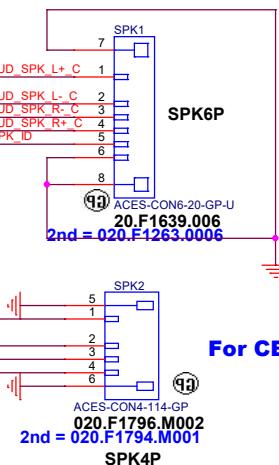
[18] SPK_ID <<< _____

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



Speaker



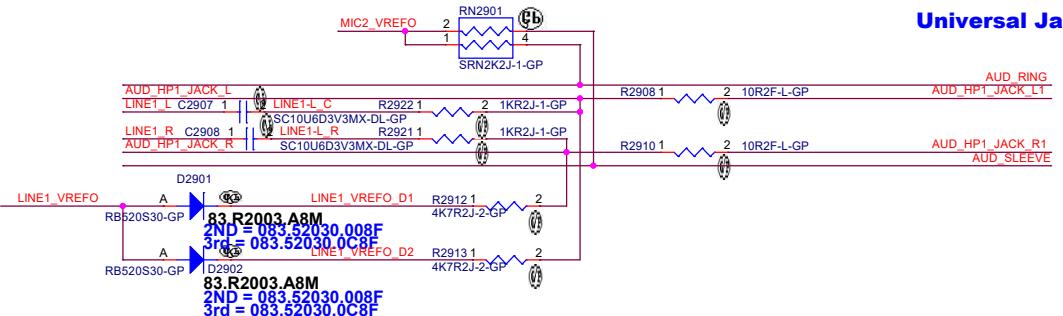
CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: VECO
 0: ZY

AUD_SPK_L- C	1	AFTP2901
AUD_SPK_L+ C	1	AFTP2902
AUD_SPK_R- C	1	AFTP2903
AUD_SPK_R+ C	1	AFTP2904
SPK_ID	1	AFTP2911

From Codec

[27] MIC2_VREFO >>> _____
 [27,29,66] AUD_RING <<< _____
 [27] AUD_HP1_JACK_L >>> _____
 [27] LINE1_L >>> _____
 [27] LINE1_R >>> _____
 [27] AUD_HP1_JACK_R >>> _____
 [27,29,66] AUD_SLEEVE <<< _____
 [27] LINE1_VREFO >>> _____



Universal Jack (Moved to I/O Board)

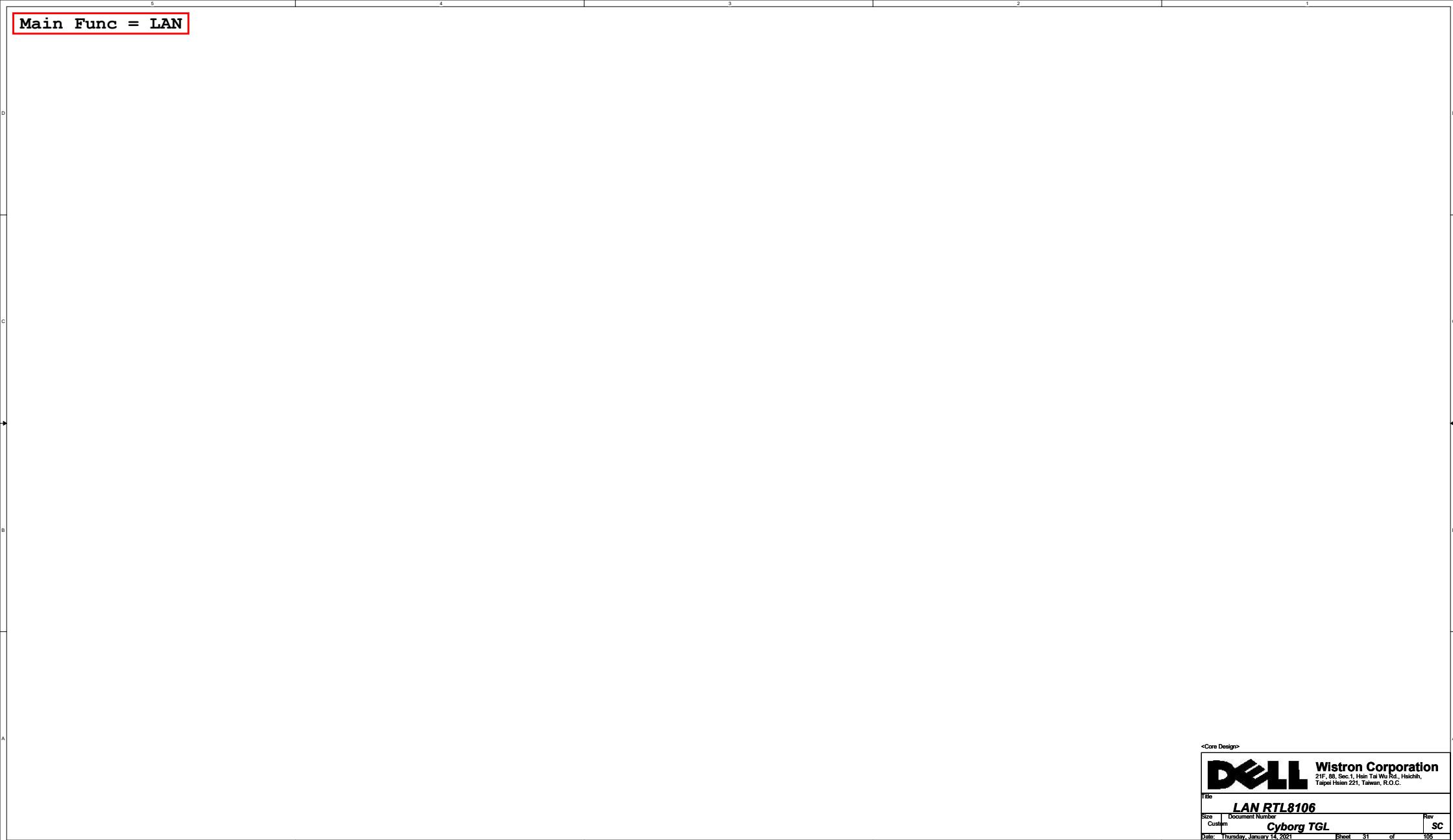
[27,29,66] AUD_RING <<< _____
 [66] AUD_HP1_JACK_L1 <<< _____
 [66] AUD_HP1_JACK_R1 <<< _____
 [27,29,66] AUD_SLEEVE <<< _____

<Core Design>

(Blanking)

<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	(Reserved)
Size A4	Document Number
	Cyborg TGL
Date: Thursday, January 14, 2021	Sheet 30 of 105



Main Func = LAN

D

D

c

C

B

B

A

A

<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	
Size A3	Document Number
	Cyborg TGL
Date: Thursday, January 14, 2021	Rev SC
Sheet 32 of 105	1

Main Func = Card Reader

5

4

3

2

1

D

D

C

C

B

B

A

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5170

Size

Document Number

Rev

A4

Cyborg TGL

SC

Date: Thursday, January 14, 2021

Sheet 33 of 105

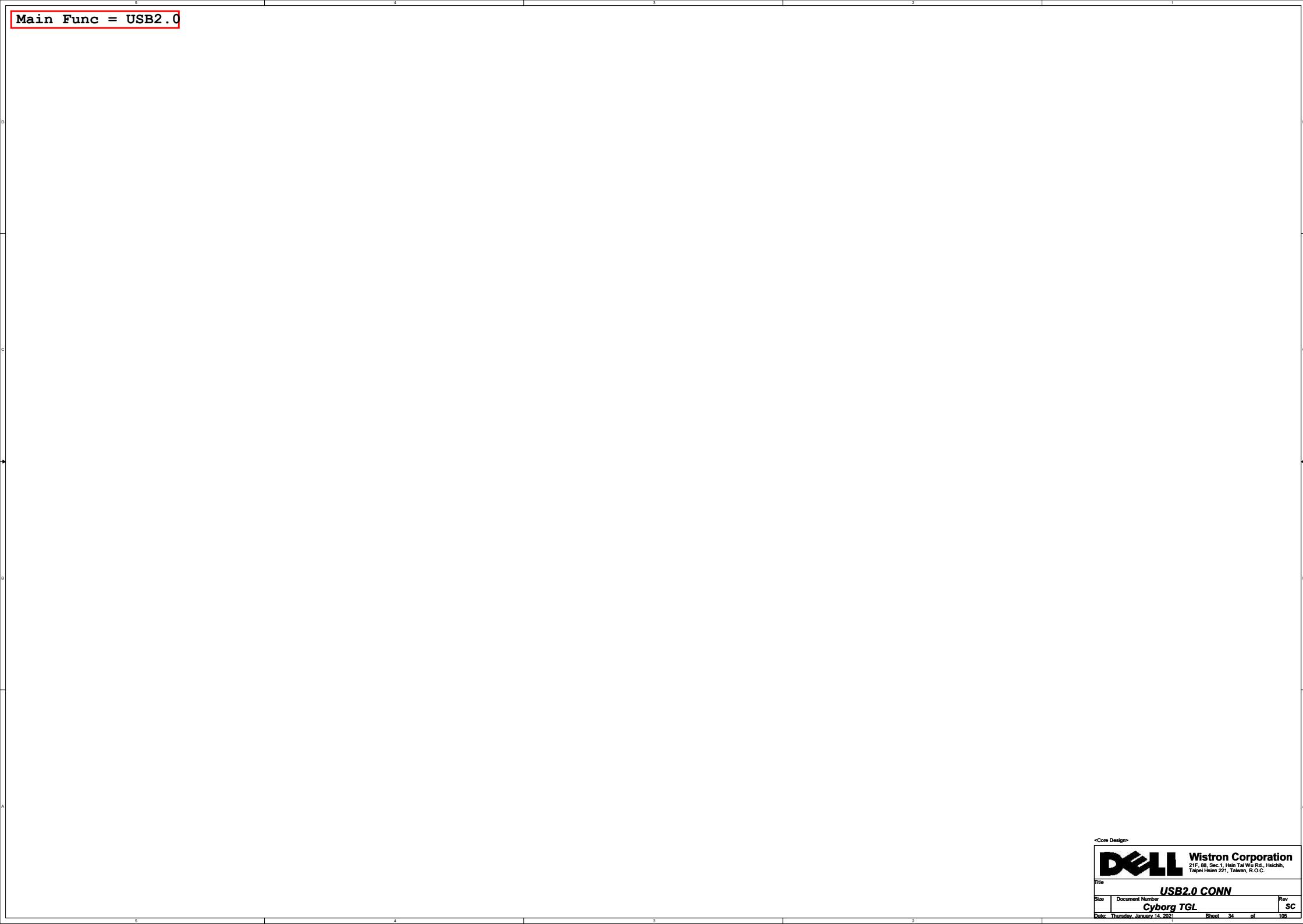
5

4

3

2

1



Main Func = USB3.0 Port1

[2456] USB_PWR_EN# <<<

[1636] USB_DCOM <<<

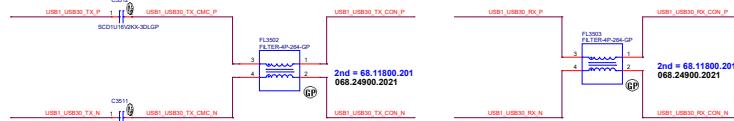
[36] USB1_USB20_N <>>
[36] USB1_USB20_P <>>

[16] USB1_USB30_TX_N
[16] USB1_USB30_RX_P
[16] USB1_USB30_RX_N
[16] USB1_USB30_RX_P <>>

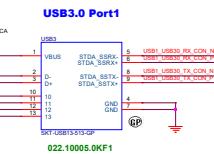


2020/02/29: swap EL3501

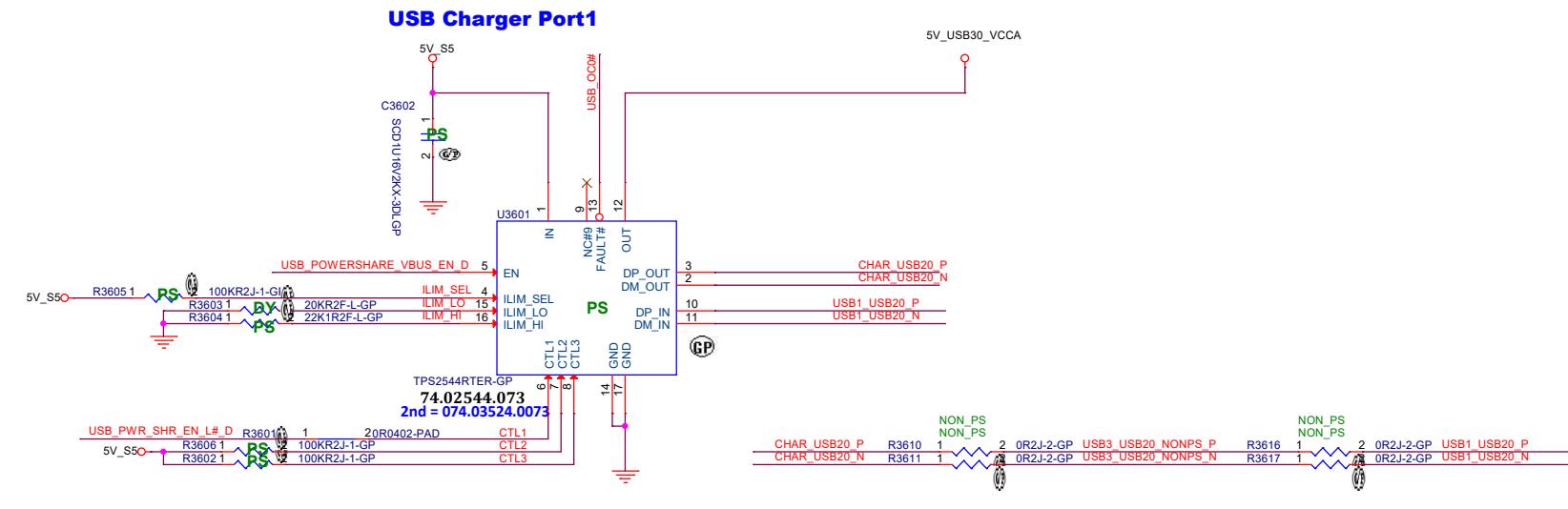
USB1_USB20_N 4 ③ USB1_USB20_CON_N
USB1_USB20_P 1 ④ 2 USB1_USB20_CON_P
DL130050001Y2D-GP
065.0901.2001
2nd = 065.02002.061



USB3.0 Port 1 Layout Note: Close USB3



Main Func = USB Charger



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS_typ} (mA) = \frac{50,500}{(R_{ILIM_XX} (\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		Rev
Size	Document Number	SC
A4	Cyborg TGL	
Date: Thursday, January 14, 2021	Sheet 37 of 105	

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size A4 Document Number

Cyborg TGL

Rev SC

Date: Thursday, January 14, 2021

Sheet 38 of 105

D

D

C

C

B

B

A

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

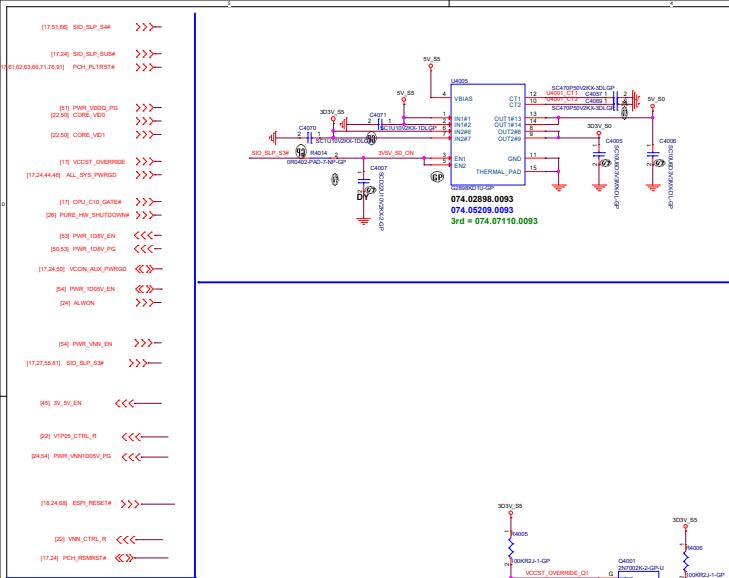
(RSVD)Size
A4

Document Number

Rev
SC**Cyborg TGL**

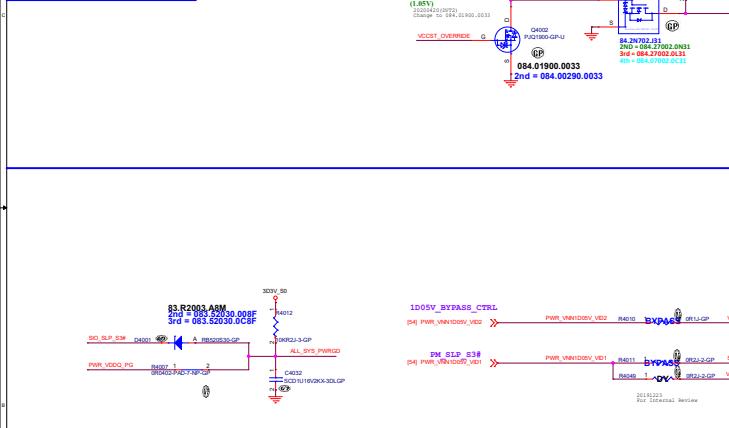
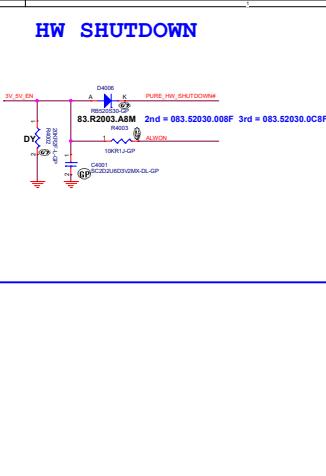
Date: Thursday, January 14, 2021

Sheet 39 of 105

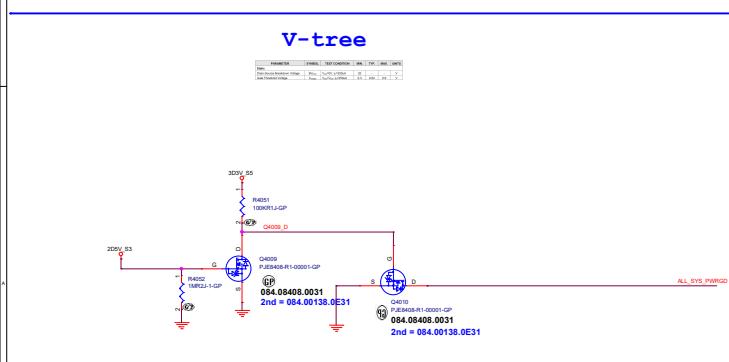


RUN Power

20200815
Remove



Power Sequence / Pull High PWRGD



20200807
Remove

D

D

C

C

B

B

A

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Connected_Standby(1/2)+DS3

Size

Document Number

Rev

A4

Cyborg TGL

SC

Date: Thursday, January 14, 2021

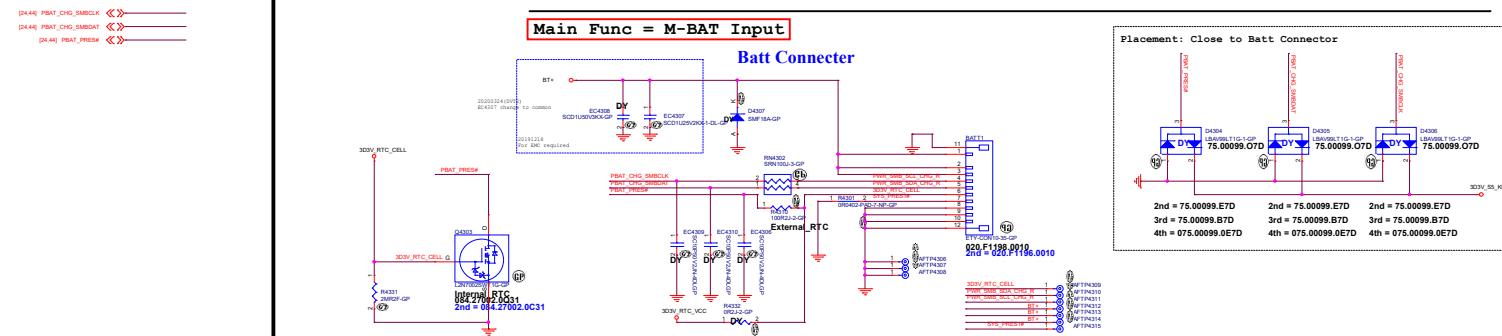
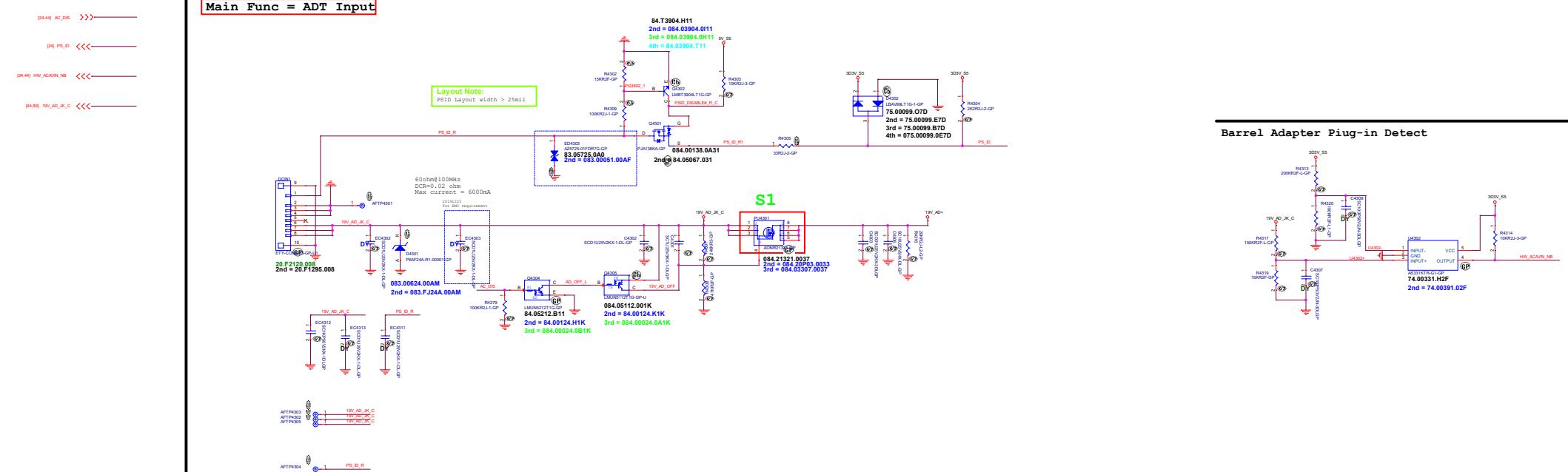
Sheet 41 of 105

(Blanking)

<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	<i>Connected_Standby(2/2)</i>
Size A4	Document Number
	Cyborg TGL

Date: Thursday, January 14, 2021 Sheet 42 of 105

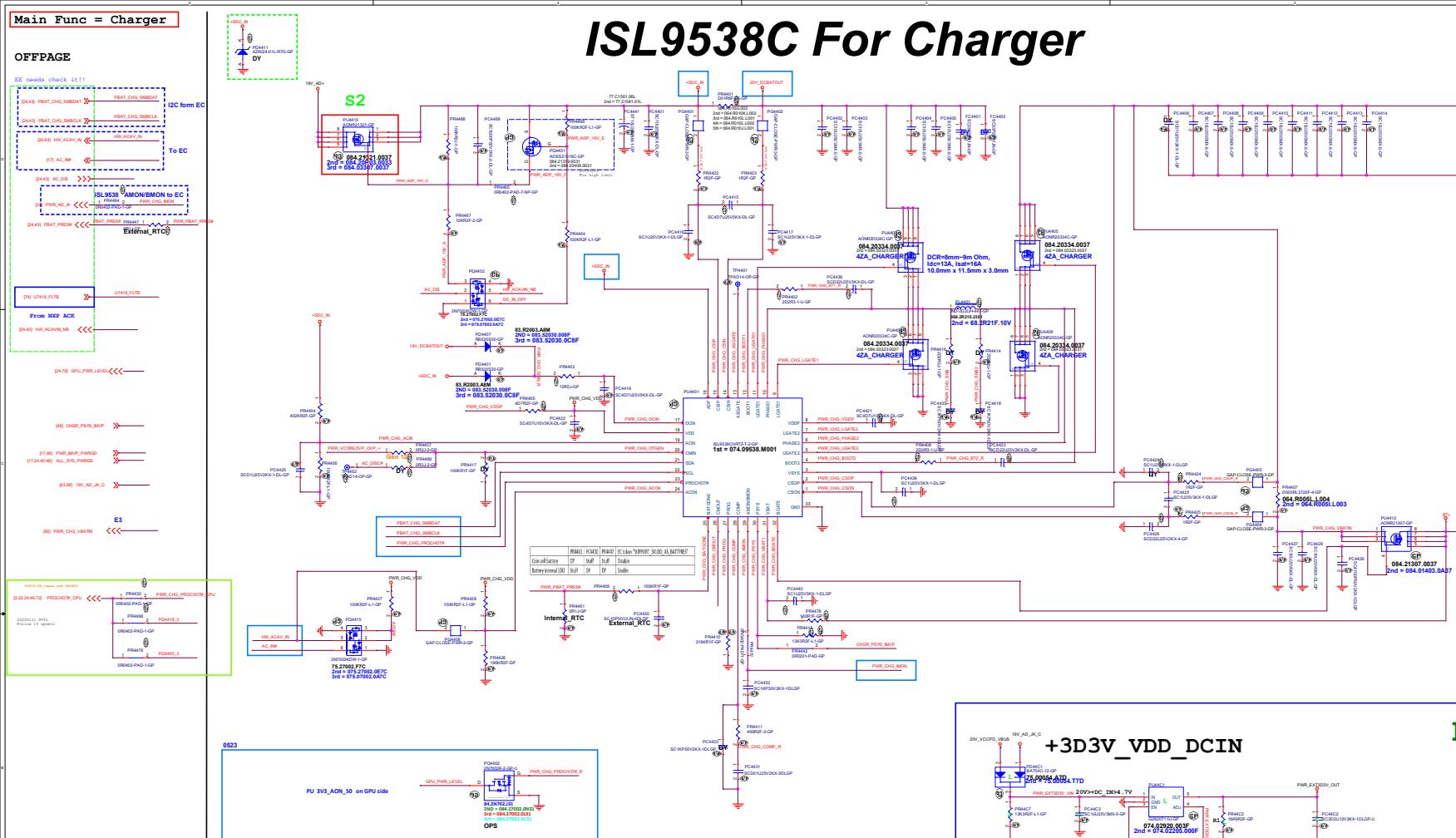


ISL9538C For Charger

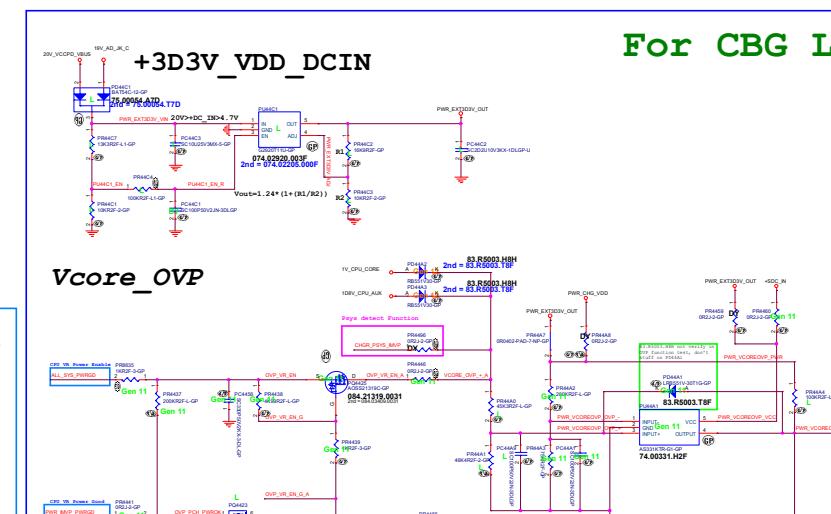
Main Func = Charger

OFFPAGE

EE needs check it!!

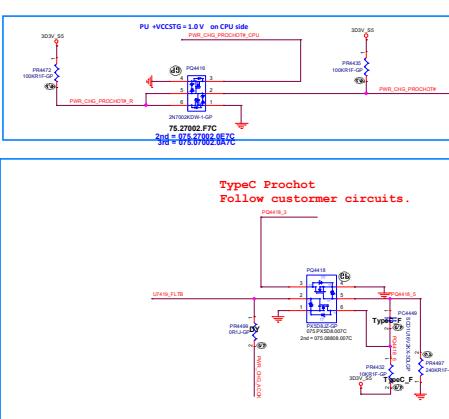


For CBG L

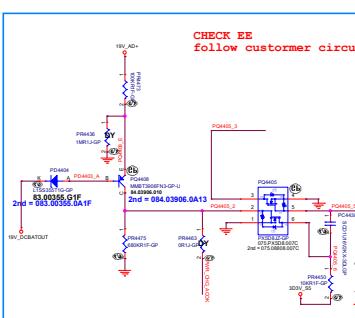


Vaere ov

TABLE 22. PROG PIN PROGRAMMING OPTIONS						
PROG-400 RESISTANCE (Ω)		CELL #	DEFAULT SWITCHING FREQUENCY		AUTONOMOUS CHARGING	DEFAULT ADJUSTED REG(A)
TYP	MIN		1	2		
0		1	733Hz	733Hz	No	0.476
8.45			733Hz	733Hz	No	1.5
14.7			1MHz	1MHz	No	1.5
21.0			1MHz	1MHz	No	0.476
28.0			733Hz	733Hz	Yes	0.476
35.7			733Hz	733Hz	Yes	1.5
43.2		2	733Hz	733Hz	Yes	1.5
52.3			733Hz	733Hz	Yes	0.476
61.9			1MHz	1MHz	No	0.476
71.5			1MHz	1MHz	No	1.5
82.5			733Hz	733Hz	No	1.5
93.1			733Hz	733Hz	No	0.476
105		3	733Hz	733Hz	No	0.476
118			733Hz	733Hz	No	1.5
133			1MHz	1MHz	No	1.5
147			1MHz	1MHz	No	0.476
162			733Hz	733Hz	Yes	0.476
178			733Hz	733Hz	Yes	1.5
196		4	733Hz	733Hz	Yes	1.5
215			733Hz	733Hz	Yes	0.476
237			1MHz	1MHz	No	0.476
261			1MHz	1MHz	No	1.5
287			733Hz	733Hz	No	1.5
316			733Hz	733Hz	No	0.476
348		1	733Hz	733Hz	No	0.476



CHECK EE
follow customer ci



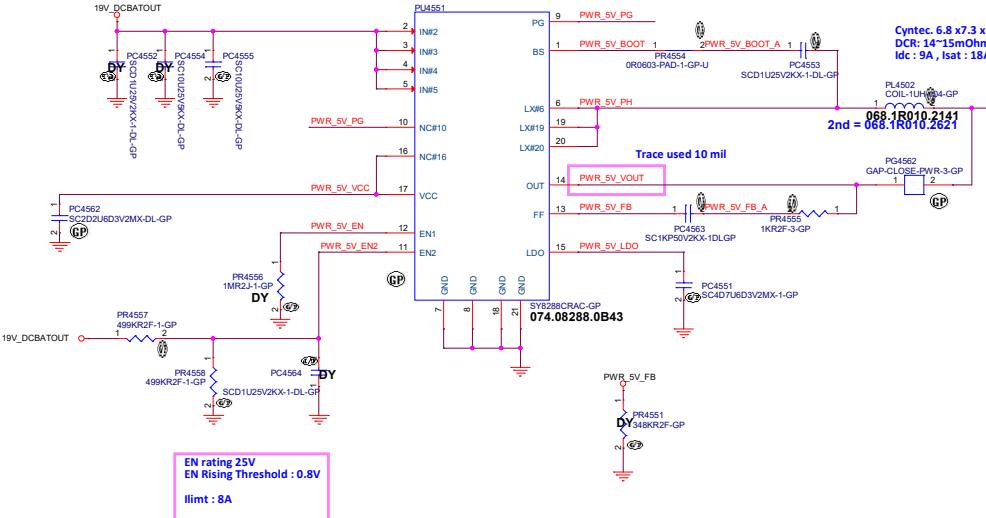
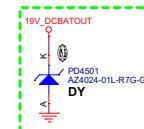
Location	Gen11	Gen12
PC44A1	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PQ4425	Stuff	DY
PR4447	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4446	Stuff	DY
PR4442	Stuff	DY
PR44A3	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU44A1	Stuff	DY
PD44A1	Stuff	DY
PD44A2	DY	Stuff
PD44A3	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff

SY8288C For 5V

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP

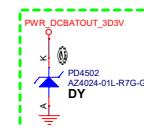


TDC=8.62A
ICCMAX=6.034A
7.2408A<OCP<9.6544A

SSID = PWR.Plane.Regulator_3D3V

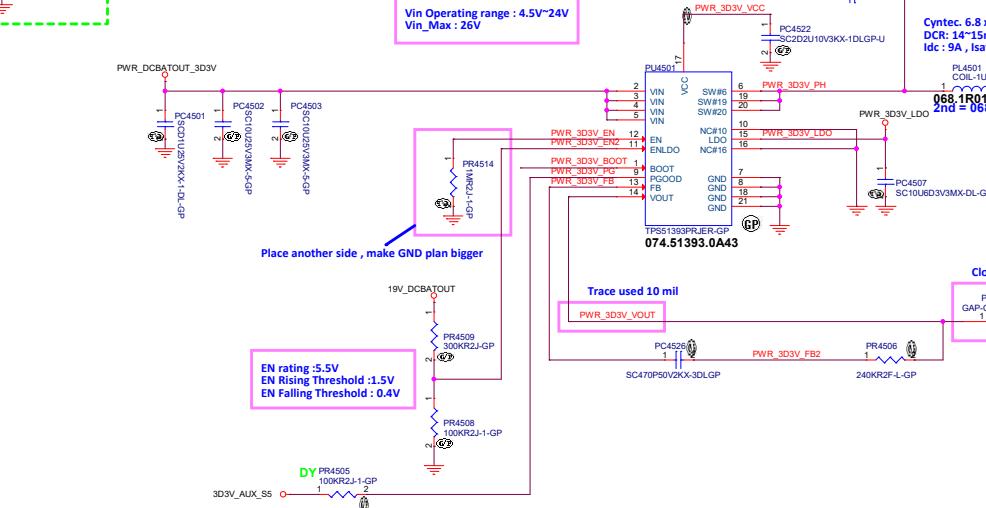
OFFPAGE-Signal

OFFPAGE-GAP



TPS51393 For 3D3V

TDC=7.1171A
ICCMAX=10.1009A
12.12108A<OCP<16.16144A
Design Current : 8A



<Core Design>



POWER (SY8288_5V/3D3V)

Size A2 Document Number Cyborg TGL

Date Thursday, January 15, 2020 Sheet 45 of 105 Rev SC

Main Func = CPU_CORE

OFFPAGE



```

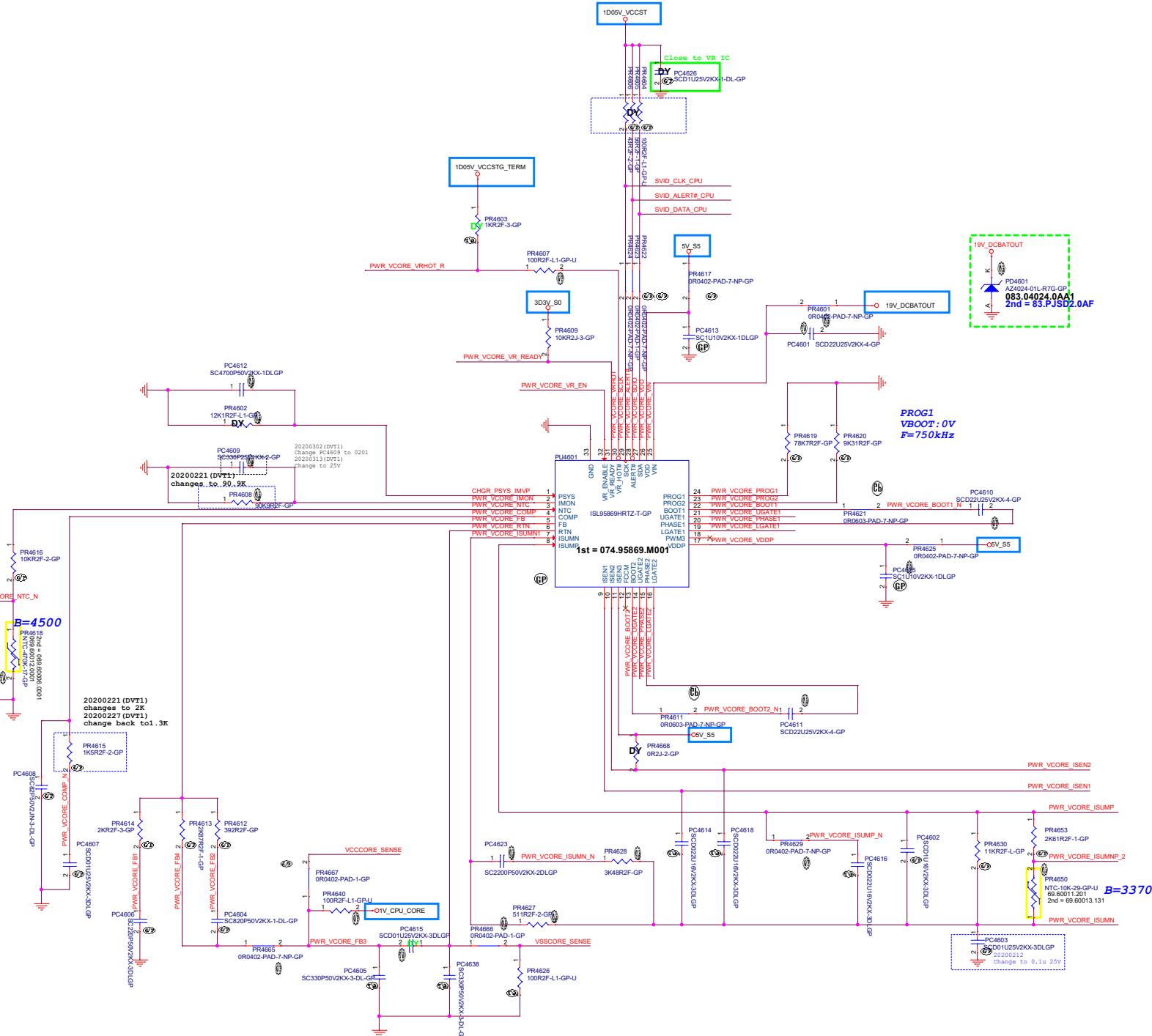
    graph LR
      PR4631[PR4631  
0R4002-PAD-1-GP] -->|1| PWR_VCORE_VRHOT[PWR_VCORE_VRHOT]
      PWR_VCORE_VRHOT -->|2| CHGR_PSYS_IMVP[CHGR_PSYS_IMVP]
      
      subgraph "32.24.44.72"
        PROCHOT_CPU[PROCHOT_CPU]
        PROCHOT_CPU -->|1| PWR_VCORE_VRHOT
      end
      
      subgraph "157.44.191.119"
        NAKIA_NEED_CHANGE[Nakia need change  
not to PWR_VCORE_VR_READ or  
PWR_VCORE_VR_WRITE]
        NAKIA_NEED_CHANGE -->|1| PWR_VCORE_VRHOT
      end
  
```

The diagram illustrates a system architecture where two memory controllers, labeled "VSCORE SENSE" and "VCCORE SENSE", are connected to a shared "VSCORE_SENSE" bus. The "VSCORE SENSE" block is shown with a blue dashed border, indicating it is a component of the Vcore Sense system. The "VCCORE SENSE" block is also connected to the same bus.

[47] PWR_VCORE_UGATE1 ⇕ PWR_VCORE_UGATE
[47] PWR_VCORE_PHASE1 ⇕ PWR_VCORE_PHASE
[47] PWR_VCORE_LGATE1 ⇕ PWR_VCORE_LGATE

[47] PWR_VCORE_UGATE2 ⇕ PWR_VCORE_UGATE2
[47] PWR_VCORE_PHASE2 ⇕ PWR_VCORE_PHASE2
[47] PWR_VCORE_LGATE2 ⇕ PWR_VCORE_LGATE2

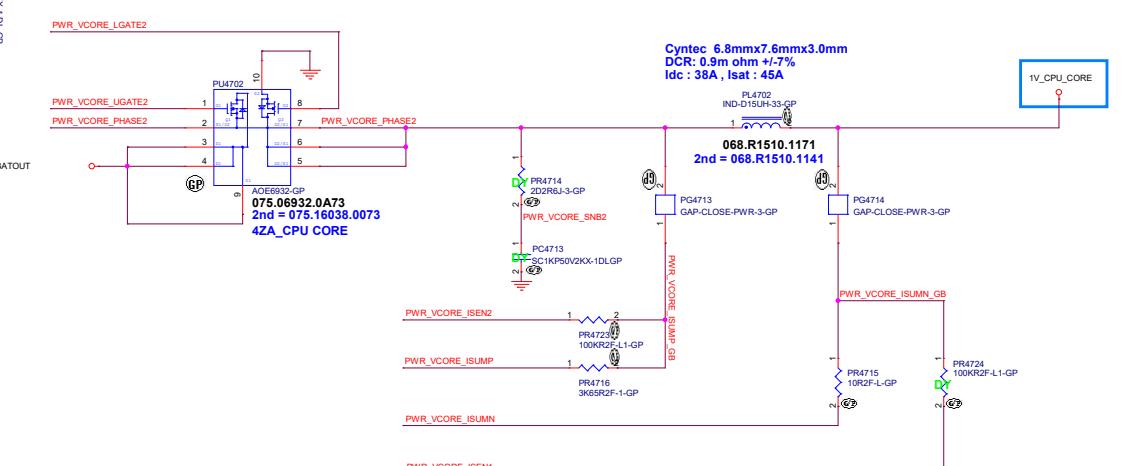
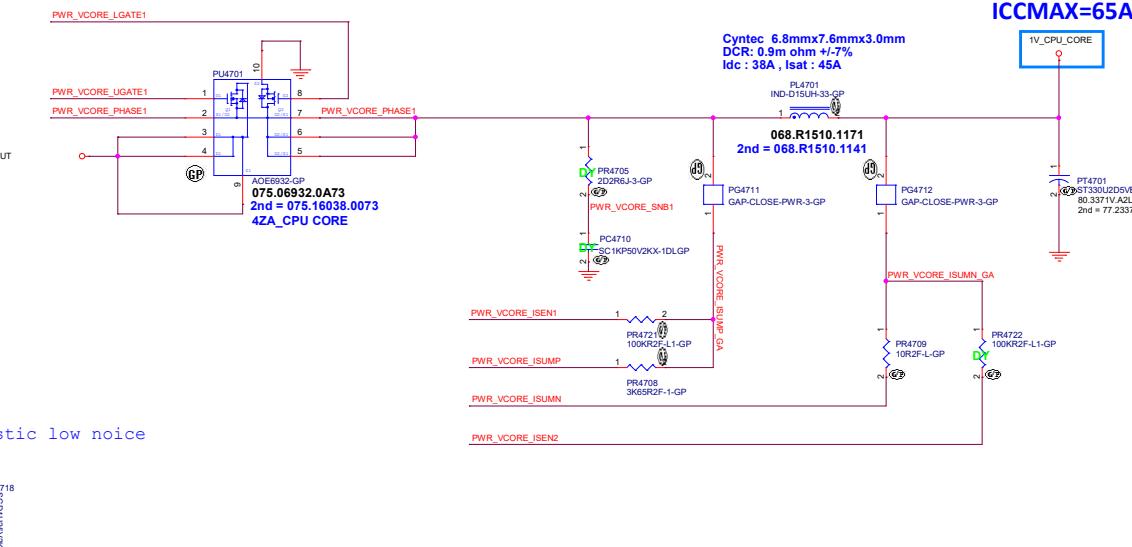
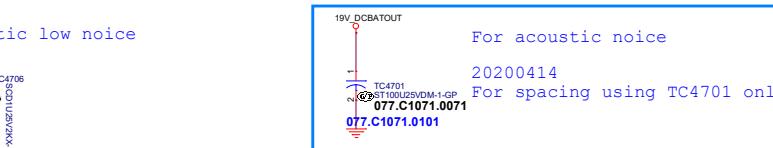
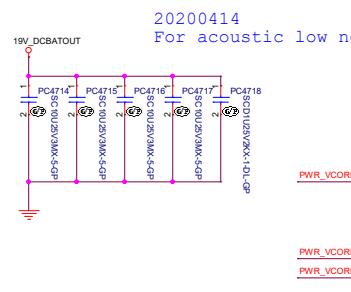
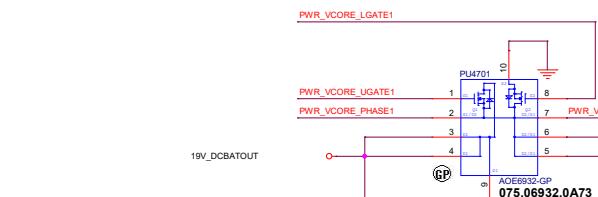
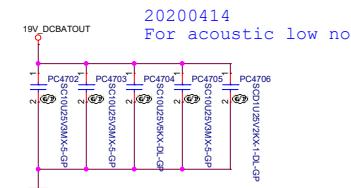
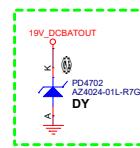
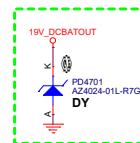
```
[47] PWR_VCORE_ISEN2 >> PWR_VCORE_ISEN2  
[47] PWR_VCORE_ISEN1 >> PWR_VCORE_ISEN1  
[47] PWR_VCORE_ISUMP >> PWR_VCORE_ISUMP  
[47] PWR_VCORE_ISUHM >> PWR_VCORE_ISUHM
```



Main Func = VCCIN

OFFPAGE

46] PWR_VCORE_UGATE	→	PWR_VCORE_UGA
46] PWR_VCORE_PHASE	→	PWR_VCORE_PHA
46] PWR_VCORE_LGATE	→	PWR_VCORE_LGA
46] PWR_VCORE_UGATE	→	PWR_VCORE_UGA
46] PWR_VCORE_PHASE	→	PWR_VCORE_PHA
46] PWR_VCORE_LGATE	→	PWR_VCORE_LGA
46] PWR_VCORE_ISEN2	←	PWR_VCORE_ISEN2
46] PWR_VCORE_ISEN1	←	PWR_VCORE_ISEN1
46] PWR_VCORE_ISJUMP	←	PWR_VCORE_ISJUMP
46] PWR_VCORE_ISJUMN	←	PWR_VCORE_ISJUMN



Main Func = CPU_CORE

D

D

c

C

→

←

B

B

A

A

<Core Design>

	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	
Size A3	Document Number
Rev SC	Date: Thursday, January 14, 2021

D

D

C

C

B

B

A

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title (RSVD)		Rev SC
Size A	Document Number Cyborg TGL	
Date: Thursday, January 14, 2021	Sheet 49 of 105	

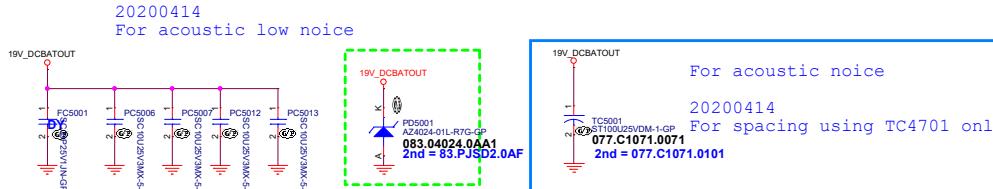
Main Func = VCCIN_AUX

OFFPAGE

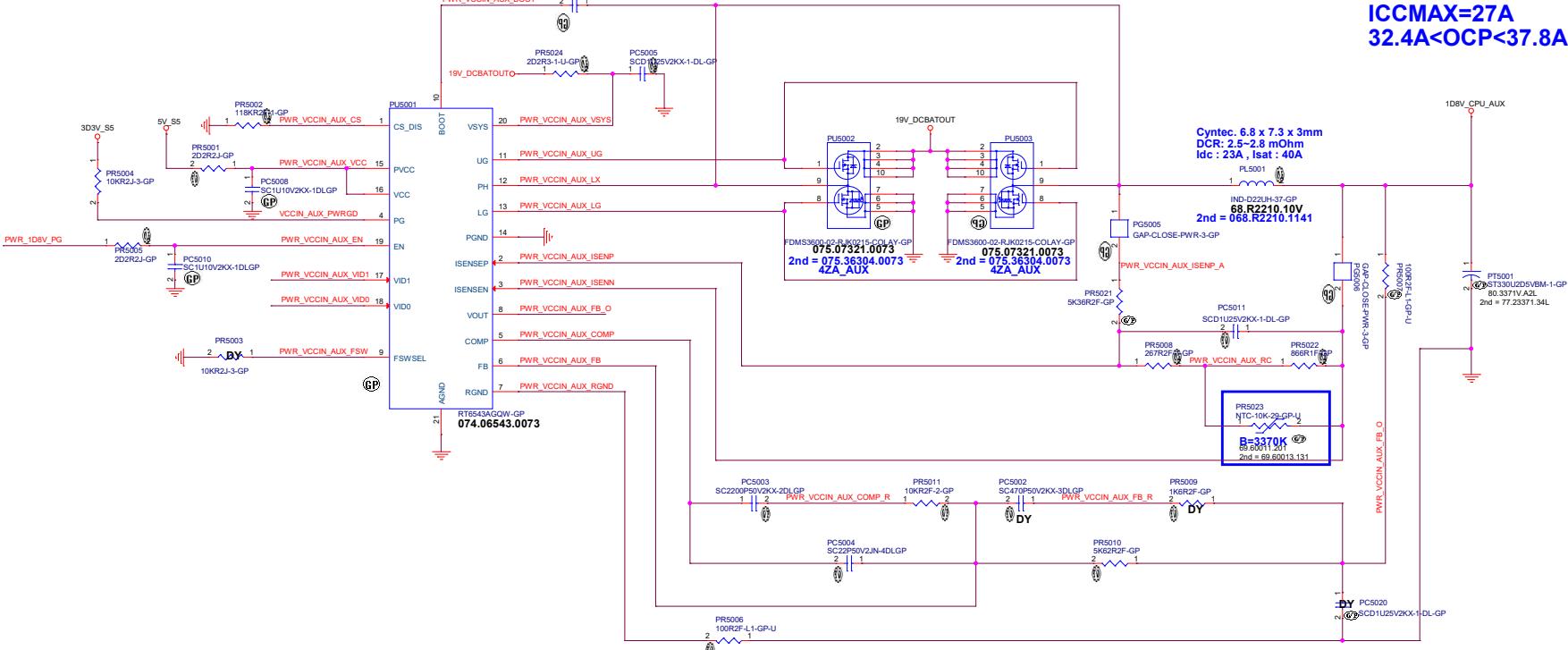
<i>VID</i>				
[22,40] CORE_VID0	>>>	1	PWR_VCCIN_AUX_VID0	
			PR5014 GR4042-PAD-7-NP-GP	
[22,40] CORE_VID1	>>>	1	PWR_VCCIN_AUX_VID1	
			PR5015 GR4042-PAD-7-NP-GP	

[40,53] PWR_1D8V_PG ➤

[17,24,40] VCCIN_AUX_PWRGD <<<—



TGL_U42 28W
Performance
TDC=14A
ICCMAX=27A
32.4A<OCP<37.8A



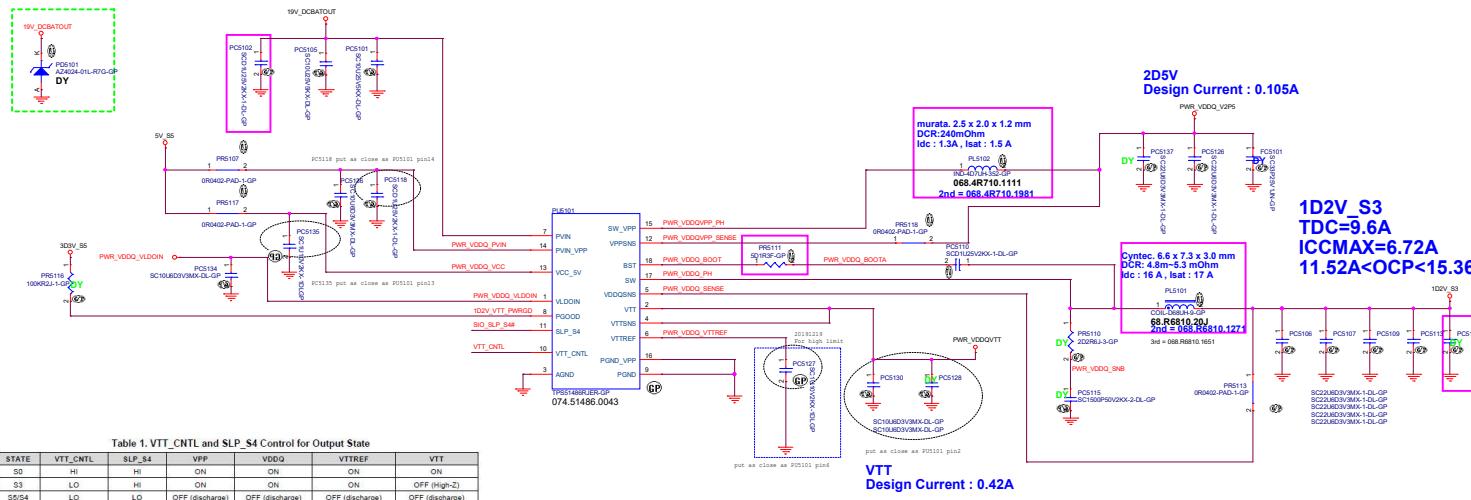
OFFPAGE

S5
[17.68] SIO_SLP_S4# >> SIO_SLP_S4#

S3
[8] VTT_CNTL >> VTT_CNTL

PH on EE Side
[4] PWR_VDDQ_PG << RSD01 102V_VTT_PWRGD
OR0402-PAD-7-NP-GP

OFFPAGE_GAP



STATE	VTT_CNTL	SLP_S4	VTF	VDDQ	VTRREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

102V_S3
PWR_VDDQ_VDDIN
GAP-CLOSE-PWR-3-GP

VTT
102V_VREF_30
1
2
PWR_VDDQ_VTT
GAP-CLOSE-PWR-3-GP

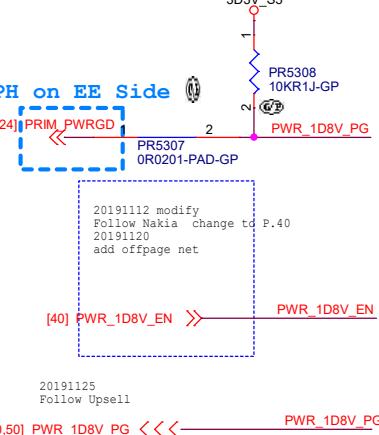
2D5V
2D5V_S3
PWR_VDDQ_V2PS
GAP-CLOSE-PWR-3-GP



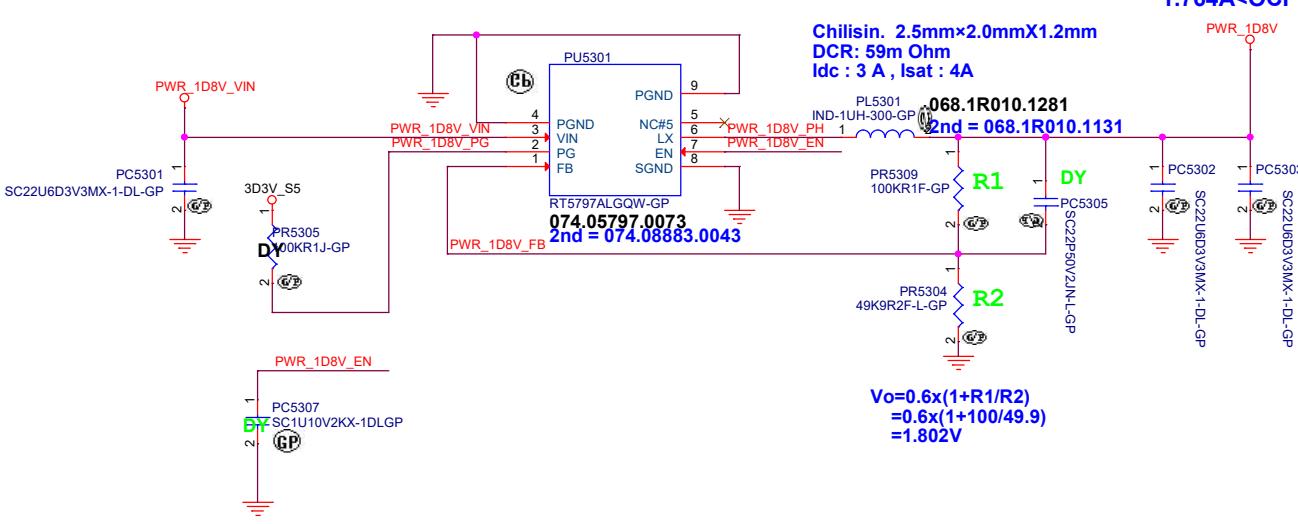
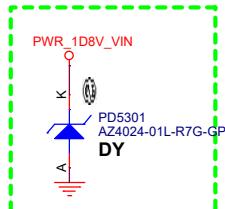
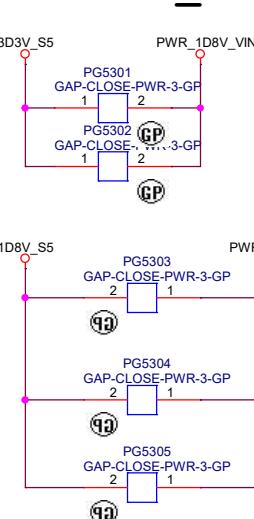
Main Func = 1D8V/1D2V

TDC=1.029A
ICCMAX=1.47A
1.764A<OCP<2.352A

OFFPAGE



OFFPAGE_GAP

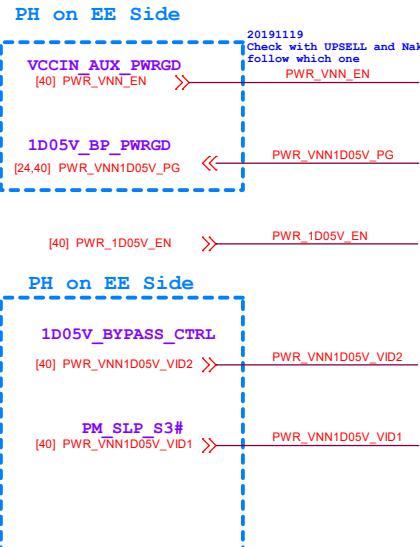


<Core Design>

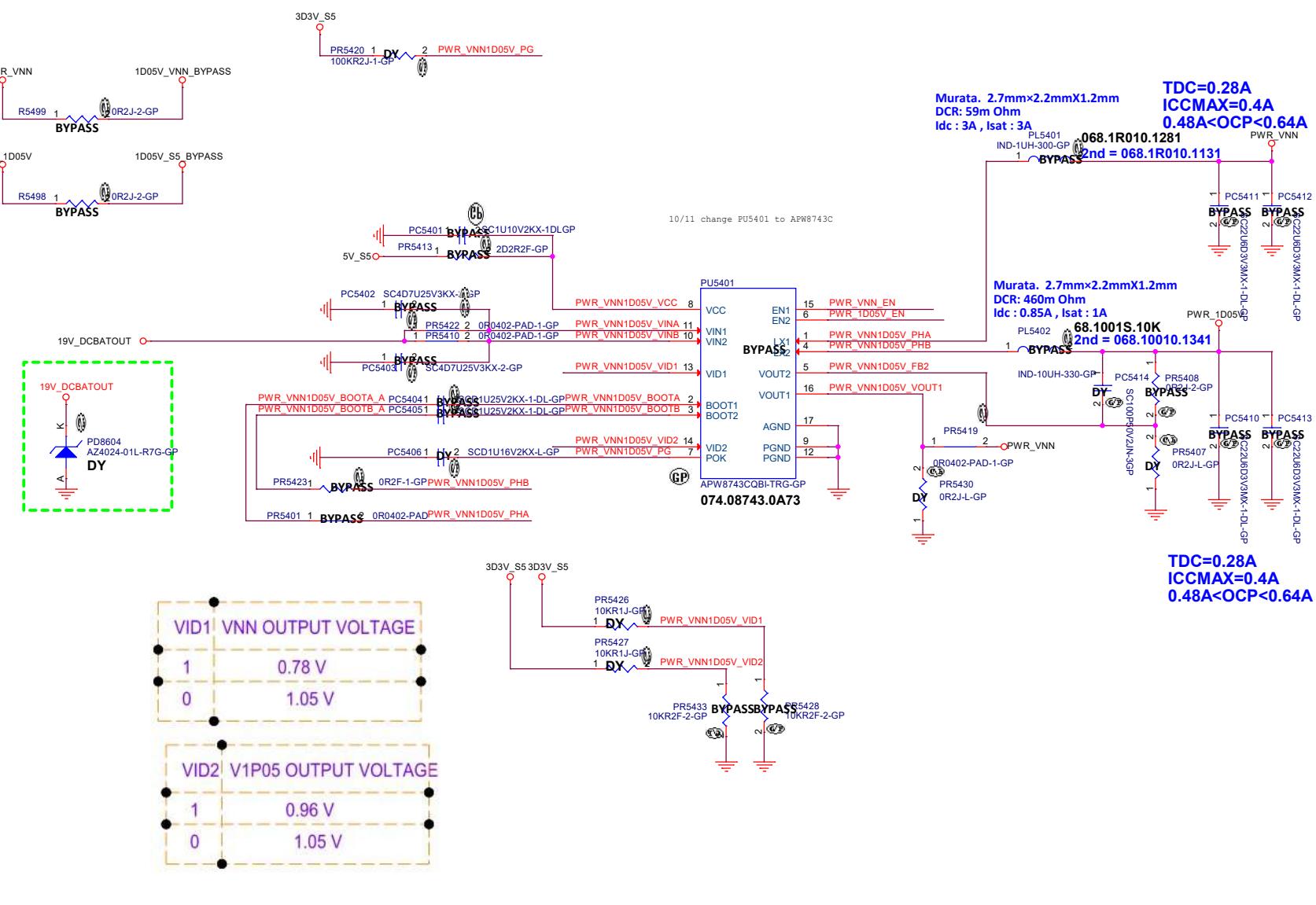
DELL	Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD&CAM&DMC&Touch
Size	Document Number
B	Cyborg TGL
Rev	SC
Date: Thursday, January 14, 2021	Sheet 53 of 105

Main Func = 1D05V

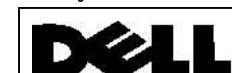
OFFPAGE



OFFPAGE-GAP



<Core Design



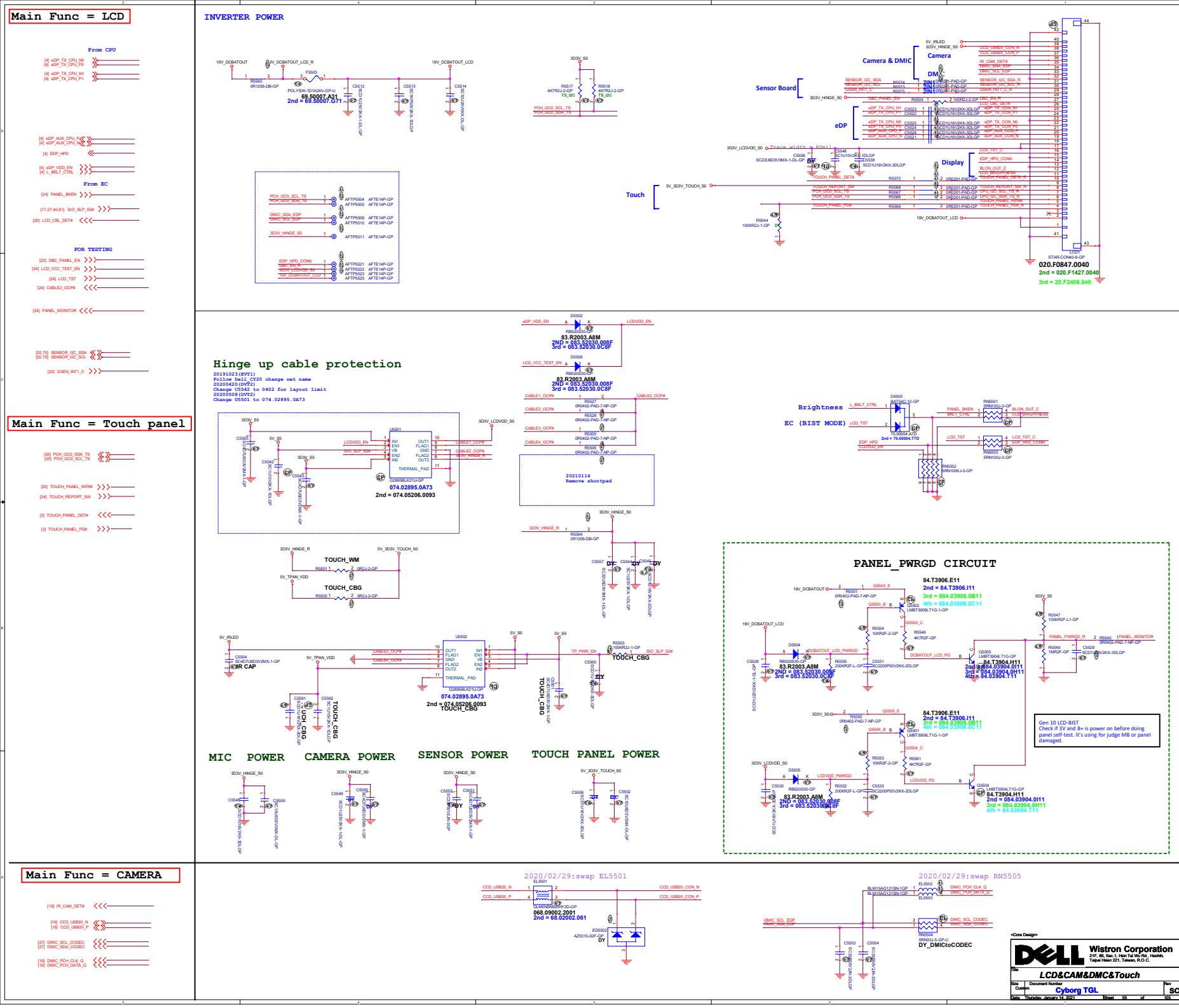
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER(API)2024-VMM1D2E

POWER(APW8738A)

N1D05

Document Number: Cyborg TGL | Page 1 of 1 | Rev: SC | Date: 01/01/2024

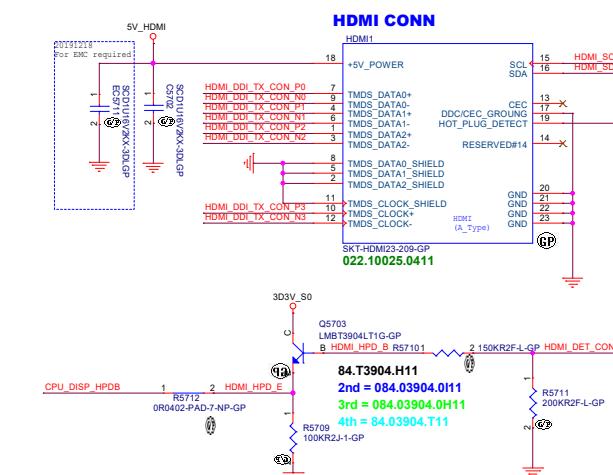
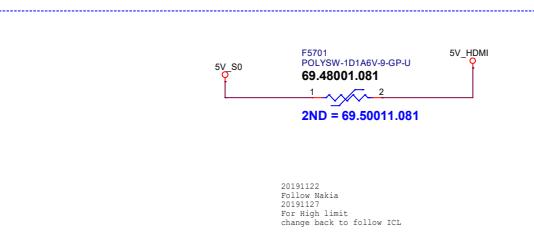
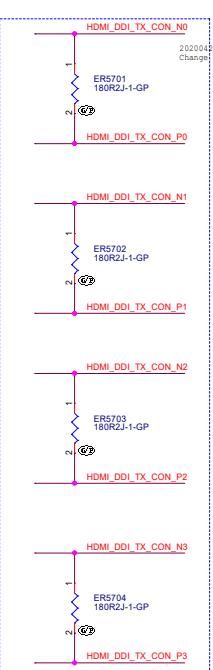
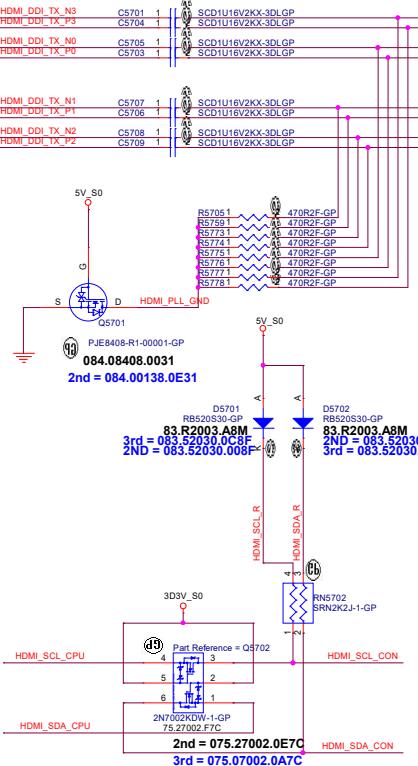




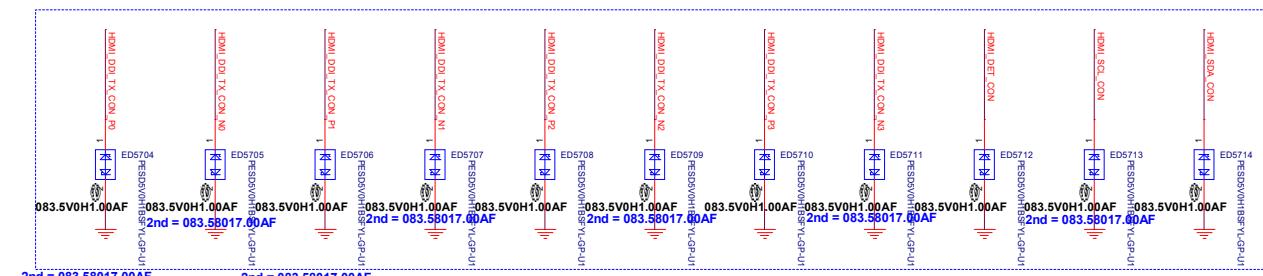
SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0
 [4] HDMI_DDI_TX_P0
 [4] HDMI_DDI_TX_N1
 [4] HDMI_DDI_TX_P1
 [4] HDMI_DDI_TX_N2
 [4] HDMI_DDI_TX_P2
 [4] HDMI_DDI_TX_N3
 [4] HDMI_DDI_TX_P3

[4] HDMI_SCL_CPU
 [4] HDMI_SDA_CPU
 [4] CPU_DISP_HPDB



EMI Request:



(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		Rev
	(Reserved)	
Size A4	Document Number Cyborg TGL	
Date: Thursday, January 14, 2021	Sheet 58 of 105	SC

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

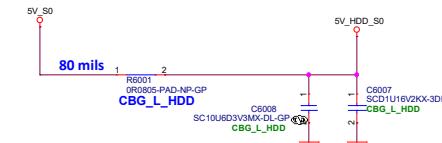
Title		Rev
	(Reserved)	
A4	Cyborg TGL	SC
Date: Thursday, January 14, 2021	Sheet 59 of 105	

Main Func = HDD

HDD POWER

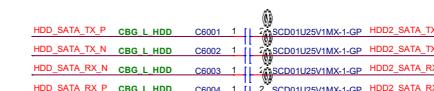
HDD

- [70] FFS_INT2_Q >>>
- [16,60] HDD_DEVSLP >>>
- [16] HDD_SATA_TX_P >>>
- [16] HDD_SATA_RX_P >>>
- [16] HDD_SATA_RX_N <<<
- [16] HDD_SATA_RX_N <<<
- [16,60] HDD_DEVSLP <<<
- [16] HDD_DETF <<<

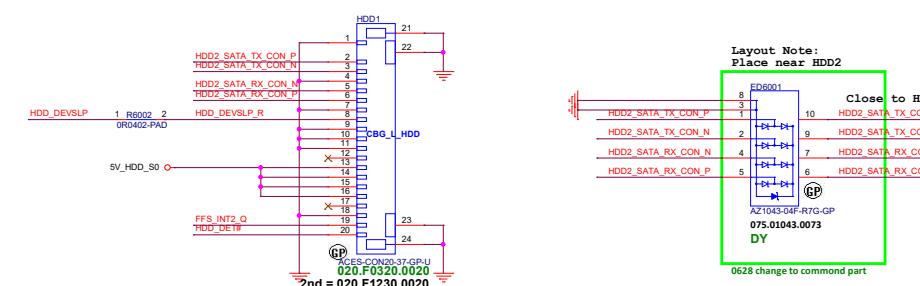


SATA RE-DRIVER

20201013
Remove



SATA HDD Connector



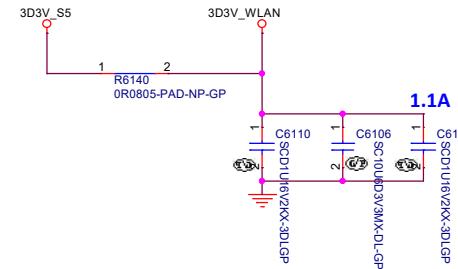
Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P

[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

3D3V_WLAN
1
R6145
10KR2J-3-GP



AFTE14P-GP	AFTP6101	1	3D3V_WLAN
AFTE14P-GP	AFTP6105	1	CLK_PCIE_WLAN_REQ#
AFTE14P-GP	AFTP6106	1	WIFI_RF_EN_R
AFTE14P-GP	AFTP6107	1	BT_USB20_EN_R
AFTE14P-GP	AFTP6108	1	PCH_PLTRST#
AFTE14P-GP	AFTP6109	1	BT_USB20_CON_N
AFTE14P-GP	AFTP6109	1	BT_USB20_CON_P
AFTE14P-GP	AFTP6110	1	JIO3_PCIE_WAKE#
AFTE14P-GP	AFTP6111	1	

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P

[18] CLK_PCIE_WLAN_REQ#

WLAN_RF_DIS#
2
R6144
0R0402-PAD-7-NP-GP

3D3V_WLAN
1
R6146
10KR2J-3-GP

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

BT_RADIO_DIS#
2
R6143
0R0402-PAD-7-NP-GP

3D3V_WLAN
1
R6147
10KR2J-3-GP

Single end

[19] BT_RADIO_DIS#
>>>
[16] WLAN_RF_DIS#
>>>
[17,62,63,66,71,76,91] PCH_PLTRST#
>>>

Debug

Power EN (Madesimo)

[21] CNV_BRI_DT_R
>>>

[21] CLKREQ_CNV
>>>

[21] CNV_RF_RESET#
>>>

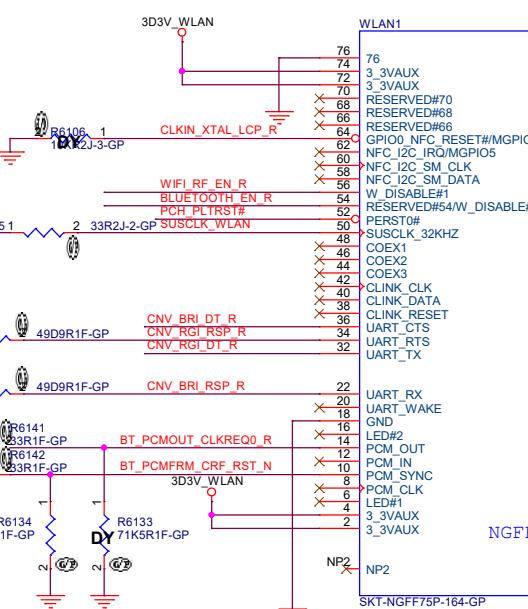
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP

[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP

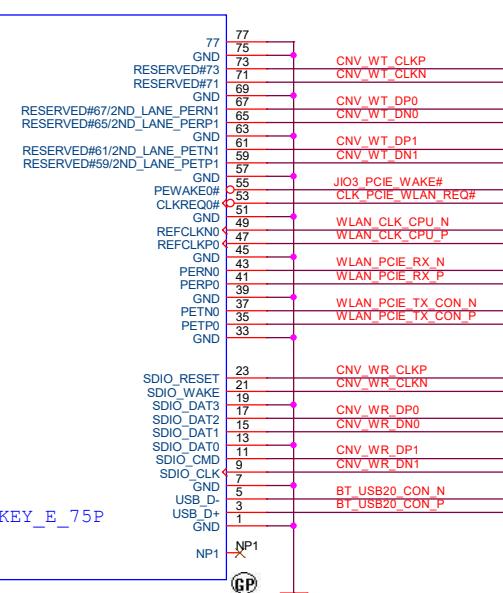
[21] CNV_BRI_RSP
>>>

[21] CNV_RGI_RSP
>>>

[24] JIO3_PCIE_WAKE#
>>>



SKT-NGFF75P-164-GP
062.10003.0B11
2nd = 062.10007.0371



CNVI_WT_CLKP
CNVI_WT_CLKN
CNVI_WT_DP0
CNVI_WT_DN0
CNVI_WT_DP1
CNVI_WT_DN1
PEWAKER0H
CLKREQ0H
REFCLK0H
REFCLKPO
PERNO
PERP0
PETNO
PETP0
GND

WLAN_CLK_CPU_N
WLAN_CLK_CPU_P

WLAN_PCIE_RX_N
WLAN_PCIE_RX_P

WLAN_PCIE_TX_N
WLAN_PCIE_TX_P

CNVI_WR_CLKP
CNVI_WR_CLKN

CNVI_WR_DP0
CNVI_WR_DN0

CNVI_WR_DP1
CNVI_WR_DN1

BT_USB20_CON_N
BT_USB20_CON_P

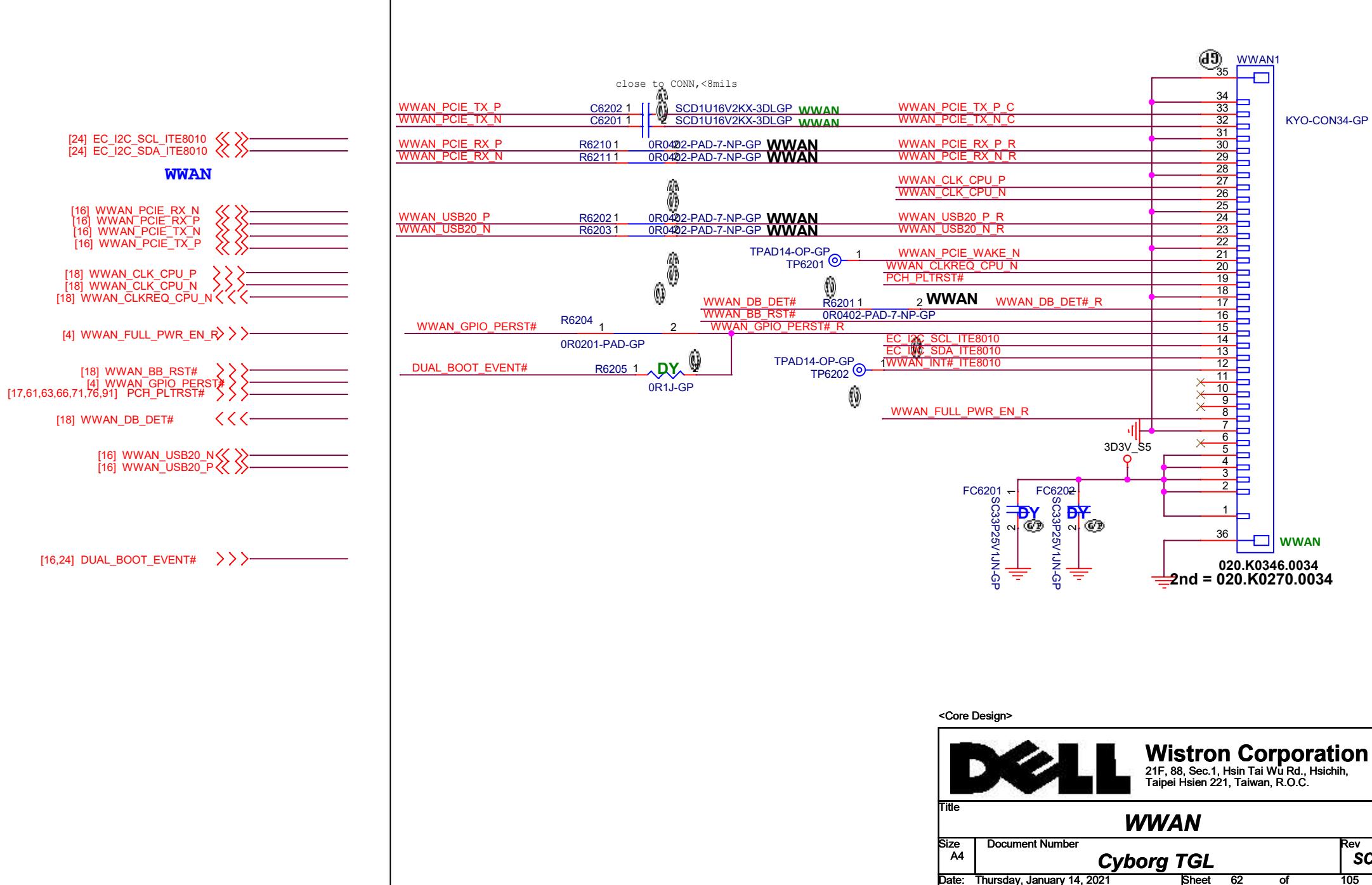
BT_USB20_P

BT_USB20_N

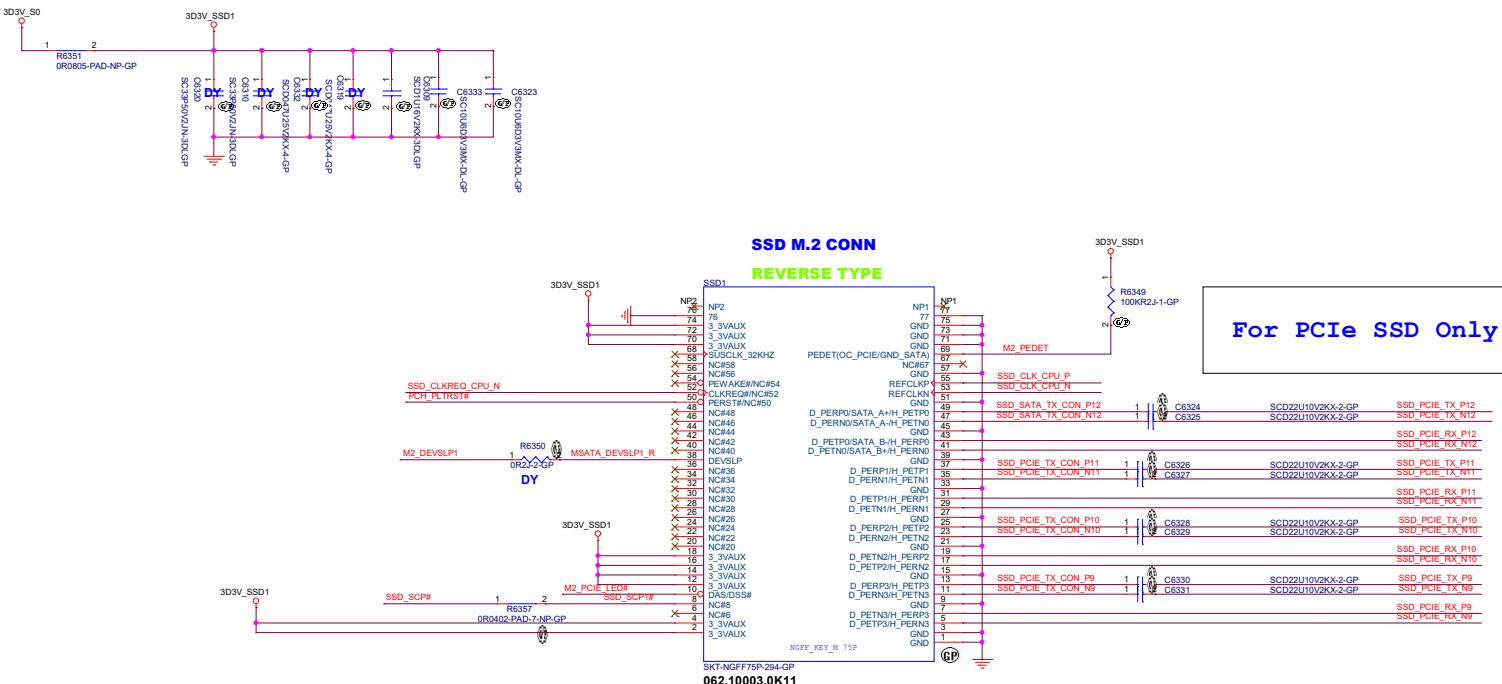
<Core Design>

Main Func = WWAN

For CBG L

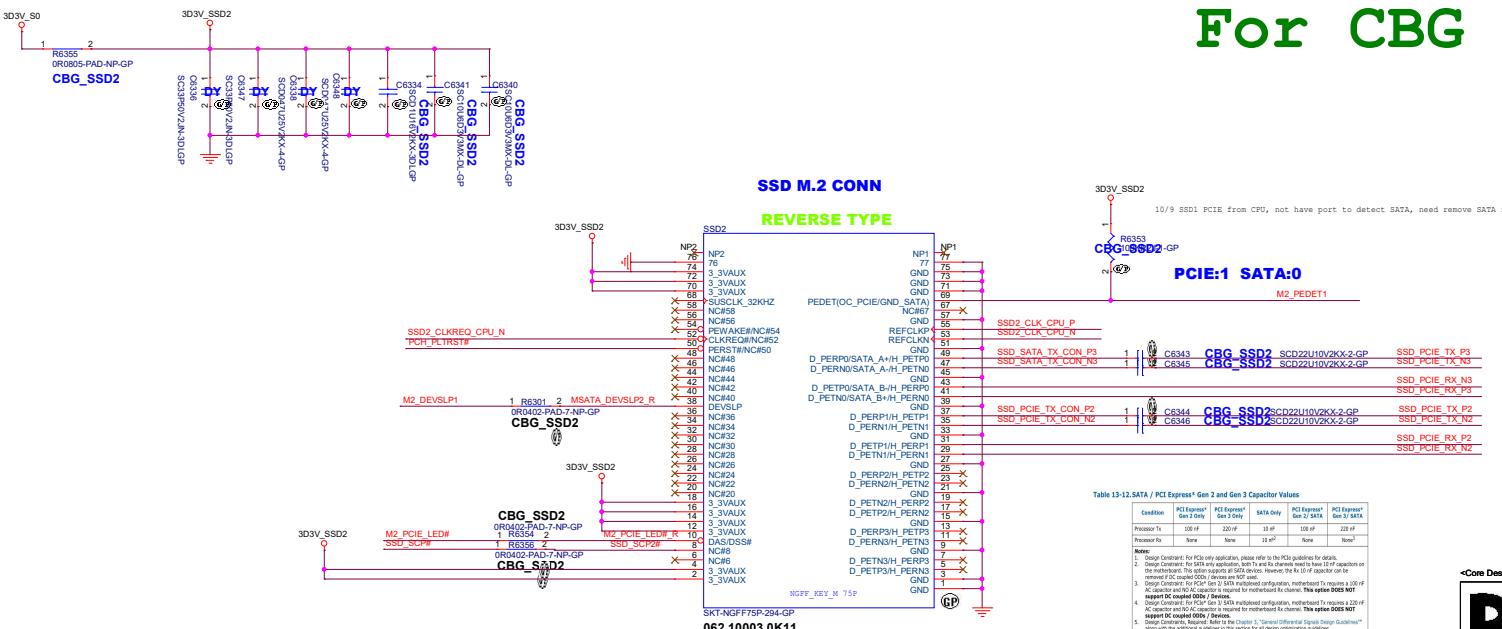


Main Func = M.2 SSD



For PCIe SSD Only

M.2 SSD2

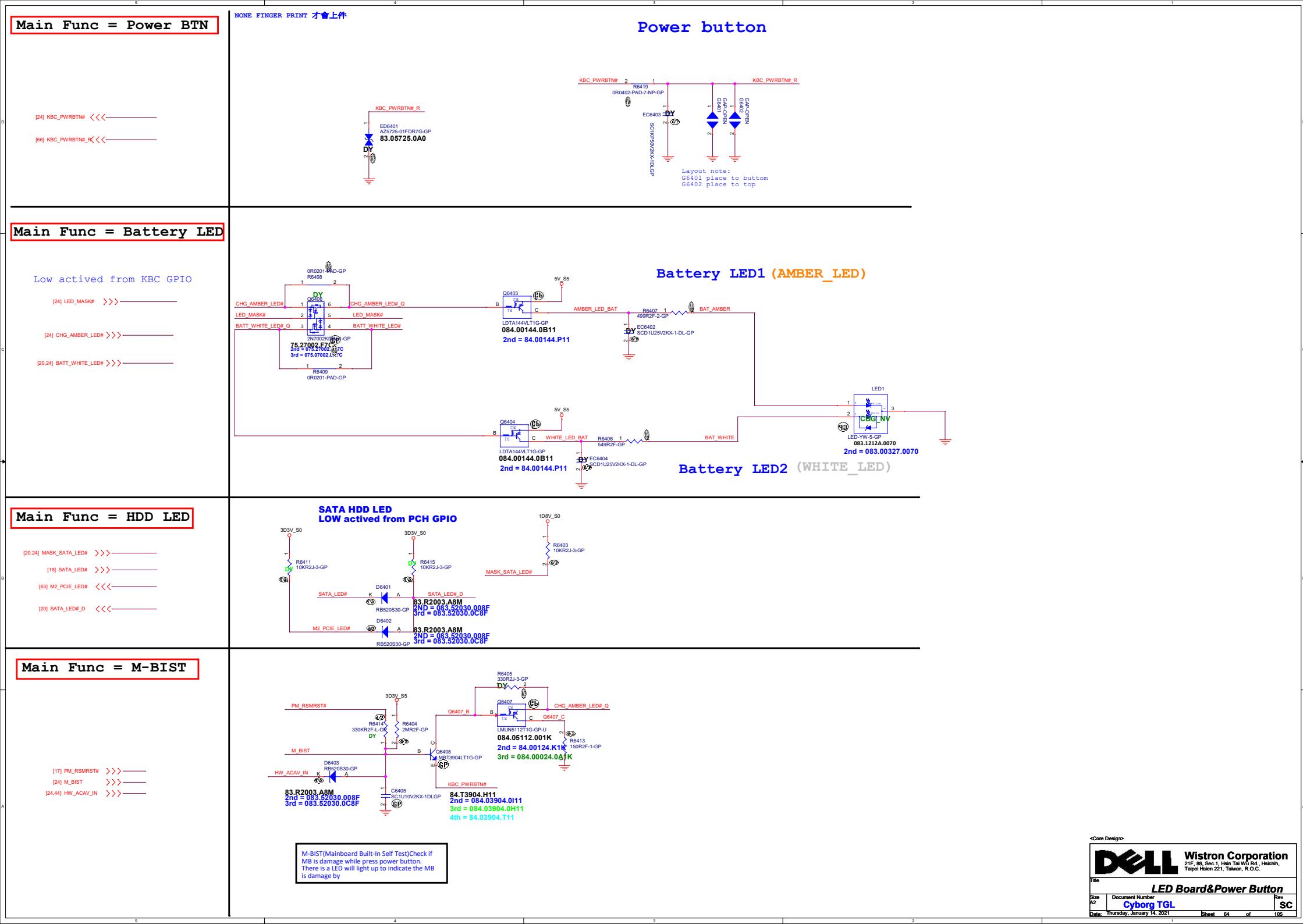


For CBG 15" N/V

Condition	PCI Express® Gen 1	PCI Express® Gen 2	PCI Express® Gen 3 Only
Processor Tx	160 MB/s	320 MB/s	
Processor Rx	Name	Name	
PCIe Lane			
Design Constraint: For PCIe only applications, please ensure that the system has enough lanes to support the required bandwidth.			
Design Constraint: This option supports all SATA devices.			
Design Constraint: For PCIe Gen 2 and SATA multipliers greater than 1, the system must have enough lanes to support DC coupled DQs / Devices.			
AC Accelerator and DC AC capability is required for most applications.			
Design Constraint: Required for RAID 1 Channel.			
Design Constraint: For PCIe lanes that need to support both AC and DC coupled DQs / Devices.			
DC coupled DQs / Devices.			

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform	
24	NC
25	NC
26	NC
27	NC
28	NC
29	NC
30	NC
31	NC
32	NC
33	NC
34	NC
35	NC
36	NC
37	NC
38	NC
39	NC
40	NC
41	NC
42	NC
43	NC
44	NC
45	NC
46	NC
47	NC
48	NC
49	NC
50	NC
51	NC
52	NC
53	NC
54	NC
55	NC
56	NC
57	NC
58	NC
59	NC
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	NC
75	NC
76	NC
77	NC
78	NC
79	NC
80	NC
81	NC
82	NC
83	NC
84	NC
85	NC
86	NC
87	NC
88	NC
89	NC
90	NC
91	NC
92	NC
93	NC
94	NC
95	NC
96	NC
97	NC
98	NC
99	NC
100	NC
101	NC
102	NC
103	NC
104	NC
105	NC
106	NC
107	NC
108	NC
109	NC
110	NC
111	NC
112	NC
113	NC
114	NC
115	NC
116	NC
117	NC
118	NC
119	NC
120	NC
121	NC
122	NC
123	NC
124	NC
125	NC
126	NC
127	NC
128	NC
129	NC
130	NC
131	NC
132	NC
133	NC
134	NC
135	NC
136	NC
137	NC
138	NC
139	NC
140	NC
141	NC
142	NC
143	NC
144	NC
145	NC
146	NC
147	NC
148	NC
149	NC
150	NC
151	NC
152	NC
153	NC
154	NC
155	NC
156	NC
157	NC
158	NC
159	NC
160	NC
161	NC
162	NC
163	NC
164	NC
165	NC
166	NC
167	NC
168	NC
169	NC
170	NC
171	NC
172	NC
173	NC
174	NC
175	NC
176	NC
177	NC
178	NC
179	NC
180	NC
181	NC
182	NC
183	NC
184	NC
185	NC
186	NC
187	NC
188	NC
189	NC
190	NC
191	NC
192	NC
193	NC
194	NC
195	NC
196	NC
197	NC
198	NC
199	NC
200	NC
201	NC
202	NC
203	NC
204	NC
205	NC
206	NC
207	NC
208	NC
209	NC
210	NC
211	NC
212	NC
213	NC
214	NC
215	NC
216	NC
217	NC
218	NC
219	NC
220	NC
221	NC
222	NC
223	NC
224	NC
225	NC
226	NC
227	NC
228	NC
229	NC
230	NC
231	NC
232	NC
233	NC
234	NC
235	NC
236	NC
237	NC
238	NC
239	NC
240	NC
241	NC
242	NC
243	NC
244	NC
245	NC
246	NC
247	NC
248	NC
249	NC
250	NC
251	NC
252	NC
253	NC
254	NC
255	NC
256	NC
257	NC
258	NC
259	NC
260	NC
261	NC
262	NC
263	NC
264	NC
265	NC
266	NC
267	NC
268	NC
269	NC
270	NC
271	NC
272	NC
273	NC
274	NC
275	NC
276	NC
277	NC
278	NC
279	NC
280	NC
281	NC
282	NC
283	NC
284	NC
285	NC
286	NC
287	NC
288	NC
289	NC
290	NC
291	NC
292	NC
293	NC
294	NC
295	NC
296	NC
297	NC
298	NC
299	NC
300	NC
301	NC
302	NC
303	NC
304	NC
305	NC
306	NC
307	NC
308	NC
309	NC
310	NC
311	NC
312	NC
313	NC
314	NC
315	NC
316	NC
317	NC
318	NC
319	NC
320	NC
321	NC
322	NC
323	NC
324	NC
325	NC
326	NC
327	NC
328	NC
329	NC
330	NC
331	NC
332	NC
333	NC
334	NC
335	NC
336	NC
337	NC
338	NC
339	NC
340	NC
341	NC
342	NC
343	NC
344	NC
345	NC
346	NC
347	NC
348	NC
349	NC
350	NC
351	NC
352	NC
353	NC
354	NC
355	NC
356	NC
357	NC
358	NC
359	NC
360	NC
361	NC
362	NC
363	NC
364	NC
365	NC
366	NC
367	NC
368	NC
369	NC
370	NC
371	NC
372	NC
373	NC
374	NC
375	NC
376	NC
377	NC
378	NC
379	NC
380	NC
381	NC
382	NC
383	NC
384	NC
385	NC
386	NC
387	NC
388	NC
389	NC
390	NC
391	NC
392	NC
393	NC
394	NC
395	NC
396	NC
397	NC
398	NC
399	NC
400	NC
401	NC
402	NC
403	NC
404	NC
405	NC
406	NC
407	NC
408	NC
409	NC
410	NC
411	NC
412	NC
413	NC
414	NC
415	NC
416	NC
417	NC
418	NC
419	NC
420	NC
421	NC
422	NC
423	NC
424	NC
425	NC
426	NC
427	NC
428	NC
429	NC
430	NC
431	NC
432	NC
433	NC
434	NC
435	NC
436	NC
437	NC
438	NC
439	NC
440	NC
441	NC
442	NC
443	NC
444	NC
445	NC
446	NC
447	NC
448	NC
449	NC
450	NC
451	NC
452	NC
453	NC
454	NC
455	NC
456	NC
457	NC
458	NC
459	NC
460	NC
461	NC
462	NC
463	NC
464	NC
465	NC
466	NC
467	NC
468	NC
469	NC
470	NC
471	NC
472	NC
473	NC
474	NC
475	NC
476	NC
477	NC
478	NC
479	NC
480	NC
481	NC
482	NC
483	NC
484	NC
485	NC
486	NC
487	NC
488	NC
489	NC
490	NC
491	NC
492	NC
493	NC
494	NC
495	NC
496	NC
497	NC
498	NC
499	NC
500	NC
501	NC
502	NC
503	NC
504	NC
505	NC
506	NC
507	NC
508	NC
509	NC
510	NC
511	NC
512	NC
513	NC
514	NC
515	NC
516	NC
517	NC
518	NC
519	NC
520	NC
521	NC
522	NC
523	NC
524	NC
525	NC
526	NC
527	NC
528	NC
529	NC
530	NC
531	NC
532	NC
533	NC
534	NC
535	NC
536	NC
537	NC
538	NC
539	NC
540	NC
541	NC
542	NC
543	NC
544	NC
545	NC
546	NC
547	NC
548	NC
549	NC
550	NC
551	NC
552	NC
553	NC
554	NC
555	NC
556	NC
557	NC
558	NC
559	NC
560	NC
561	NC
562	NC
563	NC
564	NC
565	NC
566	NC
567	NC
568	NC
569	NC
570	NC
571	NC
572	NC
573	NC
574	NC
575	NC
576	NC
577	NC
578	NC
579	NC
580	NC
581	NC
582	NC
583	NC
584	NC
585	NC
586	NC
587	NC
588	NC
589	NC
590	NC
591	NC
592	NC
593	NC
594	NC
595	NC
596	NC
597	NC
598	NC
599	NC
600	NC
601	NC
602	NC
603	NC
604	NC
605	NC
606	NC
607	NC
608	NC
609	NC
610	NC
611	NC
612	NC
613	NC
614	NC
615	NC
616	NC
617	NC
618	NC
619	NC
620	NC
621	NC
622	NC
623	NC
624	NC
625	NC
626	NC
627	NC
628	NC
629	NC
630	NC
631	NC
632	NC
633	NC
634	NC
635	NC
636	NC
637	NC
638	NC
639	NC
640	NC
641	NC
642	NC
643	NC
644	NC
645	NC
646	NC
647	NC
648	NC
649	NC
650	NC
651	NC
652	NC
653	NC
654	NC
655	NC
656	NC
657	NC
658	NC
659	NC
660	NC
661	NC
662	NC
663	NC
664	NC
665	NC
666	NC
667	NC
668	NC
669	NC
670	NC
671	NC
672	NC
673	NC
674	NC
675	NC
676	NC
677	NC
678	NC
679	NC
680	NC
681	NC
682	NC
683	NC
684	NC
685	NC
686	NC
687	NC
688	NC
689	NC
690	NC
691	NC
692	NC
693	NC
694	NC
695	NC
696	NC
697	NC
698	NC
699	NC





Main Func = KB

[24] CAP_LED#_R >>>

[4] KB_DET# <<<

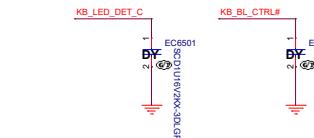
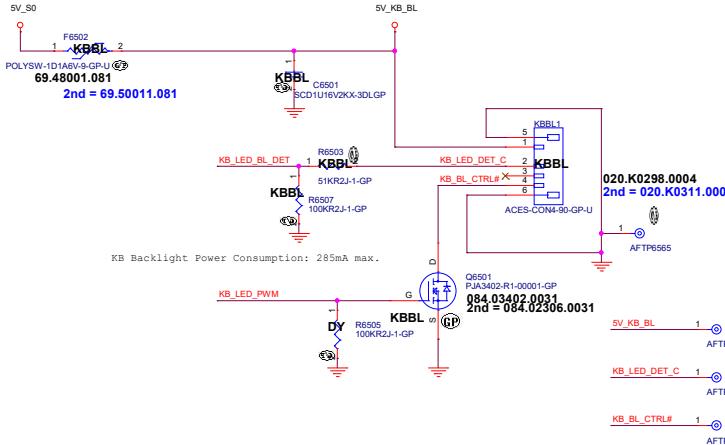
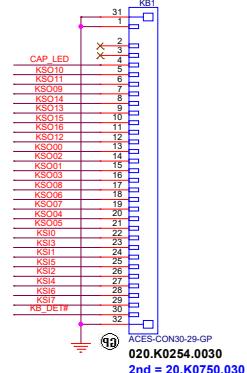
[20] KB_LED_BL_DET <<<

[24] KB_LED_PWM >>>

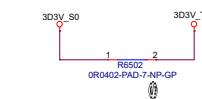
[24] KS000
[24] KS001
[24] KS002
[24] KS003
[24] KS004
[24] KS005
[24] KS006
[24] KS007
[24] KS008
[24] KS009
[24] KS010
[24] KS011
[24] KS012
[24] KS013
[24] KS014
[24] KS015
[24] KS016

[24] KSI[0..7] <<>>

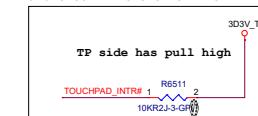
Keyboard Backlight (Reserved)

CAP LED Control
LOW activated from KBC GPIO

Main Func = TPAD



Need to check if it is Active High or Active Low and check if there is FH on TPAD side.



Support PTP

[24] EC_I2C_SDA_TP
[24] EC_I2C_SCL_TP

[20..66] CPU_I2C_SCL_P0
[20..66] CPU_I2C_SDA_P0

[3..24] TOUCHPAD_INTR#<<<

[24] PTP_DISP#<<<

5

PS2

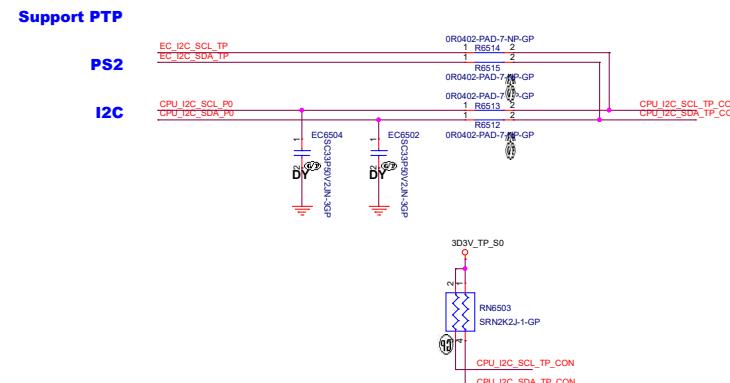
I2C

CPU_I2C_SDA_P0

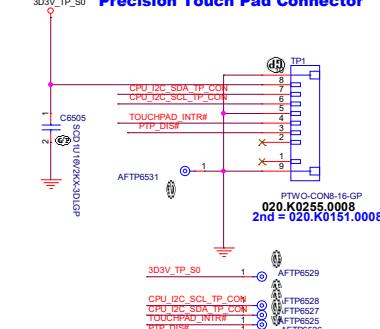
CPU_I2C_SCL_P0

CPU_I2C_SDA_TP

CPU_I2C_SCL_TP

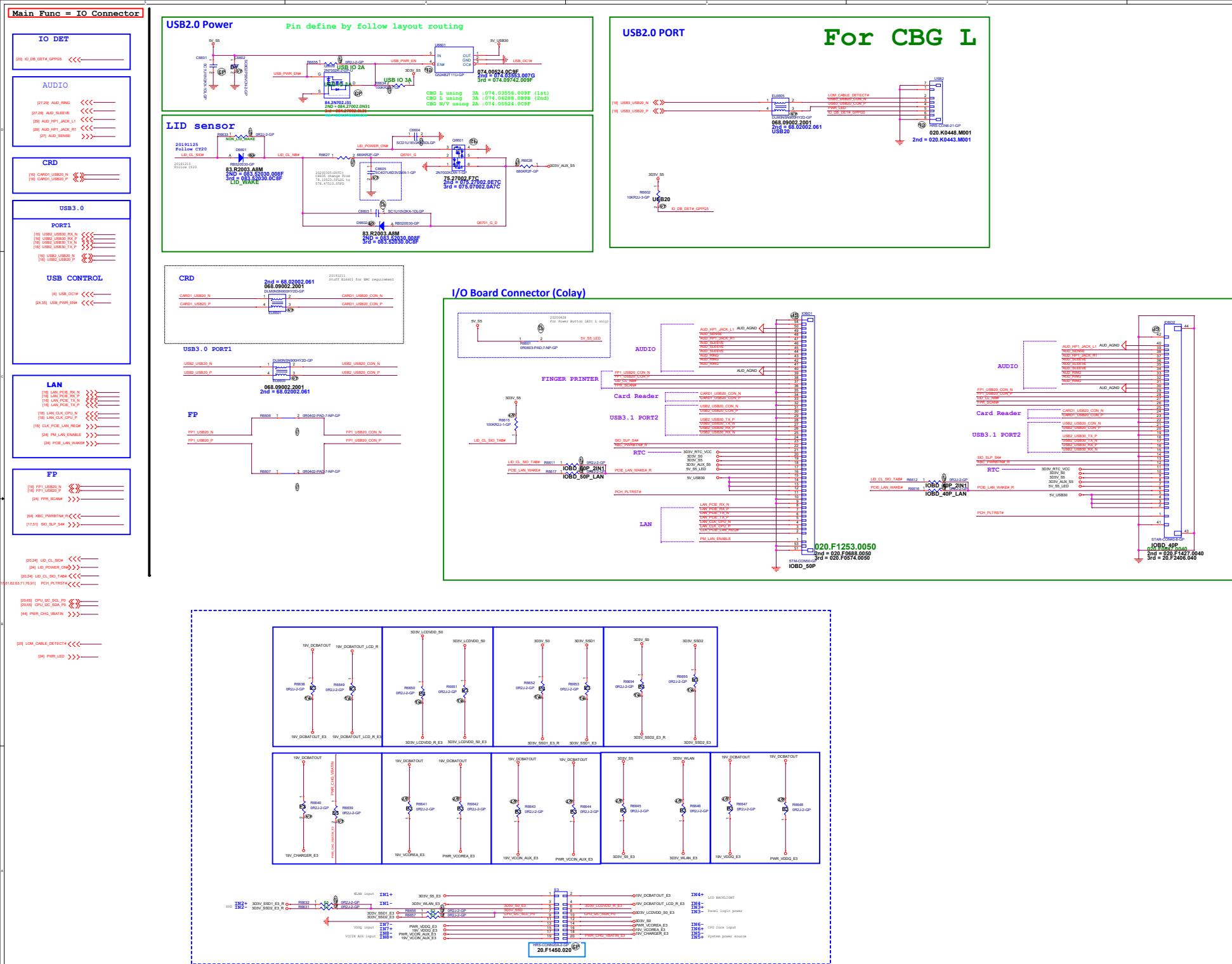


Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CIR(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>



Main Func = HALL SENSOR

D

D

c

C

B

B

A

A

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size A3	Document Number
Rev SC	Cyborg TGL

Main Func = Debug

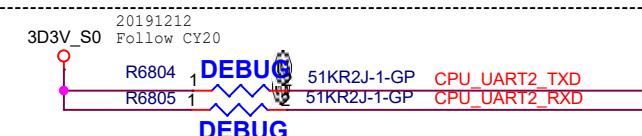
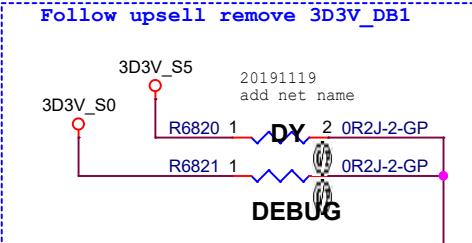
ESPI

[18,24] ESPI_CLK >>> _____
 [18,24] ESPI_RESET# >>> _____
 [18,24] ESPI_CS# >>> _____

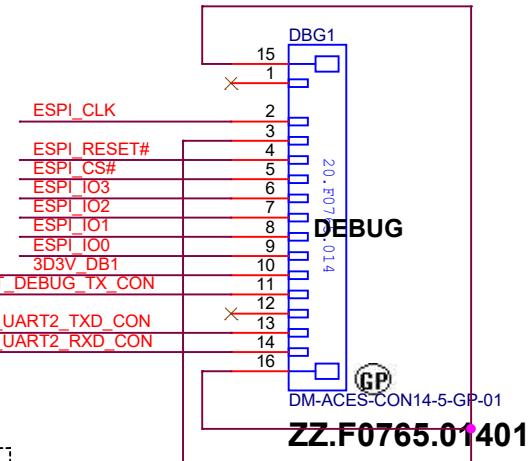
[18,24] ESPI_IO0 <<< _____
 [18,24] ESPI_IO1 <<< _____
 [18,24] ESPI_IO2 <<< _____
 [18,24] ESPI_IO3 <<< _____

UART

[24] HOST_DEBUG_TX >>> _____
 [20] CPU_UART2_TXD >>> _____
 [20] CPU_UART2_RXD <<< _____



ESPI Debug Connector



<Core Design>



Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size A4 Document Number

Cyborg TGL

Rev SC

Date: Thursday, January 14, 2021

Sheet 68 of 105

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Rev
SC

Cyborg TGL

Date: Thursday, January 14, 2021

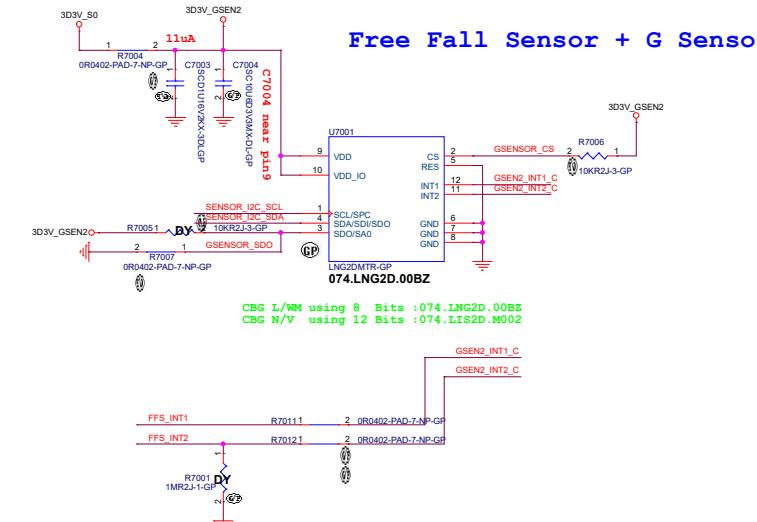
Sheet 69 of 105

SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

The slave address (SAD) associated with the **LNG2DM** is 010100b. The **SDO/SAO** pad can be used to modify the least significant bit of the device address. If the **SAO** pad is connected to a voltage supply, **LSB** is '1' (address 0101001b), or, if the **SAO** pad is connected to ground, the **LSB** value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

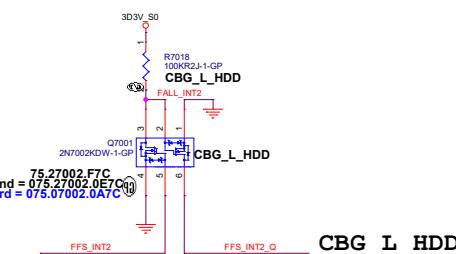
```
[20] GSEN2_INT1_C <<<_____
[20.55] SENSOR_I2C_SCL <>>_____
[20.55] SENSOR_I2C_SDA <>>_____
[20] FFS_INT1 <<<_____
[19] FFS_INT2 <<<_____
[60] FFS_INT2_Q <<<_____
```



CBG L/WM using 8 Bits :074.LNG2D.
CBG N/W using 12 Bits :074.LIS2D.

No

- no via, trace, under the sensor (keep out area around 2mm)
 - stay away from the screw hole or metal shield soldering joints
 - design PCB pad based on our sensor LGA pad size (add 0.1mm)
 - solder stencil opening to 90% of the PCB pad size
 - mount the sensor near the center of mass of the NE as possible as you can

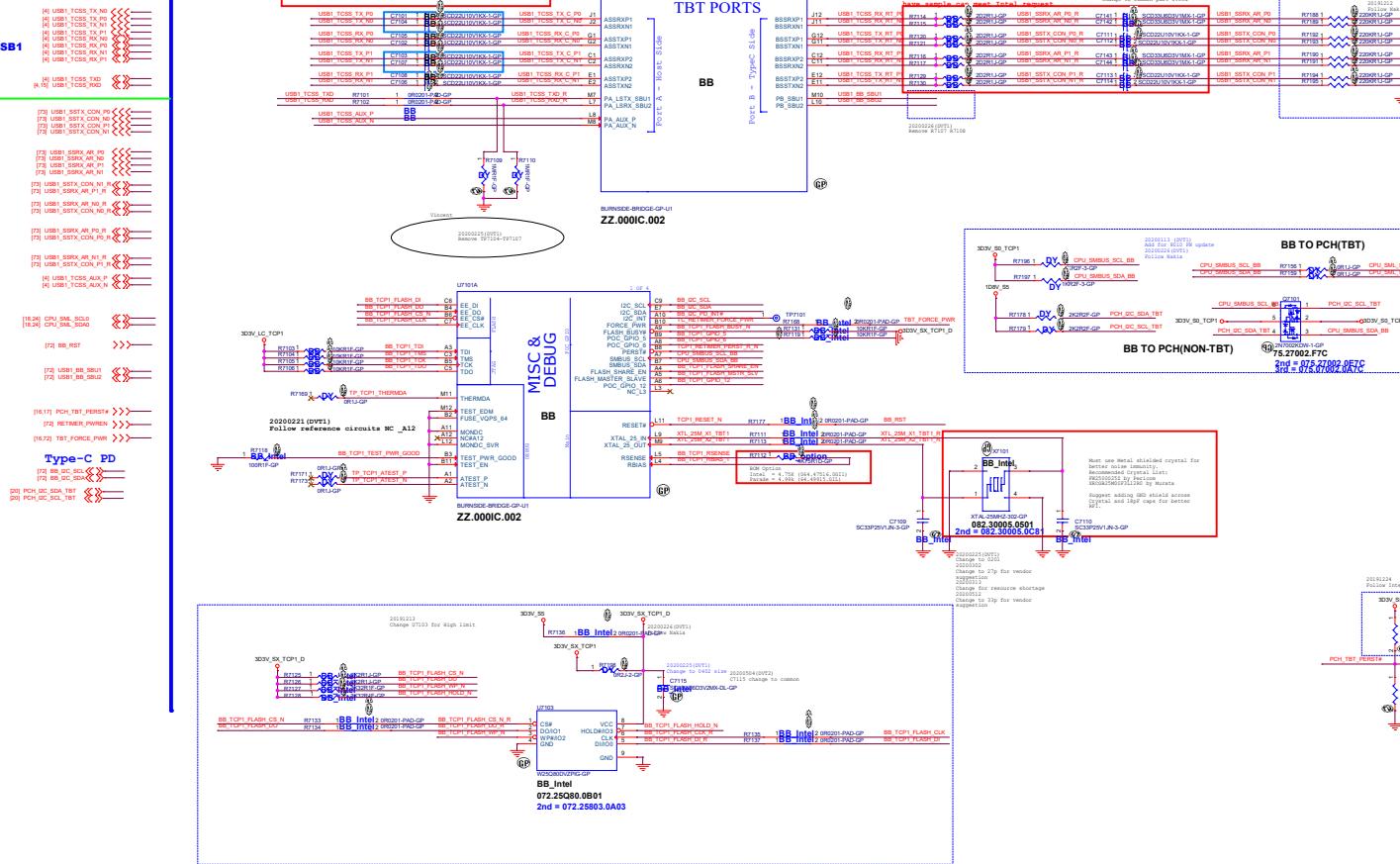


N

- NOTE:**

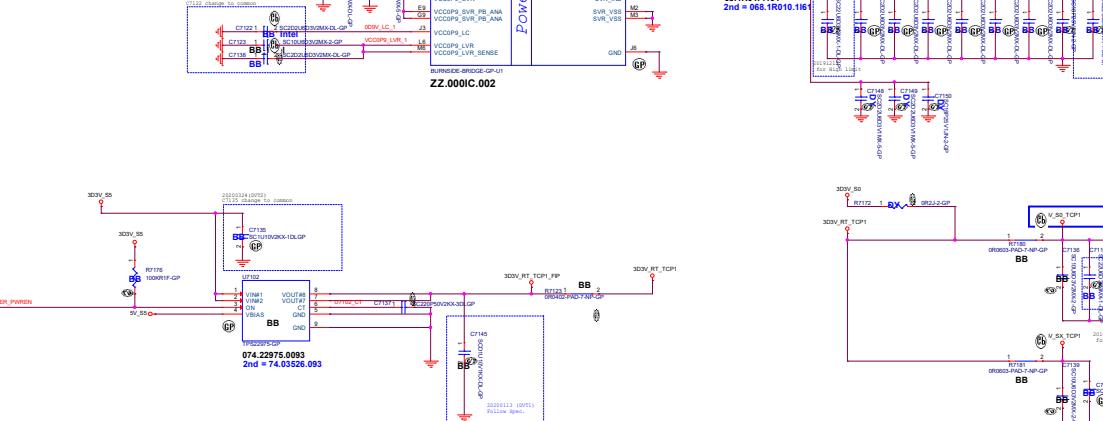
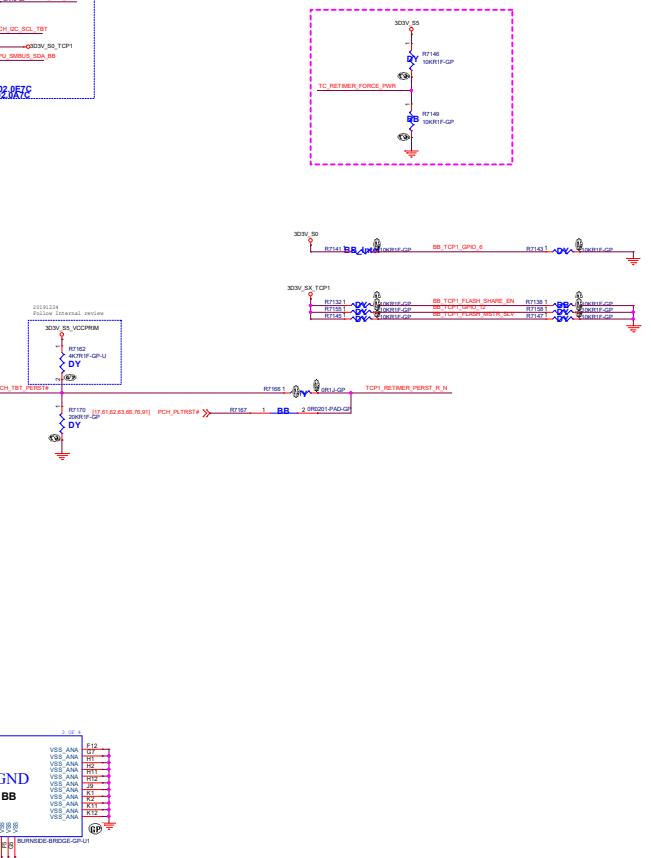
 - (1) Keep all signals are the same trace width. (included VDD, GND).
 - (2) No VIA under IC bottom.

Main Func = TBT



Follow Hellcat15 Upsell TGI

	WPN	DPN
TBT	071.00TBT.0FOU	M11GX
NON_TBT	071.00TBT.0DOU	7DYVG



Follow Hellcat15 Upsell TGI

Main Func = TypeC

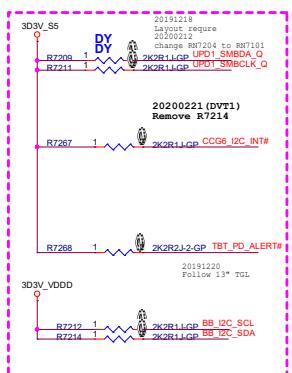
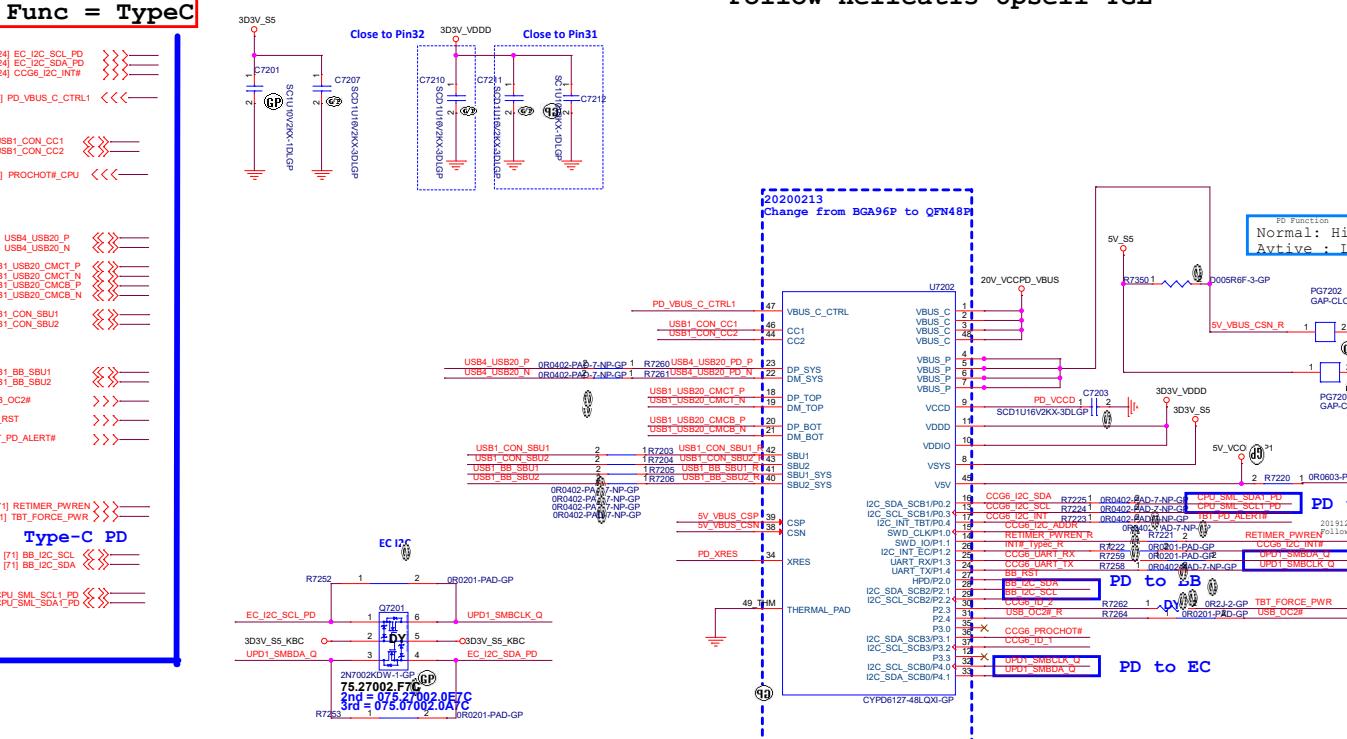
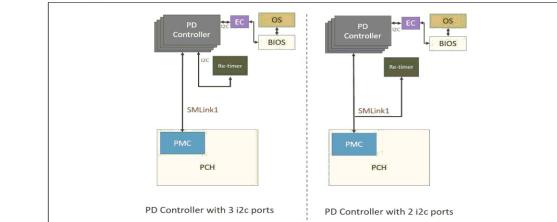
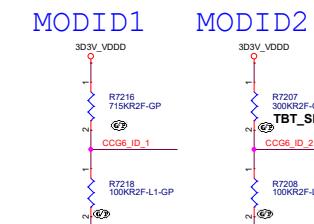


Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



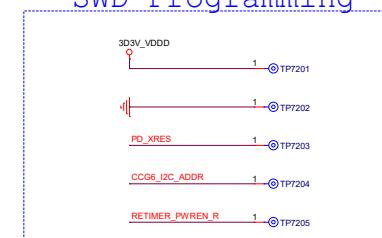
MODID Setting



SWD Programming

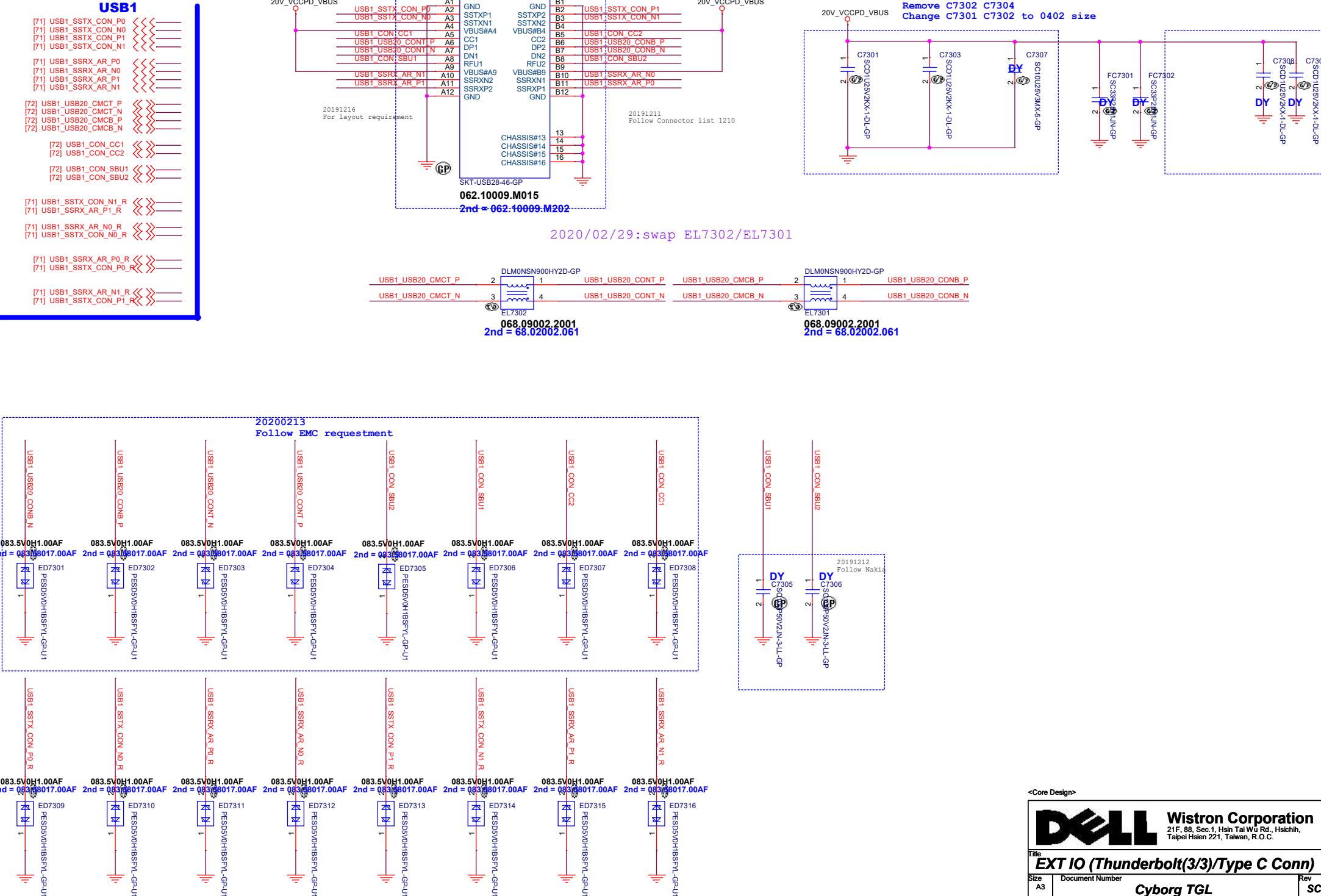
Dell TGL Platform MOD_ID Options NEW			
Project	MOD_ID1	MOD_ID2	Description
Hellcat 8040	L0	N/A	BB8040(Special for Hellcat)
Hellcat 8010	L2	N/A	BB8010(Special for Hellcat)
Moonknight N/V	L1	L0	TGL-U//BB8040//CCG6DF//SOC address 0x21 for
Cyborg TGL-U-8040	L1	L2	TGL-U//BB8040//CCG6SF
Moonknight L			
Cyborg TGL-U-8010			
Watchman	L1	L1	TGL-U//BB8010//CCG6XF
	L3	L0	TGL-H//BB8040//CCG6DF
Stradale MLK	L3	L1	TGL-H//Cascade-BB8040//CCG6DF
Cyborg-TGL-H	L3	L2	TGL-H//BB8040//CCG6SF
	L3	L3	TGL-H//No RT application//CCG6SF
	L4	L0 - L2	PS8802(MFDP)

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.123
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

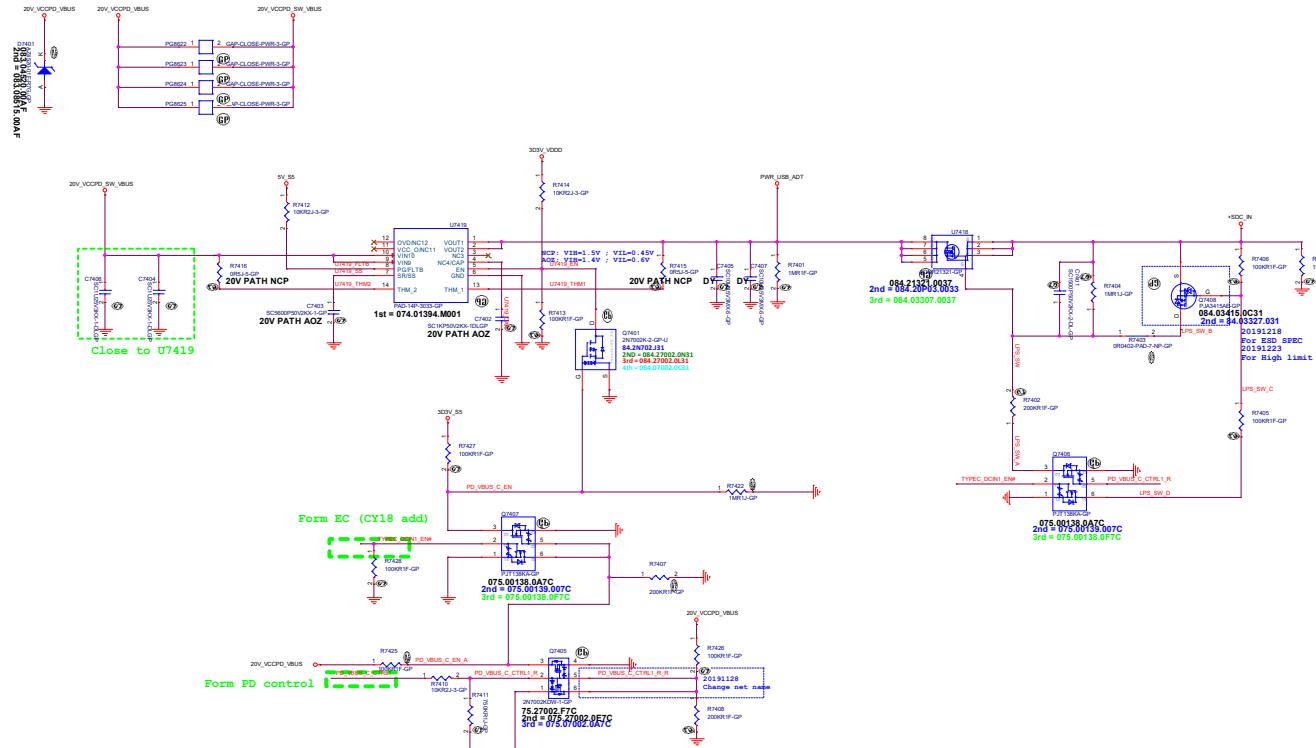


<Core Design>		
 Wistron Corporation 21F, 88, Sec. 1, Hein Tai Wu Rd., Hsinchih, Taipei Hsien 221, Taiwan, R.O.C.		
Title EXT IO (Thunderbolt(2/3)/Type C CC Logic)		
Size A2	Document Number SC	Rev. Ref.
Cyborg TGL		
Date: Thursday, January 14, 2021		Sheet 72 of 105

Main Func = TypeC

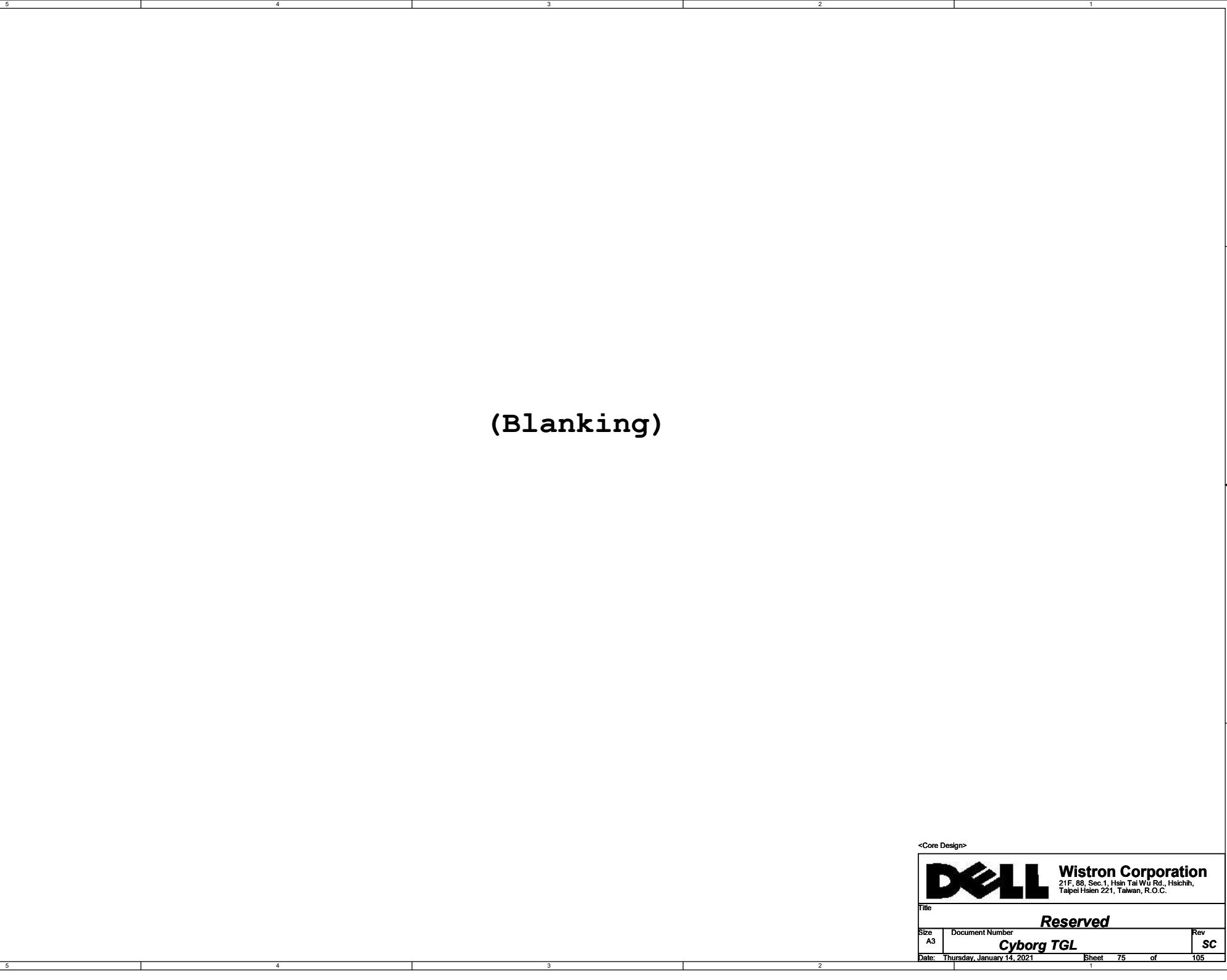


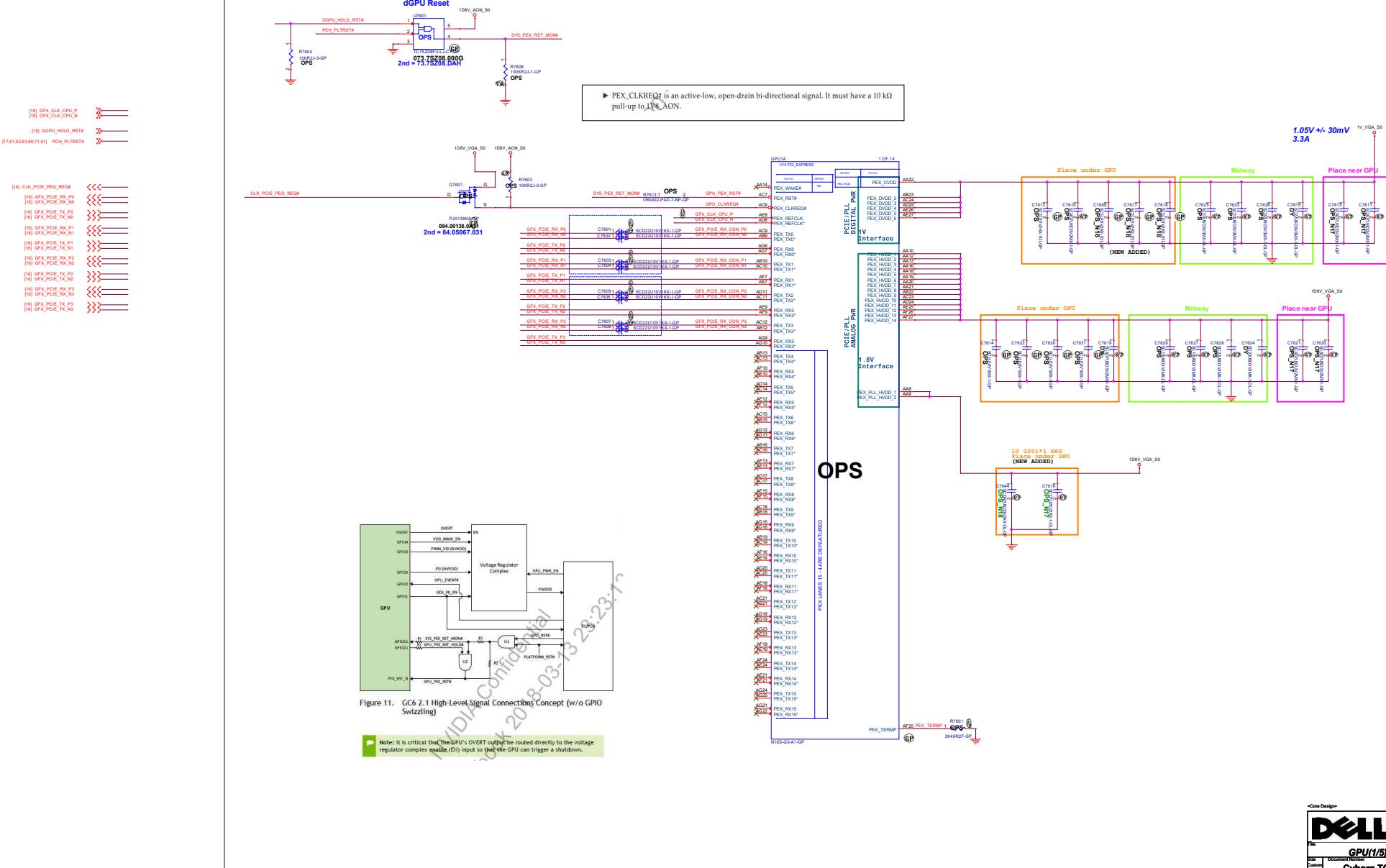
```
[72] PD_VBUS_C_CTRL1 >>>  
[24] TYPEC_DCIN1_EN# >>>  
[44] U7412_FLTB >>>
```



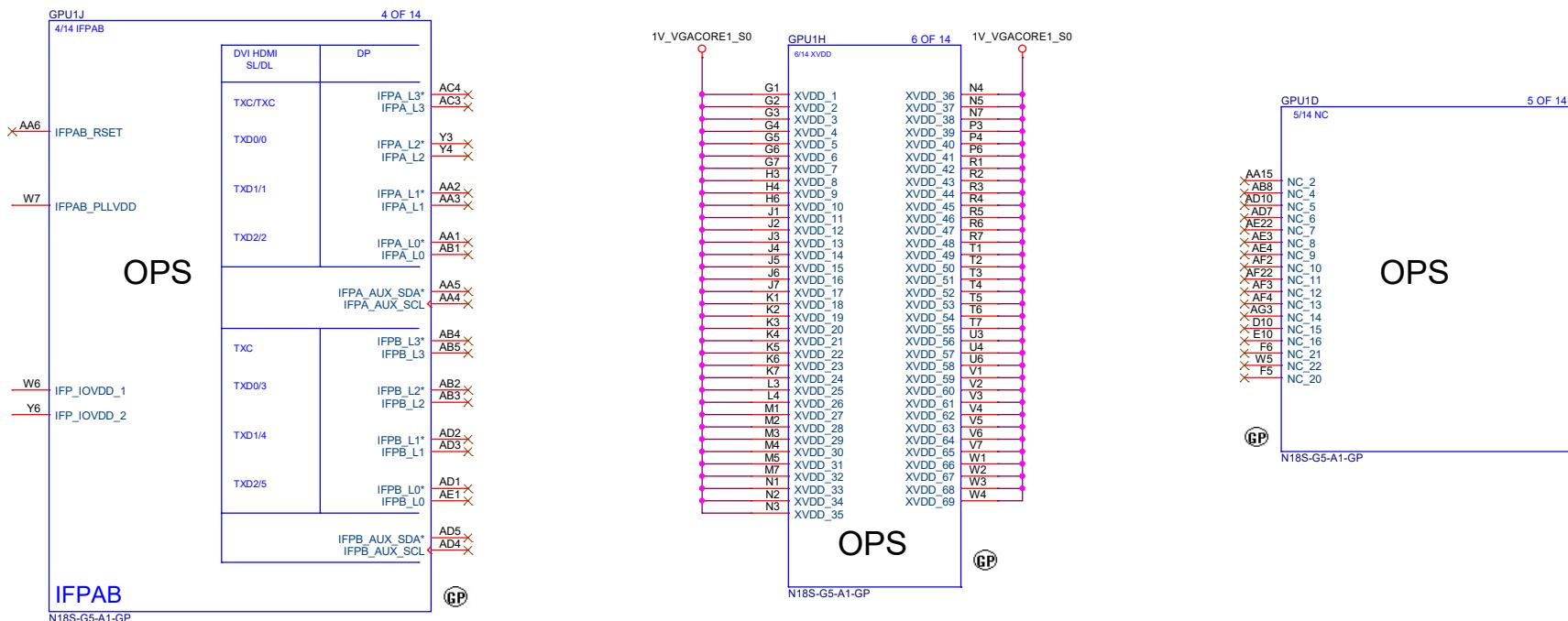
(Blanking)

<Core Design>		
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size A3	Document Number Cyborg TGL	Rev SC
Date: Thursday, January 14, 2021		Sheet 75 of 105





Main Func = dGPU



<Core Design>

DELL	Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
GPU(2/5)DIGITALOUT	
Title _____	
Size A3	Document Number Cyborg TGL
Rev SC	
Date: Thursday, January 14, 2021	Sheet 77 of 105

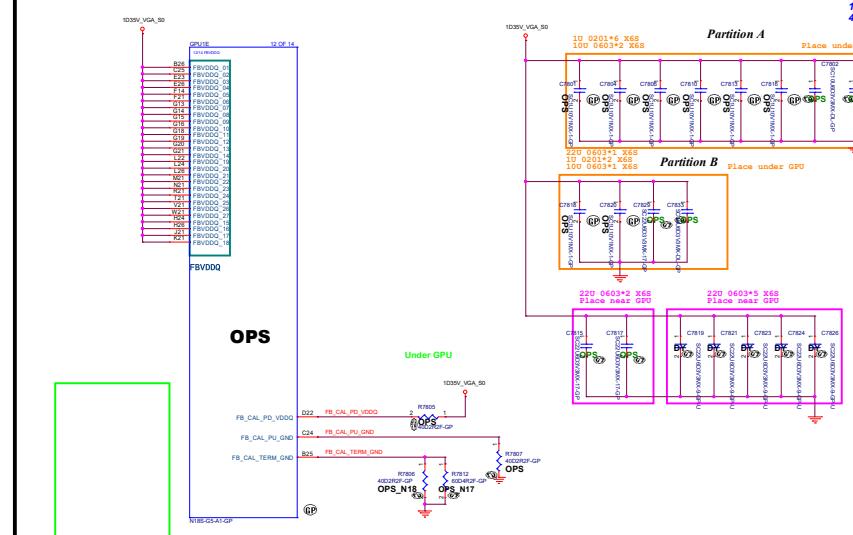
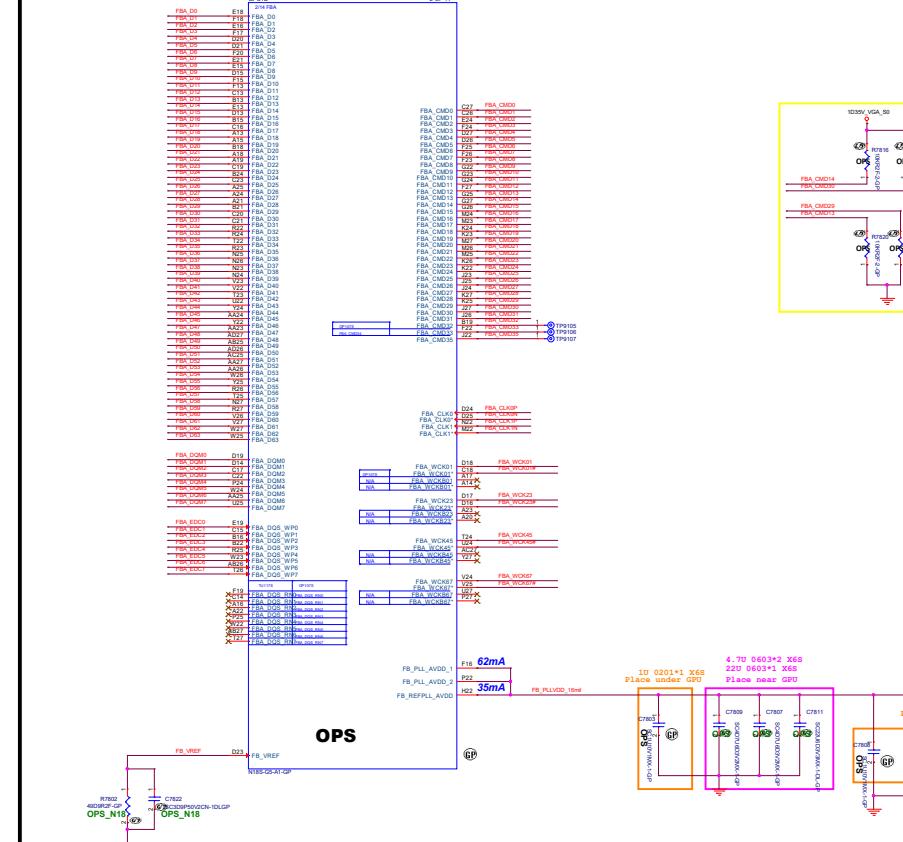
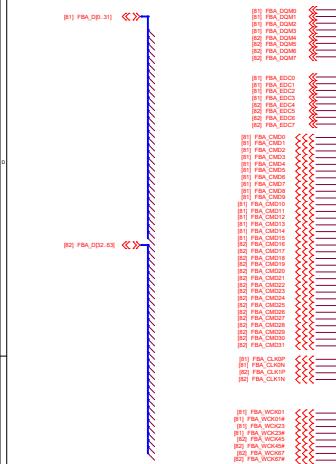


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Population		Location	
		Footprint	N16	N17	
FBVDD/Q Supply Rail for GDDR5					
GB2B-64	0.1 μ F	X7R	0402	2	0 Under GPU
GB2C-64	1 μ F	X7R	0603	2	8 Under GPU
	4.7 μ F	X6S	0603	2	0 Under GPU
	10 μ F	X6S	0603	0	2 Under GPU
	10 μ F	X6S	0603	1	1 Near GPU
	22 μ F	X6S	0603W	1	3 Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Population		Location	
		Footprint	N16	N17	
FB PLL Supply Rail for GDDR5					
GB2B-64	0.1 μ F	X7R	0402	2	4 Under GPU
GB2C-64	22 μ F	X6S	0805	1	1 Near GPU
Bead Type					
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

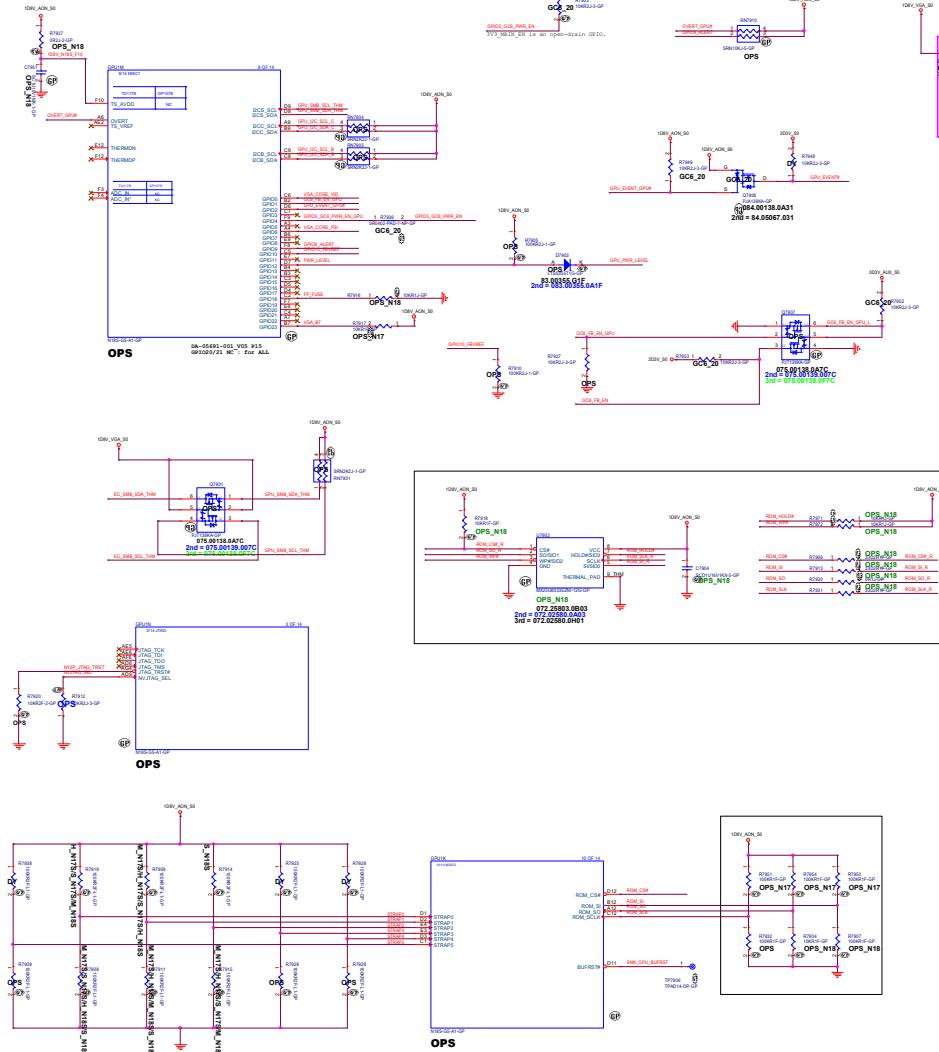


Table 5.2 RAMCFG	
Strap Pins see Note	RAMCFG Setting Number (see Memory RVL for memory config corresponding to these numbers)
L L L	0 (0x0000)
L L H	1 (0x0001)
L H L	2 (0x0002)
H L L	3 (0x0003)
H L H	4 (0x0004)
H M L	5 (0x0005)
H M H	6 (0x0006)
H H L	7 (0x0007)
L L M	8 (0x0008)
L M L	9 (0x0009)
L M H	10 (0x000A)
L H M	11 (0x000B)
M L L	12 (0x000C)
M L H	13 (0x000D)

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs						
Row Index	Strap Pin	See Note	ROM_SI	ROM_SO ¹	ROM_CLK	SOR3_EXPOSED
15	STRAP1		L	L	L	ENABLED
14	STRAP1		L	L	L	ENABLED
13	STRAP1		L	H	L	ENABLED
12	STRAP1		L	H	H	ENABLED
B	STRAP1		H	H	H	ENABLED
0	ROM_SI		M	X	X	(Reserved; do not configure)
						(Reserved)
All other Strap Configurations						

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function		
ROM_SO see Note 2	ROM_SI	ROM_SCLK	SOR1_EXPOSED	SOR2_EXPOSED	SOR3_EXPOSED
L	L	L	0	0	0

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Functions Selected by This Strapping							
Strap Pins See Note	STRAP1	STRAP2	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
	L	L	L	0	0	0	0

Table 13. N185G5 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBDQ/DQ	Vendor	Manufacturer Part Number	Die Revision	Die Type	Memory Speed Grade	Deg Code Alert	Qual Plan	Status
8 Go	256Mx32 512Mx16	1.3V	Micron	MT51256M32HF-80.B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC6H24LJR-RC2	A-die	0x2	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80125F-HC25	C-die	0x1	8 Gbps	N/A	Full	Production candidate

Notes:

1. For H185G5, the maximum allowable memory case temperature is 85 °C.

Table 4. N175-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBDQ/DQ	Vendor	Manufacturer Part Number	Die Revision	Die Type	Memory Speed Grade	Deg Code Alert	Qual Plan	Status
8 Go	256Mx32 512Mx16	1.3V	Hynix	H5GC6H24LJR-RC2	A-die	0x4	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80125F-HC25	C-die	0x4	8 Gbps	N/A	Full	Production candidate

Notes:

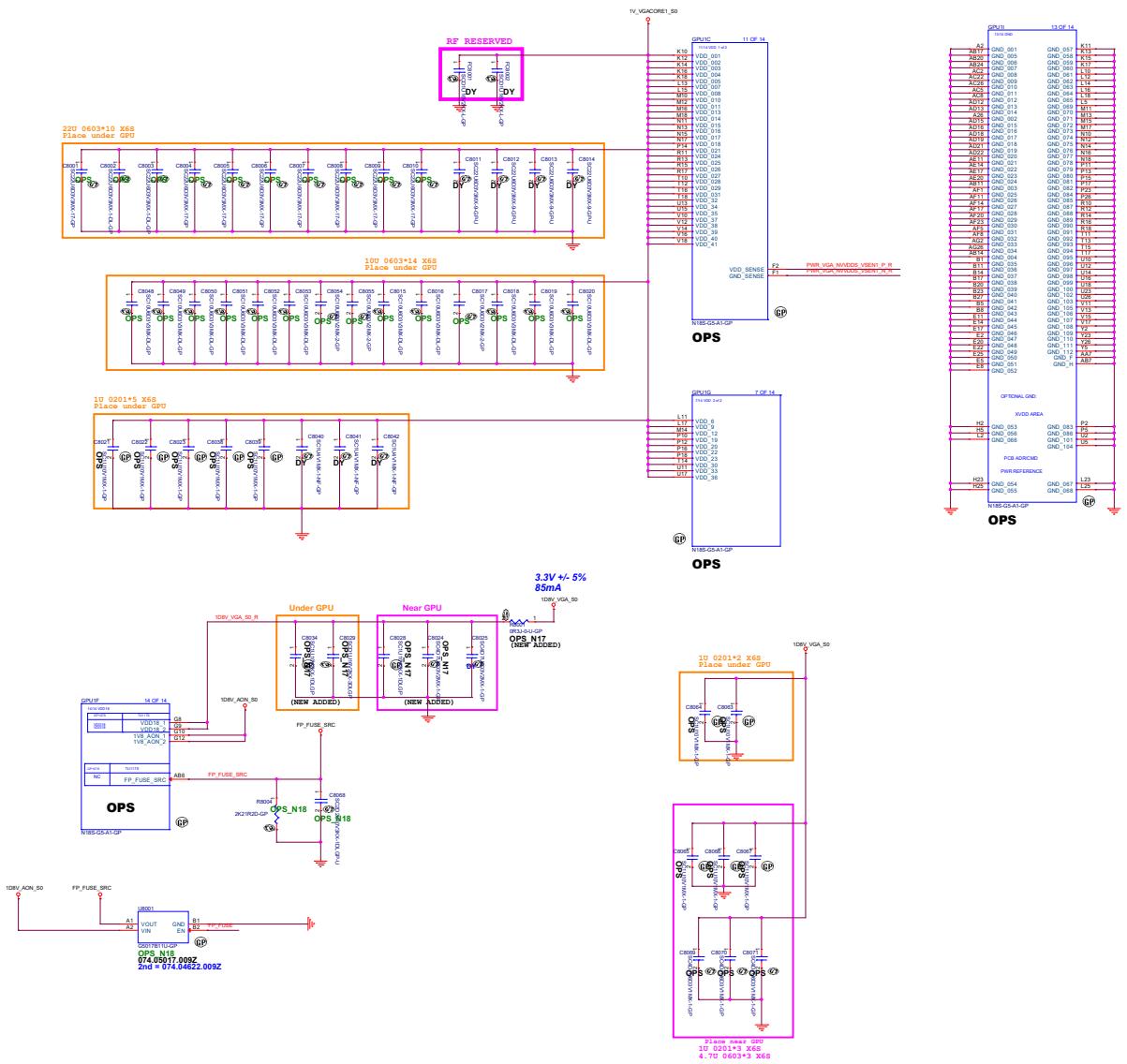
1. For H175-G5/LP, the maximum allowable memory case temperature is 85 °C.

Strap Pin	N18/GB2E-64
ROM_SI	Pull low to enable FS_OVERT*
ROM_SO ¹	
ROM_CLK	
STRAP5	
STRAP4	
STRAP3	
STRAP2	
STRAP1	
STRAP0	

Note:

The ROM_SO pin should be pulled low using a 10 kΩ resistor for N18/GB2E-64 GPUs and using a 100 kΩ resistor for N17/GB2D-64/GB2C-64 GPUs.

Main Func = dGPU



SSID = VRAM

[78.81] FBA_CMD6
 [78.81] FBA_CMD11
 [78.81] FBA_CMD7
 [78.81] FBA_CMD9
 [78.81] FBA_CMD2
 [78.81] FBA_CMD10
 [78.81] FBA_CMD3
 [78.81] FBA_CMD1
 [78.81] FBA_CMD8
 [78.81] FBA_CMD15
 [78.81] FBA_CMD4
 [78.81] FBA_CMD12
 [78.81] FBA_CMD0

[82] FBA_VREFC0 >>

[78] GPIO10_FBVREF >>

[78.81] FBA_CMD13 >>

FBA_D[0..31] [78.81]

FBA_D[0..31] [78.81]

[78.81] FBA_CMD10
 [78.81] FBA_CMD7
 [78.81] FBA_CMD11
 [78.81] FBA_CMD1
 [78.81] FBA_CMD3
 [78.81] FBA_CMD12
 [78.81] FBA_CMD8
 [78.81] FBA_CMD15
 [78.81] FBA_CMD4
 [78.81] FBA_CMD12
 [78.81] FBA_CMD0

FBA_D[0..31] [78.81]

FBA_D[0..31] [78.81]

FBA_DQ00
 FBA_DQ01
 FBA_DQ02
 FBA_DQ03

FBA_ED0
 FBA_ED1
 FBA_ED2
 FBA_ED3

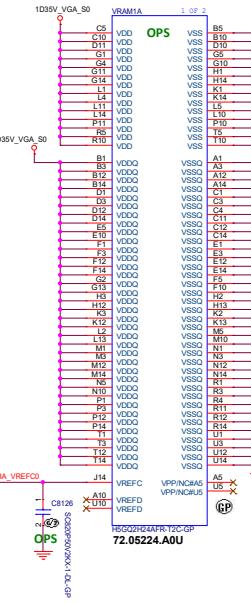
FBA_WK03
 FBA_WK02
 FBA_WK01#

FBA_CMD14 >>

FBA_CMD13 >>

[17.27.40.55] SIO_SLP_S3# <<<

[27] 10BV_En# >>

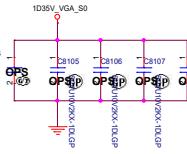


Frame Buffer Partition A-Lower Half

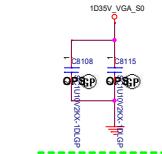
FBVREF Termination			
Type	FBVREF%	Voltage	GPU.GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

75.27002.FTC
 2nd = 075.27002.0ETC
 3rd = 075.27002.0A7C

Place close VDD ball



Place close VDD ball

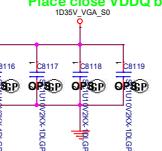


Place close VDD ball



NEW ADDED

Place close VDDQ ball



Normal(MF=0)

VRAMIB		2 of 3	
FBA_CMD6	K4	A8/A7	OPS
FBA_CMD11	H5	A9/A1	
FBA_CMD10	H6	A10/A0	DQ1
FBA_CMD9	K5	A11/A1	DQ2
FBA_CMD8	J6	A12/R1/U1/S1/CALU	DQ3
FBA_CMD2	H11	BAA/A2	F4
FBA_CMD1	H12	BAA/A3	F5
FBA_CMD3	K11	BAA/A4	DQ7
FBA_CMD0	H10	BAA/A3	A11
FBA_DQ0	J4		A13
FBA_DQ1	J5	A8/B	DQ10
FBA_DQ0	J6	RAS#I	B13
FBA_DQ1	G12	RAS#I	D11
FBA_DQ0	I3	C4#S	D12
FBA_DQ1	I4	C4#S	E13
FBA_DQ0	L10	C4#S	F11
FBA_DQ1	L11	WE#I	D14
FBA_DQ0	J12	WE#I	D15
FBA_DQ1	J13	WE#I	U11
FBA_DQ0	J14	C4#C	T12
FBA_DQ1	J15	C4#C	Y11
FBA_DQ0	J16	C4#E	T13
FBA_DQ1	J17	C4#E	Y12
FBA_DQ0	D2	D8#I	D20
FBA_DQ1	D3	D8#I	M11
FBA_DQ0	D4	D8#I	D22
FBA_DQ1	D5	D8#I	D23
FBA_DQ0	P2	D8#I	L4
FBA_DQ1	P3	D8#I	D24
FBA_DQ0	J2	RESET#I	D25
FBA_DQ1	J3	RESET#I	T2
FBA_SEN0	J10	SEN	D26
FBA_Z00	J11	SEN	N2
FBA_MP1	J12	MF	D30
FBA_WK01	D4	WKC01	D31
FBA_WK01#P	D5	WKC01#P	C7
FBA_WK02	P4	WKC02	ED0
FBA_WK02#P	P5	WKC02#P	ED1
FBA_WK03	P6	WKC03	R13
FBA_WK03#P	P7	WKC03#P	R2

Byte 0

0~7

Byte 1

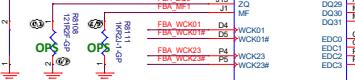
8~15

Byte 2

16~23

Byte 3

24~31



FBA_CLKIP	
BB	402R2F-GP
402R2F-GP	BB

BB_M2_M0_M0T
 402R2F-GP_M2_M0T

<<<

Core Design

Rev

SC

Size

Custom

Date

Thursday, January 14, 2021

Sheet

81

of

105

DELL Wistron Corporation

3F, No. 12, Hsin Hua 2nd Rd., Hsin Chu, Taiwan, R.O.C.

GPU-VRAM1.2 (1/4)

Cyborg TGL

SSID = VRAM

«» FBA_D[32..63] [78.82]

«» FBA_D[32..63] [78.82]

[78.82] FBA_CMD22

[78.82] FBA_CMD27

[78.82] FBA_CMD23

[78.82] FBA_CMD25

[78.82] FBA_CMD18

[78.82] FBA_CMD17

[78.82] FBA_CMD19

[78.82] FBA_CMD17

[78.82] FBA_CMD26

[78.82] FBA_CMD58

[78.82] FBA_CMD31

[78.82] FBA_CMD21

[78.82] FBA_CLKIP

[78.82] FBA_CMD30

[81] FBA_VREFC0 >>

[78.82] FBA_CMD29 >>

«» FBA_D[32..63] [78.82]

[78.82] FBA_CMD26

[78.82] FBA_CMD22

[78.82] FBA_CMD27

[78.82] FBA_CMD25

[78.82] FBA_CMD19

[78.82] FBA_CMD17

[78.82] FBA_CMD20

[78.82] FBA_CMD24

[78.82] FBA_CMD31

[78.82] FBA_CMD21

[78.82] FBA_CMD22

[78.82] FBA_CMD16

[78.82] FBA_CMD30

[78.82] FBA_CMD29

[78] FBA_WK67

[78] FBA_WK49

[78] FBA_WK45

[78] FBA_DOM4

[78] FBA_DOM5

[78] FBA_DOM6

[78] FBA_DOM7

[78] FBA_EDC4

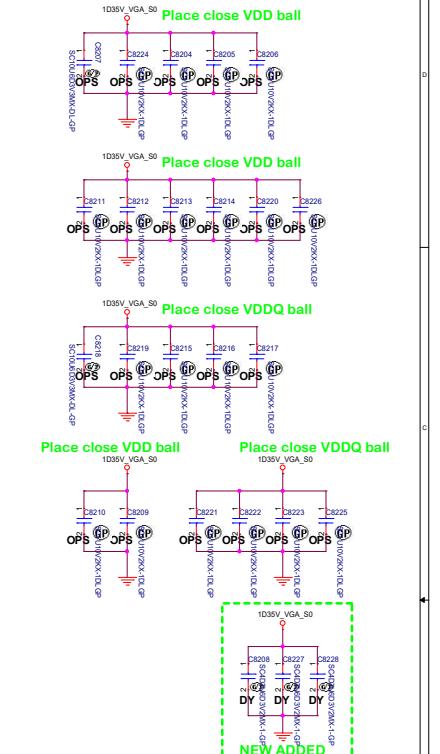
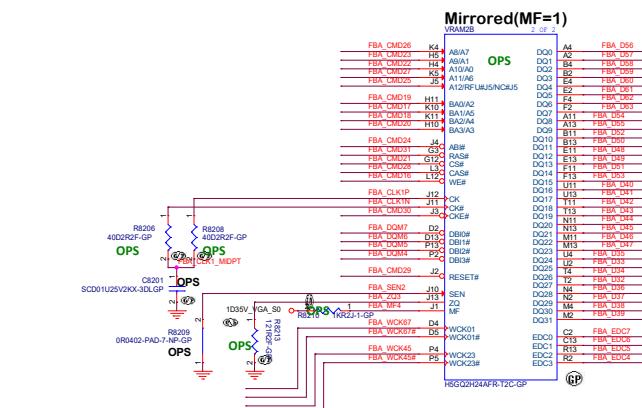
[78] FBA_EDC5

[78] FBA_EDC7

Frame Buffer Partition A-Upper Half

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



D

D

c

C

B

B

A

A

<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GPU-VRAM5,6 (3/4)	
Size A3	Document Number Cyborg TGL
Date: Thursday, January 14, 2021	Rev SC Sheet 83 of 105

D

C

B

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM7,8 (4/4)Size
A4

Document Number

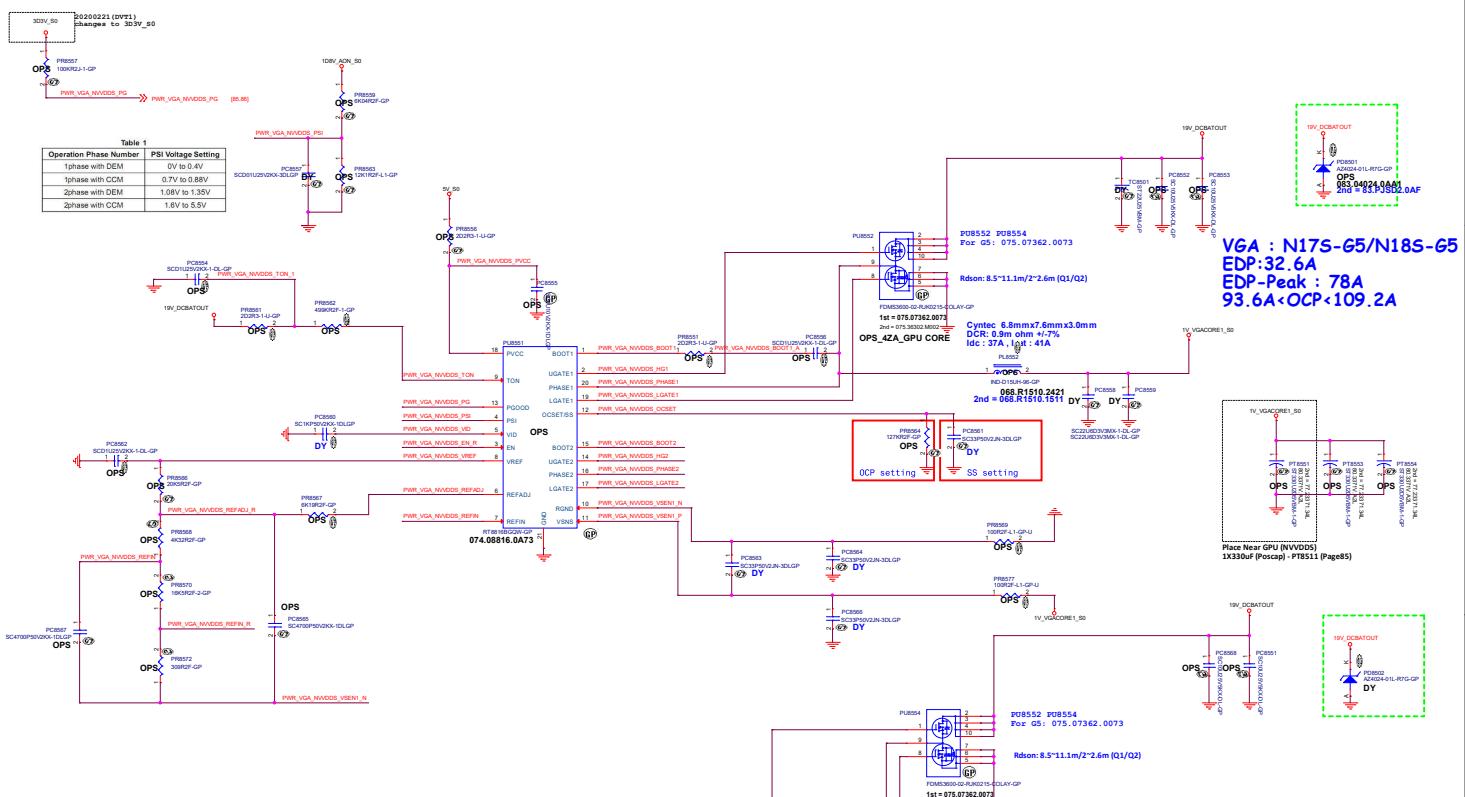
Rev
SC**Cyborg TGL**

Date: Thursday, January 14, 2021

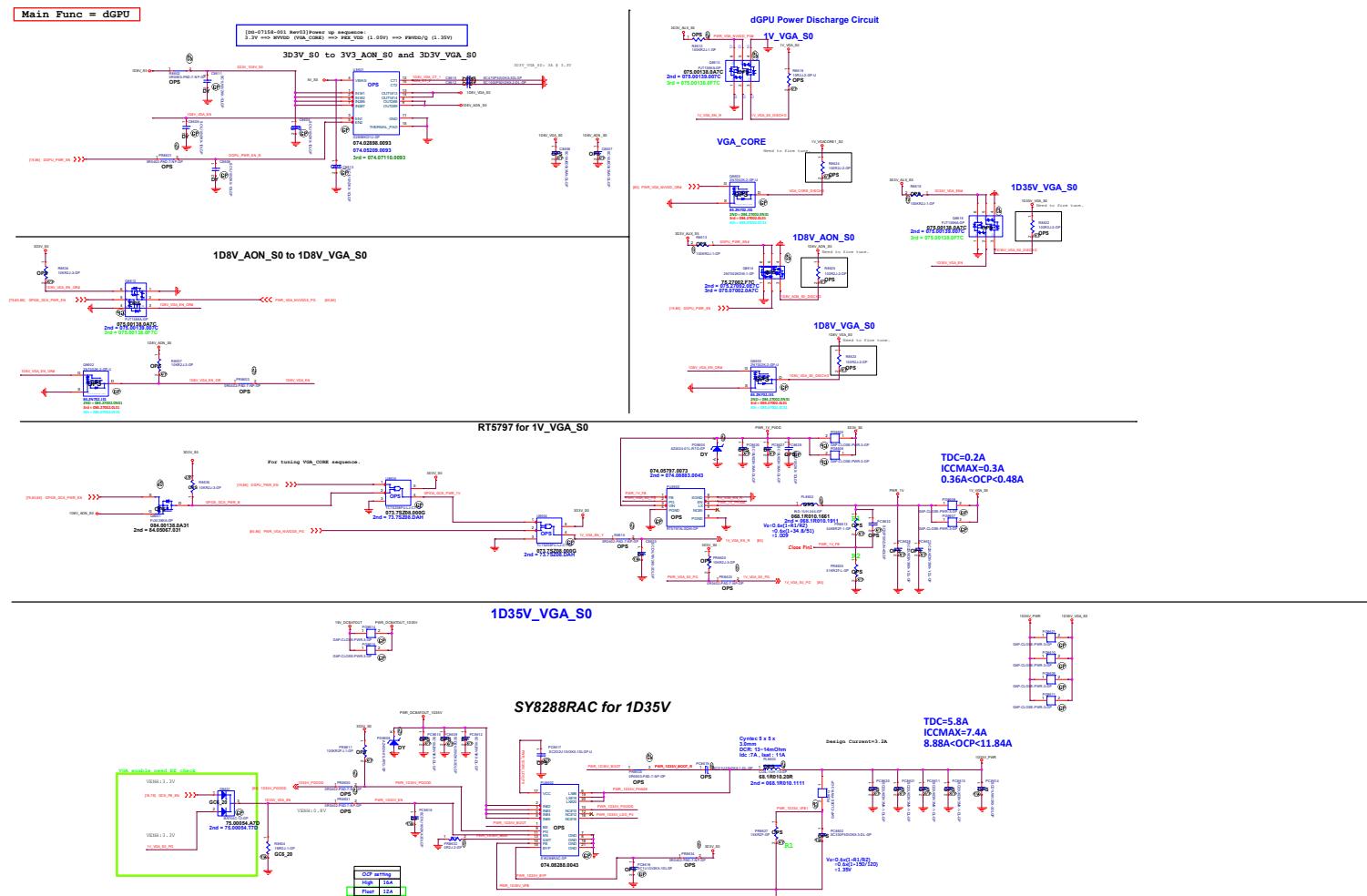
Sheet 84 of 105

RT8816B For NVVDDS

VGA : N17S-G3/G
EDP-Peak : 69.9A



Main Func = dGPU



Main Func = dGPU

D

C

B

A



A

D

C

B

A

(Blanking)

<Core Design>



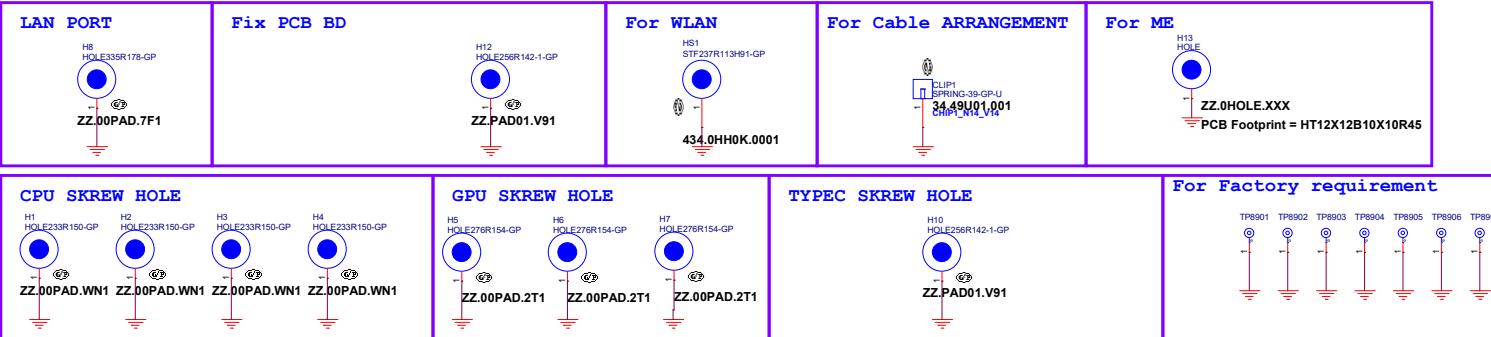
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

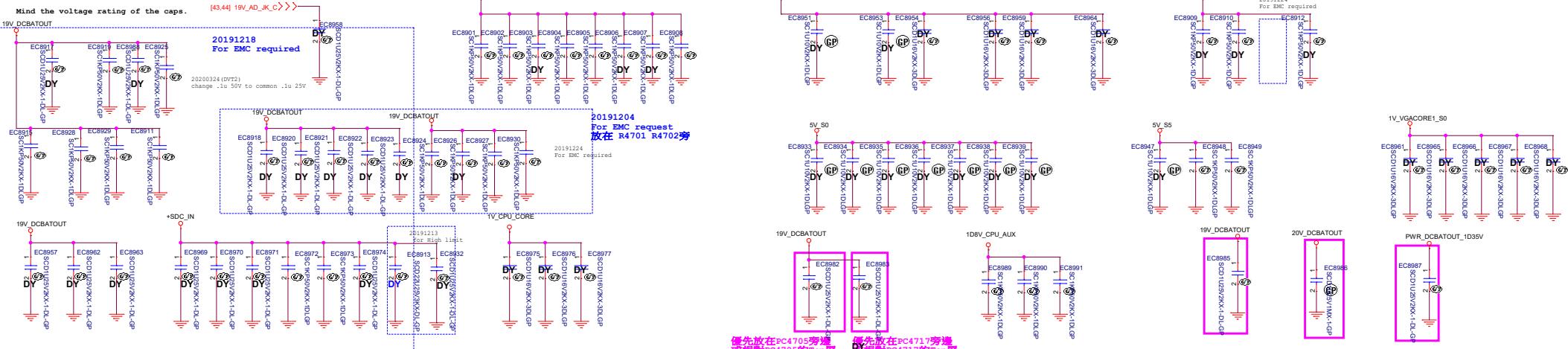
Reserved

Size	Document Number	Rev
A4	Cyborg TGL	SC
Date: Thursday, January 14, 2021	Sheet 88 of 105	

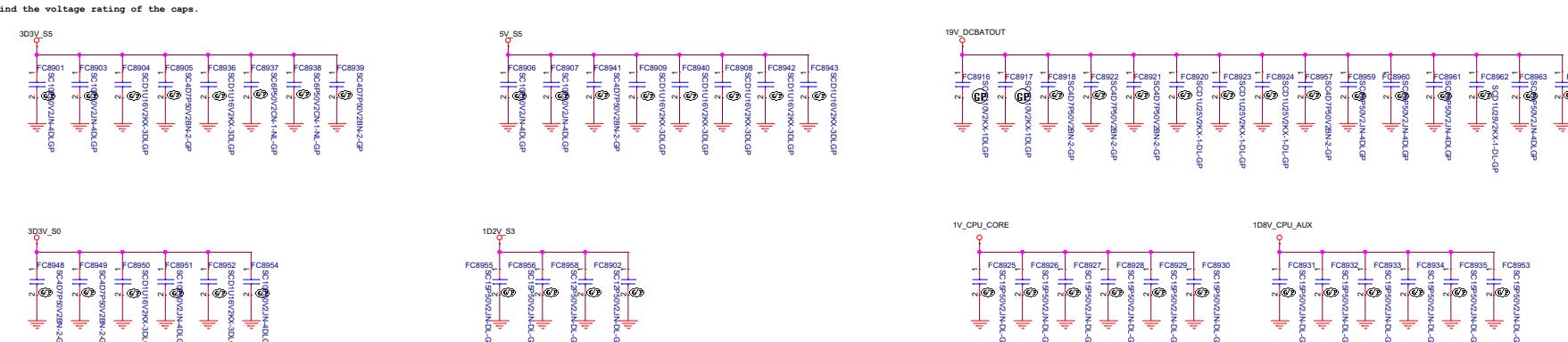
Main Func = UnusedParts



Main Func = EMI Capacitors



Main Func = RF Capacitors



(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

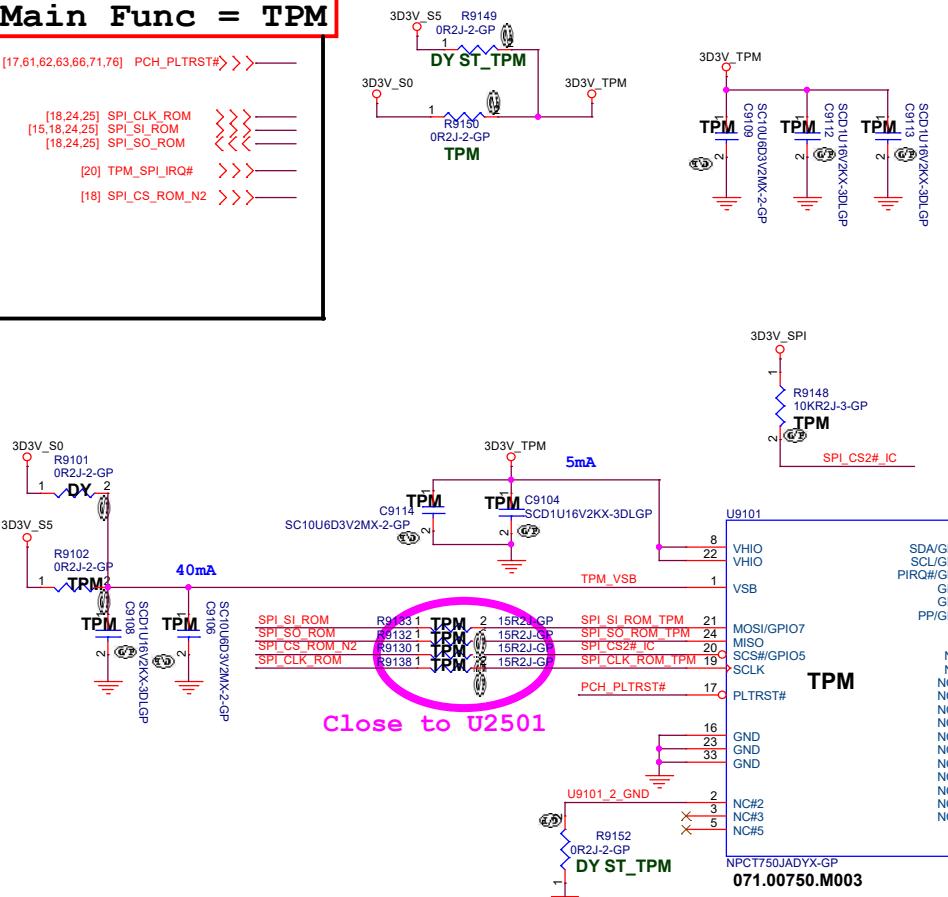
Reserved

Size	Document Number	Rev
A4	Cyborg TGL	SC
Date: Thursday, January 14, 2021	Sheet 90 of 105	

For CBG V/L

Main Func = TPM

[17,61,62,63,66,71,76] PCH_PLTRST#>>>
 [18,24,25] SPI_CLK_ROM
 [15,18,24,25] SPI_SI_ROM
 [18,24,25] SPI_SO_ROM
 [20] TPM_SPI IRQ#>>>
 [18] SPI_CS_ROM_N2>>>



<Core Design>

DELL	Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
INT IO (TPM)	
Size A3	Document Number
	Cyborg TGL
Date: Thursday, January 14, 2021	Rev SC
Sheet 91 of 105	

SSID = Finger Print

5

4

3

2

1

D

D

C

C

→

←

B

B

A

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Finger Print

Size
A4

Document Number

Rev
SC

Cyborg TGL

Date: Thursday, January 14, 2021

Sheet 92 of 105

5

4

3

2

1

(Blanking)

<Core Design>		
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd, Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)		
Size A3	Document Number Cyborg TGL	Rev SC
Date: Thursday, January 14, 2021 Sheet 93 of 105		

(Blanking)

<Core Design>		
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd, Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)		
Size A3	Document Number Cyborg TGL	Rev SC
Date: Thursday, January 14, 2021 Sheet 94 of 105		

(Blanking)

<Core Design>		
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd, Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)		
Size A3	Document Number Cyborg TGL	Rev SC
Date: Thursday, January 14, 2021 Sheet 95 of 105		

20200915
Remove



(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS Switch

Size
A4

Document Number

Cyborg TGL

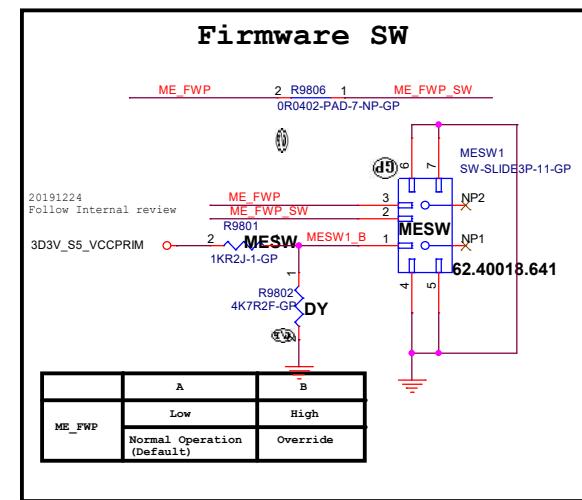
Rev
SC

Date: Thursday, January 14, 2021

Sheet 97 of 105

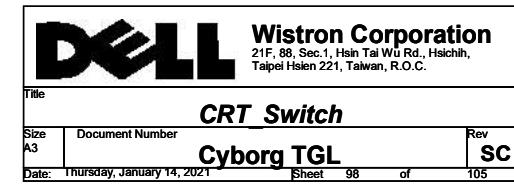
Main Func = Firmware SW

[19] ME_FWP_SW>>
[24] ME_FWP <<



	3	1
ME_FWP	LOW Normal Operation (Default)	HIGH Override

<Core Design>



D

D

C

C

B

B

A

A

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Debug (XDP debug)

Size

Document Number

Rev

A4

Cyborg TGL

SC

Date: Thursday, January 14, 2021

Sheet 99 of 105

5 4 3 2 1

CLK Block Diagram

TBD

<Core Design



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

—
Title

Change History

Size

Cyborg TGL

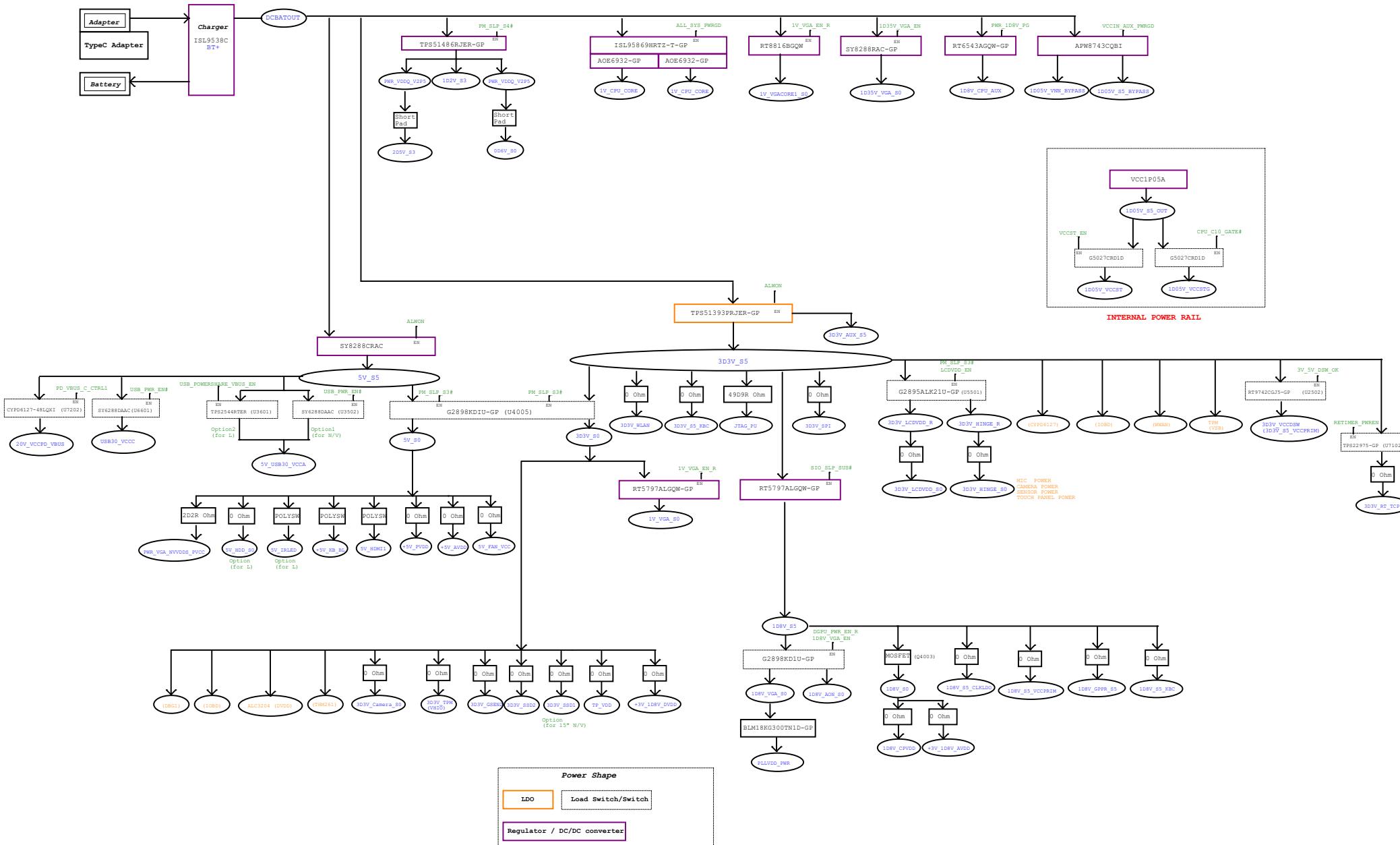
Rev

SC

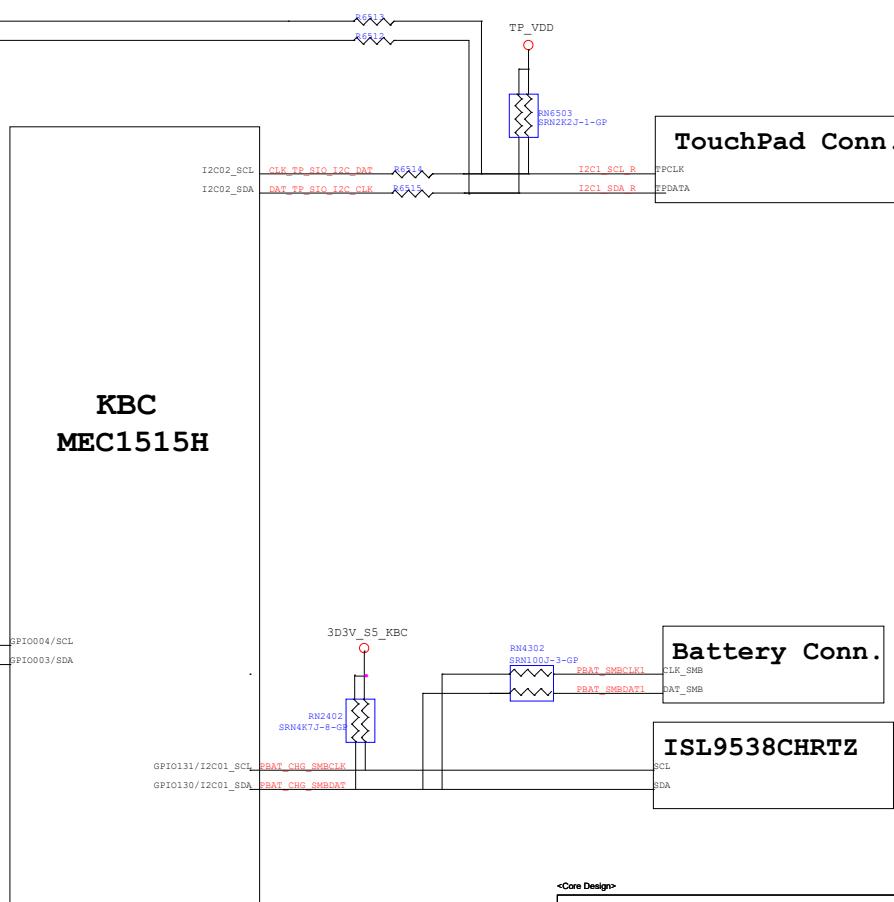
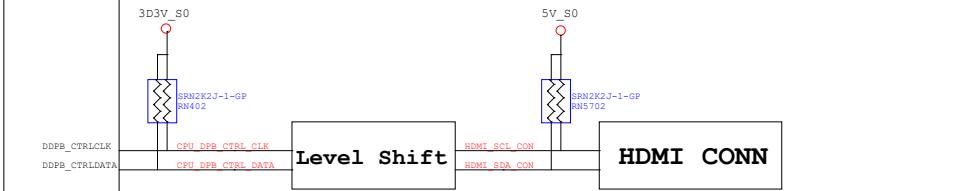
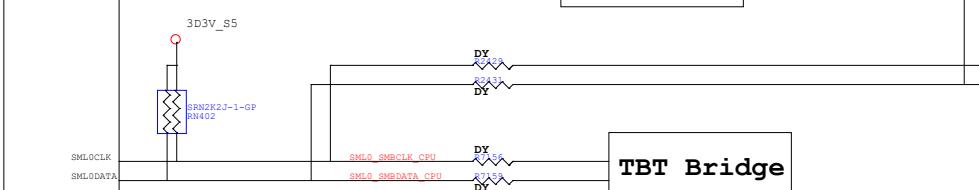
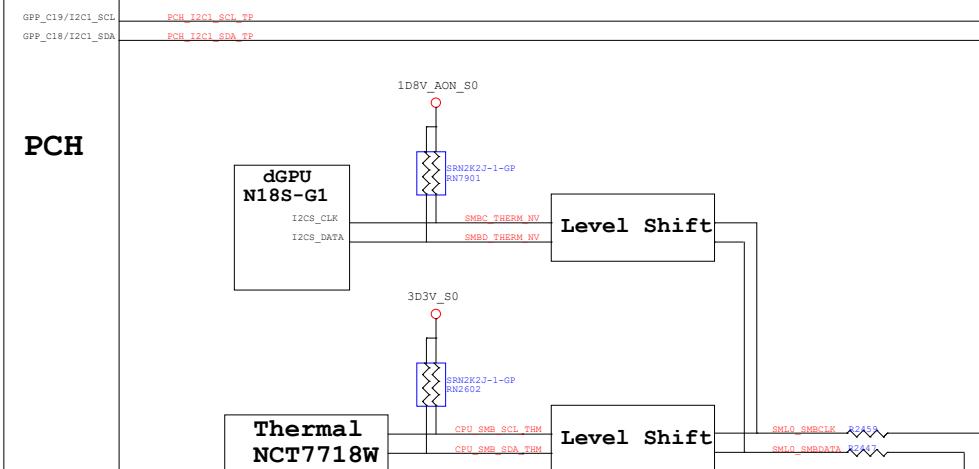
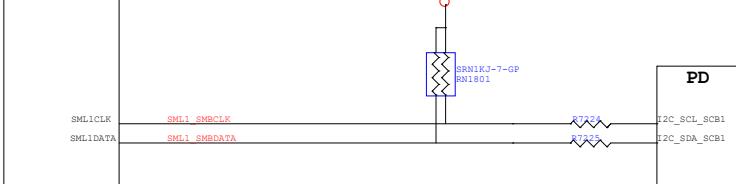
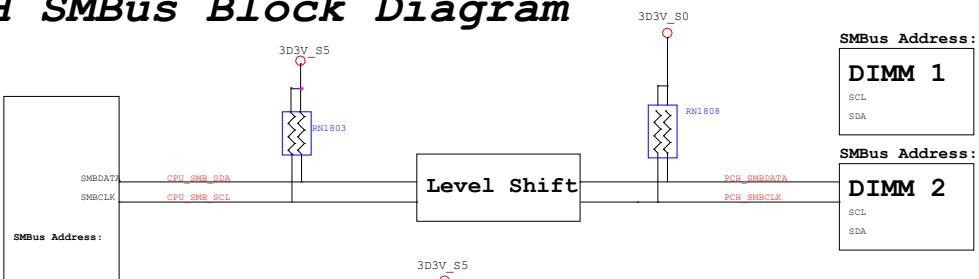
Date: Thursday, January 14, 2021

Sheet 101 of 105

TBD



PCH SMBus Block Diagram



KBC SMBus Block Diagram

Thermal Block Diagram

Audio Block Diagram

