Descriptions

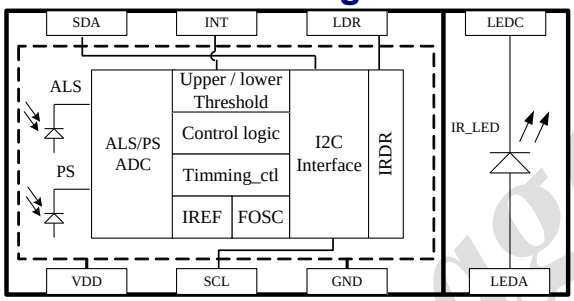
AP3426 is a module integrated with a digital ambient light sensor [ALS], a proximity sensor [PS], and an IR LED in a single package.

This device provides a multiple gain ALS function with linear response over various dynamic ranges 512 / 2048 / 8192 / 32768 Lux and is well suited for applications under clear or darkened glass.

The proximity function is specifically targeted towards near field application and detects external object with simple configurable zone, controlled by registers. With multiple proximity gain control, multiple IR LED current control and 10-bit ADC output, this device is designed specially to fix low reflection objects, such as black hair.

The device supports an interrupt feature to improve system efficiency and several features that help to minimize the occurrence of false triggering. Through internal calibration and CMOS design, the AP3426 is designed to minimize device-to-device variations for ease of manufacturability.

Function Block Diagram



Features

- I²C interface (Fast Speed mode at 400k Hz)
- Mode Select: Ambient Light Sensor (ALS), Proximity Sensor (PS), Power Down (PD), ALS once, PS once, SW Reset.
- Built-in temperature compensation circuit
- Wide operating temperature range (-40°C to +85°C)
- Ambient Light Photo Sensor
  - 16-bit effective linear output (0~65535)
  - 4 user selectable dynamic range
  - Flicker rejection (reject 50/60Hz)
  - High sensitivity at darkened glass
  - Window loss compensation
- Proximity Detector
  - 10 bit effective linear output (0~1023)
  - 4 programmable IR LED current output
  - High ambient light suppression
  - Crosstalk compensation
  - Paired with 940nm IR LED to avoid red light blinding
- RoHS compliant

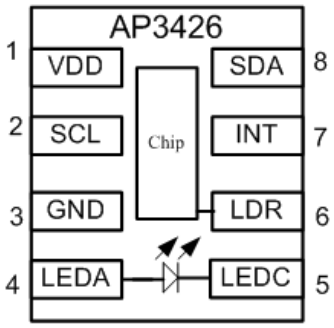
Applications

- Smart phone, Tablet PC, Wearable
- Personal Navigation Device
- Notebook/ Ultrabook
- LCD/PDP TV backlight systems
- Digital Photo Frame
- Applications with Capacitive Touch Panel

Ordering Information

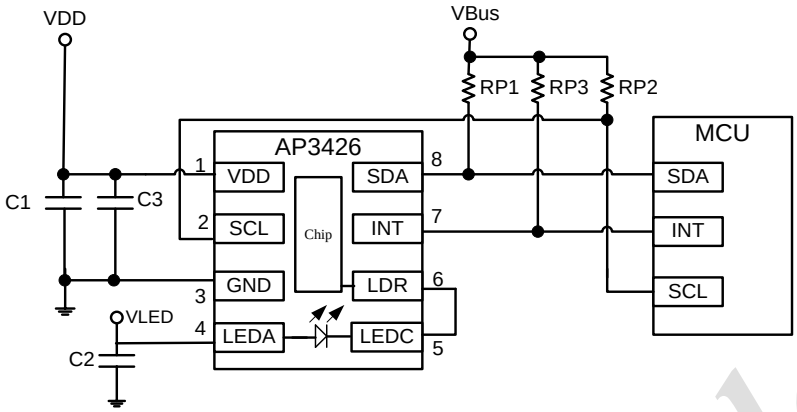
Part No.	Packing Type	Package	Q'ty	Reel Size
AP3426	Tape and Reel (MSL3)	8Ld ODFN 3.94x2.36x1.35mm³	2500	7"
AP3426-3.5		8Ld ODFN-Interposer 4.94x3.36x3.50mm³	1500	13"

Pin Description

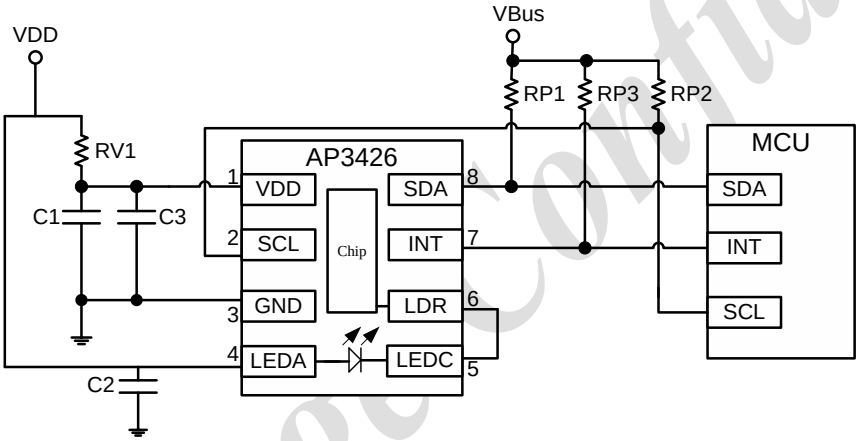


Typical Application Circuit

Two Power Supply Application Circuit Design



Single Power Supply Application Circuit Design



Recommended Application Circuit Components (*1)

Component	Recommended Value	Condition / Range
VLED	Depends on system design, connect to VDD or VBatt	
R_{p1}, R_{p2}	Typical 2.2kΩ, depends on system design	
R_{p3}	Typical 10kΩ, depends on system design	
RV1	Typical 22Ω, depends on IC setting (1)	Only for Single Power Supply Design
C_1	1μF, ±20%	As close as possible to the sensor
C_2	2.2μF, ±20%	As close as possible to the sensor
C_3 (Optional)	0.1μF, ±20%	As close as possible to the sensor

***Note 1: It is highly suggested to have separate power sources for VDD and LED. If LED and VDD power source must be bound together due to design considerations, R/C low pass filter must be utilized to reduce LED to VDD switching noise. RV1 value differs depending on the system power noise level.**

Pin Descriptions

Pin Number	I/O Type	Pin Name	Description
1		VDD	Digital/Analog Power Supply
2	I	SCL	I²C serial clock signal (open drain)
3		GND	Ground
4		LEDA	LED anode
5		LEDC	LED cathode
6	O	LDR	LED driver for proximity emitter
7	O	INT	Interrupt pin
8	I/O	SDA	I²C serial data signal (open drain)

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage 1 Note 1	VDD	+4.5	V
Supply Voltage 2 Note 1	VLED	+5	V
I²C Bus Pin Voltage	SCL, SDA	-0.2 to +4	V
I²C Bus Pin Current	SCL, SDA	+10	mA
ESD Rating, HBM	HBM	4k	V
Storage Temperature	Tstg	-40 to +100	°C
Operating Temperature	Tope	-40 to +85	°C

Note 1: Stresses beyond the ranges listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and are not to be seen as implications of functional operation of the device exceeding the conditions under "Recommended Operating Conditions". Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage Note1	V_{DD}	2.4		3.6	V	
Supply Voltage Note2	V_{LED}	2.4		4.5	V	
I²C Bus Pin Voltage Note3	V_{Bus}	1.7		V_{DD}	V	$V_{Bus} \leqq V_{DD}$
Operating Temperature	T_{ope}	-40		+85	°C	
I²C Bus Input High Voltage Note4	V_{IH_SCL}, V_{IH_SDA}	1.4		V_{DD}	V	
I²C Bus Input Low Voltage Note4	V_{IL_SCL}, V_{IL_SDA}			0.4	V	
I²C Bus Output Pin Low Voltage	V_{OL_SDA}	0		0.4	V	3mA sinking current
		0		0.6	V	6mA sinking current
	V_{OL_INT}	0		0.4	V	3mA sinking current

Notes:

1. To ensure correct initiation of the sensor, VDD slew rate must be at least 0.6V/ms
2. Please refer to Page 2: **Two Power Supply Application Circuit Design** diagram
3. The specs are defined under VDD=2.8V, T=25°C
4. Please refer to **Operation** (page 5)

Electrical & Optical Specifications

All specifications are at VDD=3.3V, Tope=25°C, white light LED, unless otherwise noted.

Parameter		Symbol	MIN	TYP	MAX	Notes	UNIT
Active Supply Current Note1		Idd		170	250	Ev=0, excluding LED current	μA
Active Supply Current Note2		Idd		325		Ev=0, including LED current	μA
Shutdown Current		Ipd		2	5	Ev=0, I²C inactive	μA
Ambient Light Sensor							
Dynamic Range	Range 1			32768		0.5lux/count	lux
	Range 2			8192		0.125lux/count	lux
	Range 3			2048		0.0313lux/count (Default)	lux
	Range 4			512		0.007813lux/count	lux
ALS ADC Count	Range 1		112	128	143	Ev=64lux, white LED	count
	Range 2		450	512	573	Ev=64lux, white LED	count
	Range 3		1802	2048	2294	Ev=64lux, white LED	count
	Range 4		7209	8192	9175	Ev=64lux, white LED	count
Dark Count					5	Ev=0, Range 4	count
Proximity Sensor							
LED Forward Voltage		V_F	1.35	1.55	1.75	I_F=250mA	V
LED Peak Wavelength		λp		940		I_F=20mA	nm
LED Spectral Bandwidth		Δλ		50		I_F=20mA	nm
PS Sensing Full Scale ADC Count (delta value)					1023		count
Proximity ADC count value Note3			366	430	495		count
Proximity Sensing Distance				100			mm
LED Driver Current 100% = 140mA @ Typ.				16.7		IR LED, VOL=1V (Saturation)	%
				33.3		IR LED, VOL=1V (Saturation)	%
				66.7		IR LED, VOL=1V (Saturation)	%
				100		IR LED, VOL=1V (Saturation) Default	%

Notes:

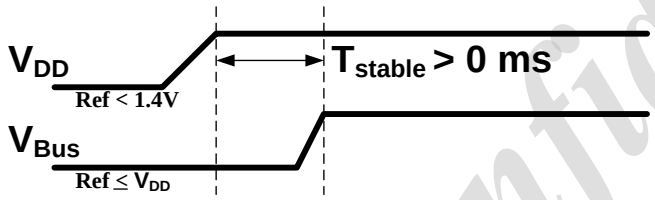
1. The current consumption is tested under 0x00 set 0x01, 0x10 set 0x00, 0x20 set 0x04, 0x21 set 0x03, 0x23 set 0x00 respectively, excluding LED current.
2. The current consumption is tested under 0x00 set 0x03, 0x20 set 0x04, 0x21 set 0x03, 0x23 set 0x00respectively.
3. Test condition : 90% white card at 10cm, register setting register 0x00 set 0x02, 0x20 set 0x04, 0x21 set 0x03, 0x23 set 0x03, and 0x25 set 0x1Eopen view (no glass) above the module.

Operation

Power Sequence

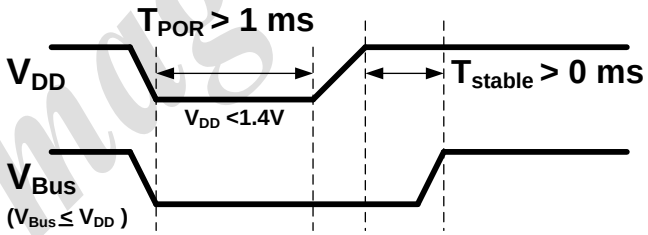
Considering V_{DD} rising time, please make sure a V_{DD} slew rate at least 0.6V/ms. The device has a built-in POR circuit. When the V_{DD} drops below1.4V under room temp, the POR would be triggered and system will be reset. Then power back up at the requirement slew rate, and write registers to the desired values.

While Supply Voltage (V_{DD}) and I^2C Bus Pin Voltage (V_{Bus}) are in the same supply voltage, the stable time between V_{DD} and V_{Bus} (T_{stable}) should be no less than 0ms.V_{Bus} should be less than or equal to V_{DD} always.



Power-on-Reset(POR)

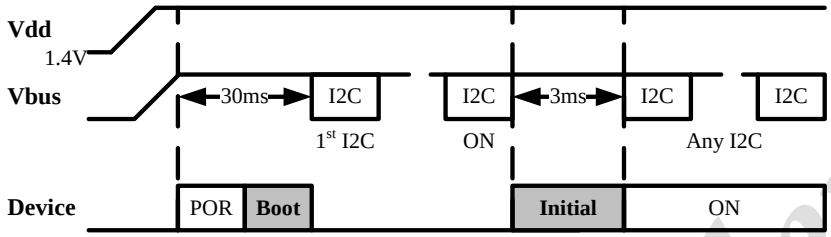
While the HOST wantsto trigger the device power on reset, the V_{DD} should drop below1.4Vand keep at least 1ms (T_{POR}), then raise V_{DD} back following power sequence. V_{Bus} shouldalways be less than or equal to V_{DD}.



POR / Device ON Sequence

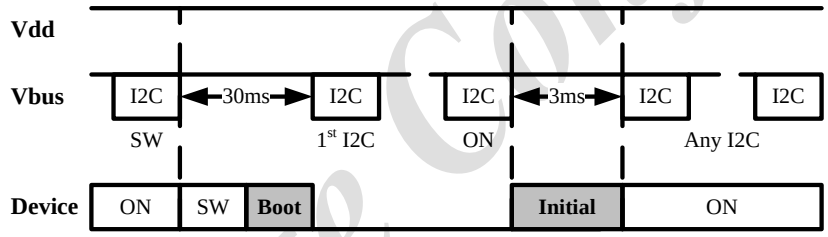
While Supply Voltage (V_{DD}) is rise from 1.4V or under, the device will trigger POR. If the POR has been triggered, the device must be required 30ms to boot. And then the 1st I2C should be send after 30ms (T_{boot}).

When any function (register 0x00) has been enabled, the device will trigger Device ON. If Device ON has been triggered, the device must be required 3ms to initiate. The next I2C should be send after 3ms.



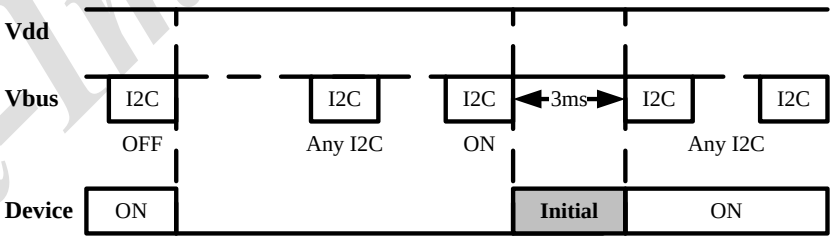
SW / Device ON Sequence

While **SW reset**(register 0x00 = 0x04) has been send by host, the device will trigger SW, too. If the SW has been triggered, the device must be required30ms to boot. And then the 1st I2C should be send after 30ms (T_{boot}).



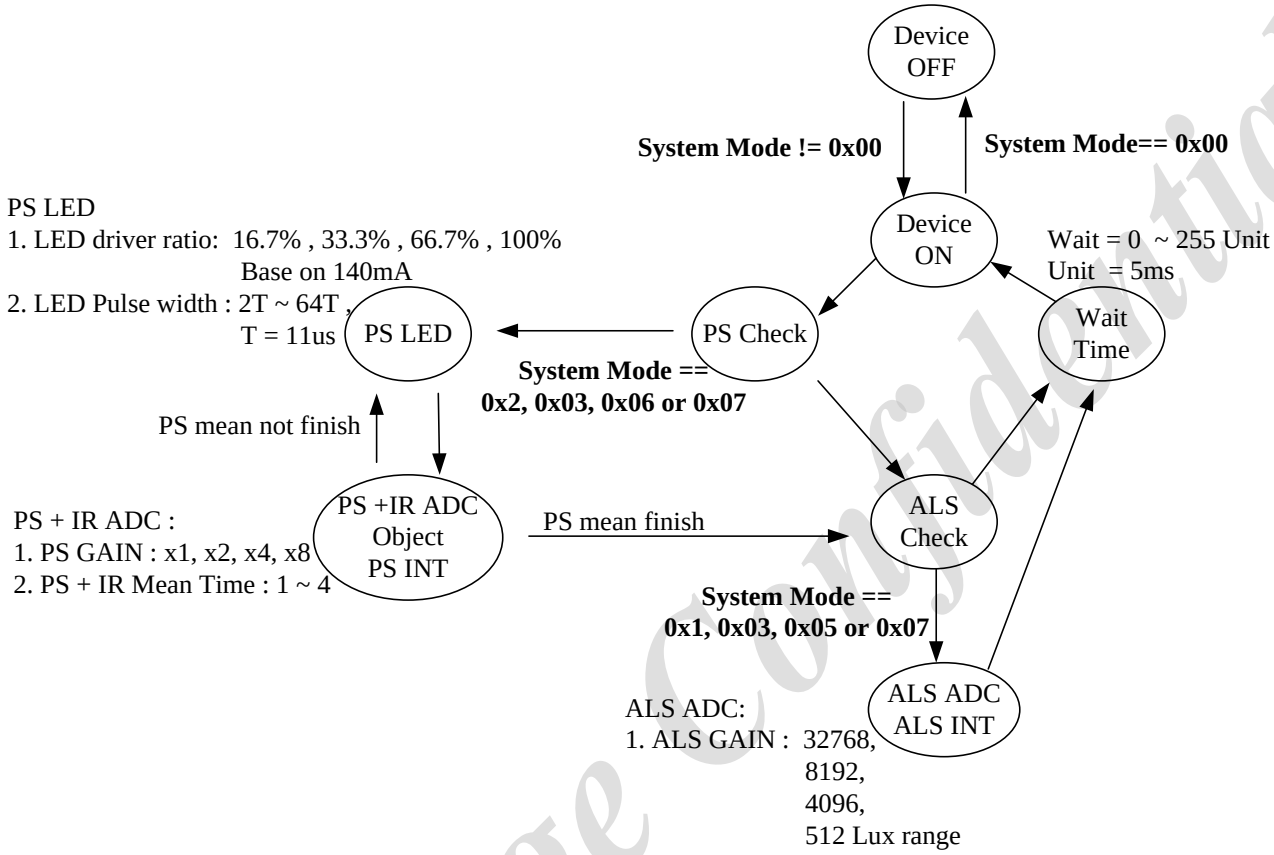
Device OFF / Device ON Sequence

While all function (register 0x00) has been disabled by host, the device will become Device OFF. The device doesn't need additional delay for next I2C command.



State Machine

There are 2 operation functions embedded in this device: ALS,It is controlled by **System Mode** (register 0x00). The state machine behavior describes as below:



Typical Performance Charts

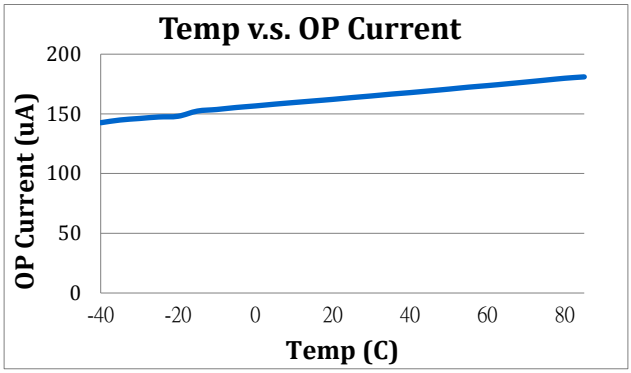


Fig.1 Active Current vs Temp

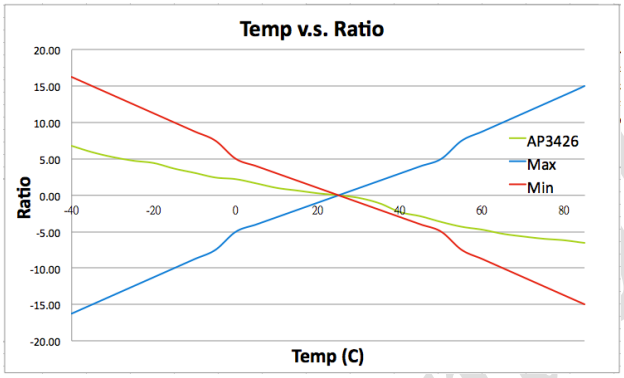


Fig.2ALS Output Code Ratio vs Temp

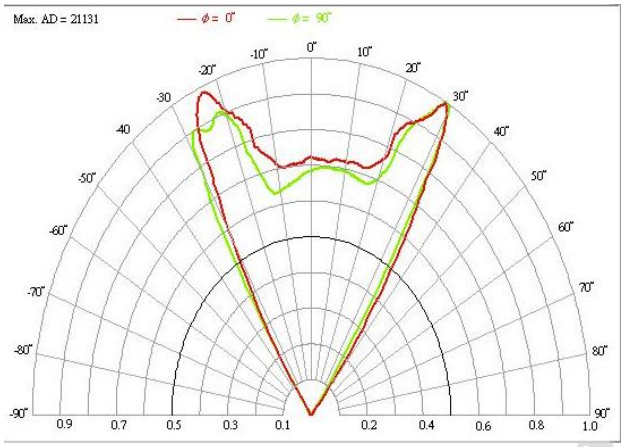


Fig.3 Angular Response of ALS

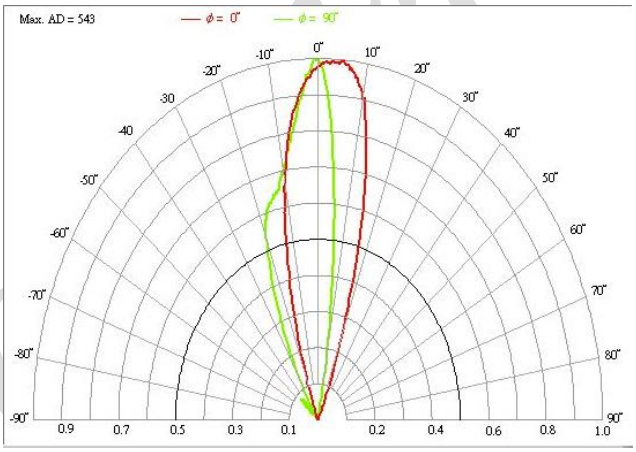


Fig.4 Angular Response of PS

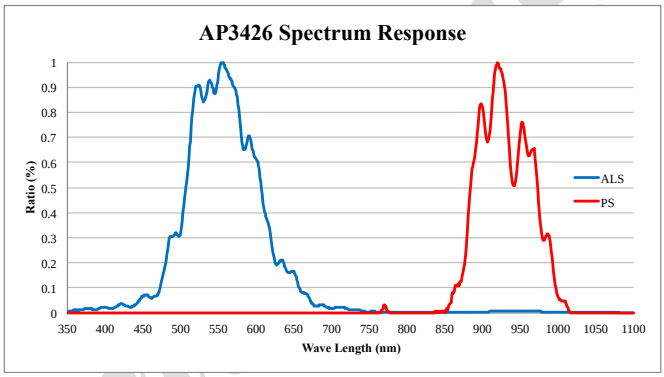


Fig.5Spectrum Response

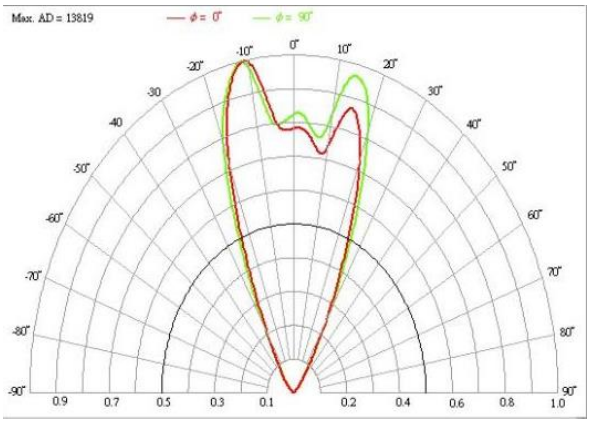
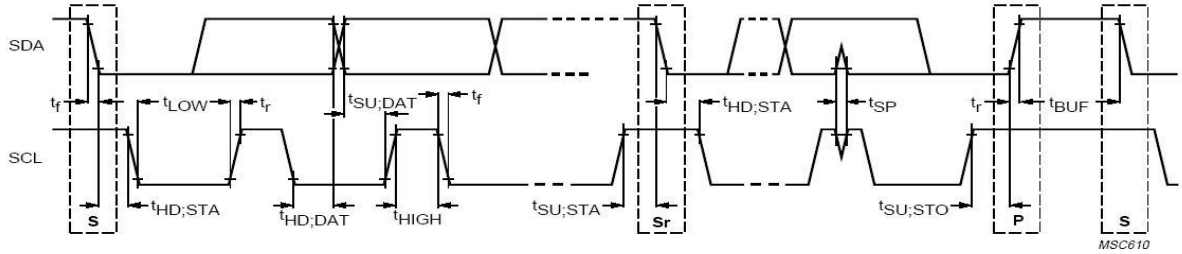


Fig.6 LED Emitting Angle

Definition of timing for I²C devices

This section will describe the main protocol of the I²C bus. For more details and timing diagrams, please refer to the I²C specification.



The device can operate at the standard mode I²C bus line or the fast mode I²C bus line. The characteristics of the I²C bus for difference modes are as bellow.

Characteristics of the SDA and SCL bus lines for I²C bus devices

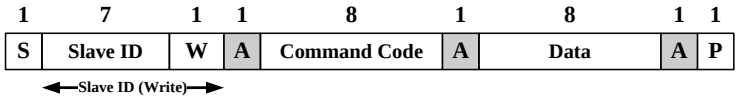
(All specifications are at T_{ope}=25°C, unless otherwise noted.)

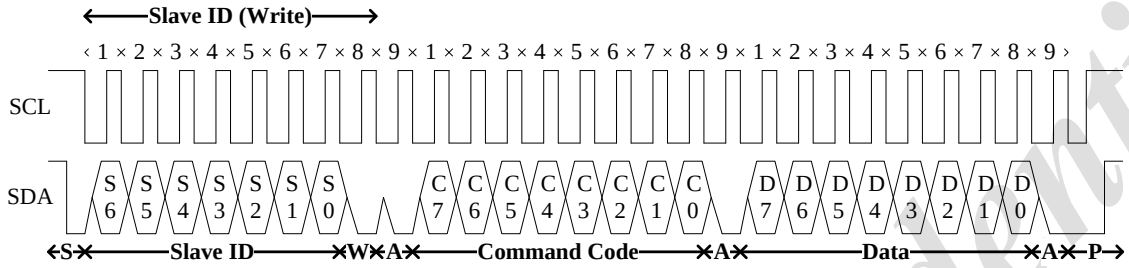
Parameter (*)	Symbol	Fast mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	1	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3	--	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	--	µs
LOW period of the SCL clock	t_{LOW}	1.3	--	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	--	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	--	µs
Set-up time for STOP condition	$t_{SU;STO}$	0.6	--	µs
Rise time of both SDA and SCL signals	t_r	--	300	ns
Fall time of both SDA and SCL signals	t_f	--	300	ns
Data hold time	$t_{HD;DAT}$	50	--	ns
Data setup time	$t_{SU;DAT}$	100	--	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns

(*) Specified by design and characterization; not production tested

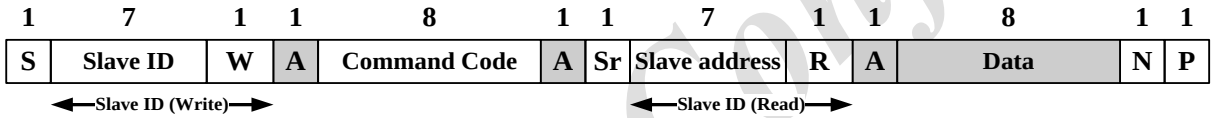
I²C Protocols (7-bit slave address)

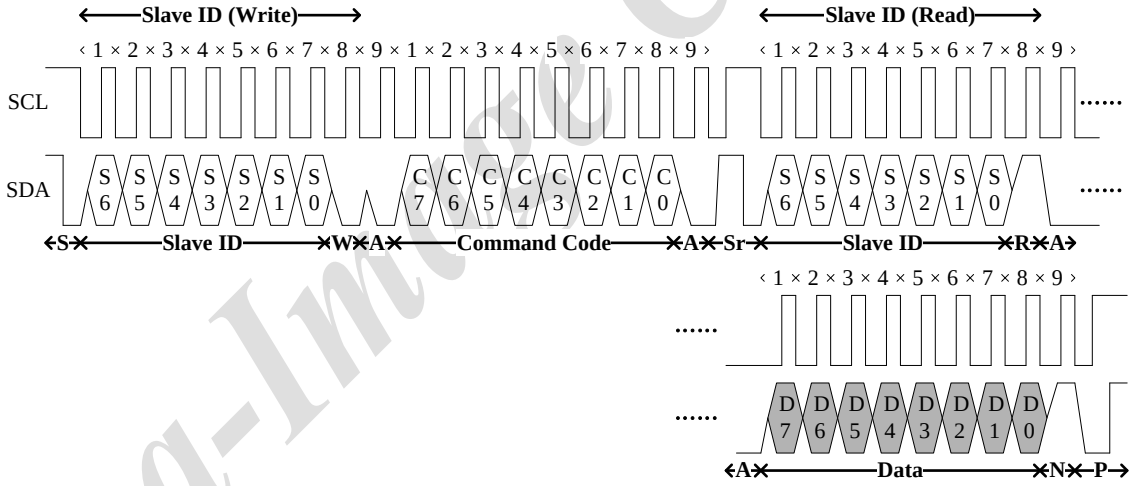
· I2C Write Protocol :





· I2C Read Protocol:

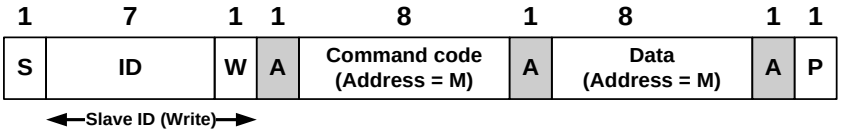




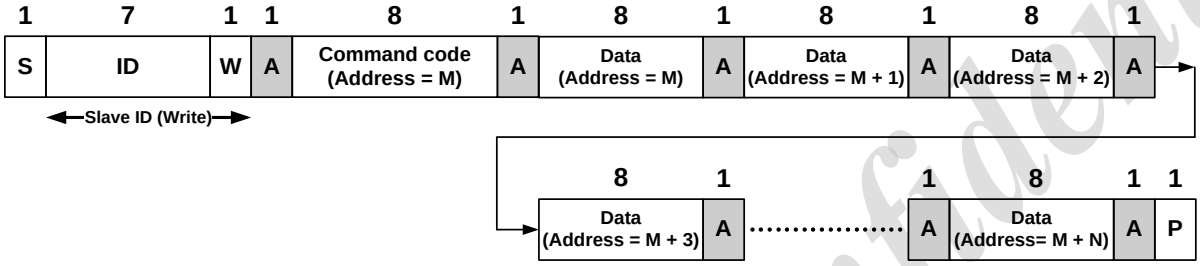
A	Acknowledge (0 for an ACK)	**N**	Non-Acknowledge(1 for an NACK)
S	Start condition	**Sr**	Repeated Start condition
P	Stop condition		
W	Write (0 for writing)	**R**	Read (1 for read)
■	Slave-to-master	□	Master-to-Slave

I2C Block Write Protocol:

Single Write



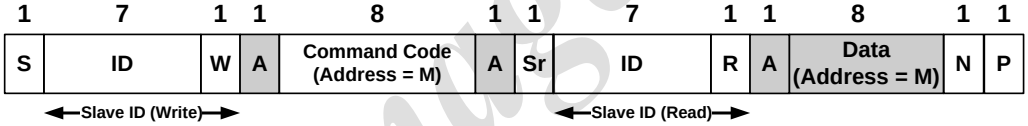
Auto-increment Write



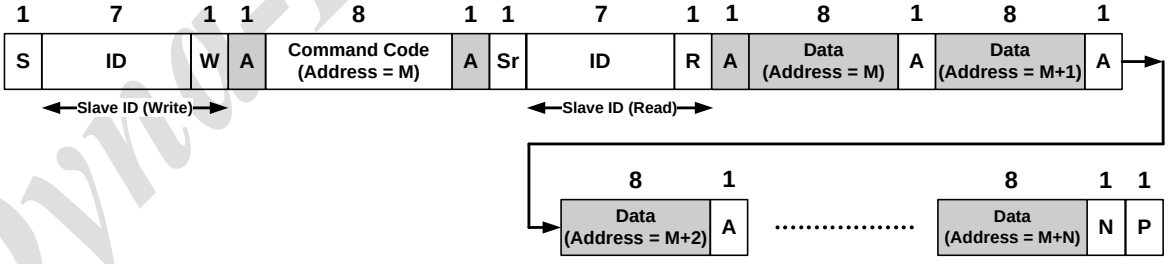
Note : The next address will have rollover if the M+N is equal 0x3F

I2C Block read Protocol:

Single Read



Auto-increment Read



Note : The next address will have rollover if the M+N is equal 0x3F.

I²C Slave Address

Devices' slave address is set**0x1E**. The slave addresses are 7 bits. A read/write bit should be appended to the slave address by the master device to properly communicate with the device.

Register Table List

System Register set

ADDR (Hex)	REGISTER NAME	Bits	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
0x00	System Control (Default=0x00)	2:0	System Mode (Default=0x0)	0x0: Power down **(Default)**
				0x1: ALS function active
				0x2: PS+IR function active
				0x3: ALS and PS+IR functions active
				0x4: SW reset
				0x5: ALS function once
				0x6: PS+IR function once
				0x7: ALS and PS+IR functions once
0x01	Interrupt Flag	5	IR overflow **(Read only)**	0x0: Valid IR, PS data and object detected 0x1: Invalid IR, PS data and object detected
		4	Object detect **(Read only)**	0x0: Object distancing 0x1: Object approaching
		1	PS INT **(Read only)** (Default=0x0)	0x0: Interrupt is cleared or not triggered yet 0x1: Interrupt is triggered Note1
		0	ALS INT **(Read only)** (Default=0x0)	0x0: Interrupt is cleared or not triggered yet 0x1: Interrupt is triggered Note1
0x02	INT Control (Default=0x88)	7	PS INT enable (Default=0x1)	0x0: PS interrupt pin disable 0x1: PS interrupt pin enable (Default)
		3	ALS INT enable (Default=0x1)	0x0: ALS interrupt pin disable 0x1: ALS interrupt pin enable (Default)
		0	Clear Manner (Default=0x00)	0x0: Automatically clear INT by reading data registers 0x1: Software clear after writing 0 into address 0x01 each bit.
0x06	Waiting Time (Default=0x00)	7:0	Waiting Time (Default=0x00)	0x00: no waiting **(Default)** 0x01: 1 waiting …….. 0x3e: 62 waiting 0xff: 255 waiting
0x0A	IR DATA LOW	7:0	(Read only)	IR Lower byte of ADC Output
0x0B	IR DATA HIGH	1:0	(Read only)	IR High byte of ADC Output
0x0C	ALS DATA LOW	7:0	(Read only)	ALS Lower byte of ADC Output
0x0D	ALS DATA HIGH	7:0	(Read only)	ALS High byte of ADC Output
0x0E	PS DATA LOW	7:0	(Read only)	PS Lower byte of ADC Output
0x0F	PS DATA HIGH	1:0	(Read only)	PS High byte of ADC Output

Note 1. The INT pin will be set low and set Interrupt Flag bit when ALS or PS or (ALS+PS) interrupt event occurrence. User can clear INT bit and individual status bits when reading the register 0xD(ALS), 0xF(PS) and 0xD+0xF(ALS+PS) respectively.

ALS Register set

ADDR (Hex)	REGISTER NAME	Bit	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
0x10	ALS Gain (Default=0x00)	5:4	ALS Gain (Default=0x0)	0x0: 32768 lux / Resolution bit **(Default)** 0x1: 8192 lux / Resolution bit 0x2: 2048 lux / Resolution bit 0x3: 512 lux / Resolution bit
0x14	ALS Persistence (Default=0x01)	5:0	ALS Persistence (Default=0x01)	ALS Interrupt is triggered after (integration cycle) 0x00: Force every conversion time 0x01: 1 conversion time **(Default)** 0x02: 2 conversion time 0x03: 3 conversion time 0x04: 4 conversion time …… 0x3f: 63 conversion time
0x1A	ALS Threshold low L (Default=0x00)	7:0		Low byte of Low interrupt threshold for ALS
0x1B	ALS Threshold low H (Default=0x00)	7:0		High byte of Low interrupt threshold for ALS
0x1C	ALS Threshold High L (Default=0xFF)	7:0		Low byte of High interrupt threshold for ALS
0x1D	ALS Threshold High H (Default=0xFF)	7:0		High byte of High interrupt threshold for ALS

PS Register set

ADDR (Hex)	REGISTER NAME	Bit	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
0x20	PS Gain (Default=0x04)	3:2	PS Gain (Default=0x1)	0x0: 1 0x1: 2 **(Default)** 0x2: 4 0x3: 8
0x21	PS LED DRIVER (Default=0x03)	1:0	Max LED driver ratio Based on=140mA @ typ (Default=0x3)	0x0: 16.7% (External/Internal mode) 0x1: 33.3% 0x2: 66.7% 0x3: 100% **(Default)**
0x22	PS INT Form (Default=0x01)	0	PS_Algo (Default=0x1)	0x0: Zone Interrupt Mode 0x1: Hysteresis Interrupt Mode **(Default)**
0x23	PS Mean Time (Default=0x00)	1:0	Edit PS Mean Time (Default=0x0)	0x0: 1 time **(Default)** 0x1: 2 time 0x2: 3 time 0x3: 4 time
0x24	Smart INT (Default=0x00)	0	Smart INT (Default=0x0)	0x0 : normal persistence function 0x1 : enable smart persistence function
0x25	PS / IR IntegrationTime (Default=0x00)	5:0	PS / IR IntegrationTime (Default=0x00)	0x00: 2T (Default) 0x01: 2T …….. 0x3f: 64T, T = 11µs Read out always 0X00, but data setting is the same as 2T.
0x26	PS Persistence (Default=0x02)	5:0	PS Persistence (Default=0x02)	PS Interrupt is triggered after (conversion time) 0x00: Force every conversion time 0x01: 1 conversion time 0x02: 2 conversion time **(Default)** 0x03: 3 conversion time

ADDR (Hex)	REGISTER NAME	Bit	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
				0x04: 4 conversion time …… 0x3f: 63 conversion time
0x28	PS calibration L (Default=0x00)	7:0	PS calibration	Low byte of PS calibration
0x29	PS calibration H (Default=0x00)	0	PS calibration	High byte of PS calibration
0x2A	PS Threshold low L (Default=0x00)	7:0		Low byte of low interrupt threshold for PS
0x2B	PS Threshold low H (Default=0x00)	1:0		High byte of low interrupt threshold for PS
0x2C	PS Threshold high L (Default=0xFF)	7:0		Low byte of high interrupt threshold for PS
0x2D	PS Threshold high H (Default=0x03)	1:0		High byte of high interrupt threshold for PS

Register Set

ADDR (HEX)	REGISTER NAME	DESCRIPTION
0x00	System Control	Control of basic functions
0x01	Interrupt Status	ALS and PS interrupt status and flag output
0x02	INT Clear Manner	Interrupt enable and auto/semi clear INT selector
0x06	Waiting Time	Waiting Time Setup
0x0A	IR DATA LOW	Low byte for IR ADC channel output
0x0B	IR DATA HIGH	High byte for IR ADC channel output
0x0C	ALS DATA LOW	Low byte for ALS ADC channel output
0x0D	ALS DATA HIGH	High byte for ALS ADC channel output
0x0E	PS DATA LOW	Low byte for PS ADC channel output
0x0F	PS DATA HIGH	High byte for PS ADC channel output
0x10	ALS GAIN	Gain control of ALS
0x1A	ALS LOW THRESHOLD(7:0)	Lower part of ALS low threshold
0x1B	ALS LOW THRESHOLD(15:8)	Upper part of ALS low threshold
0x1C	ALS HIGH THRESHOLD(7:0)	Lower part of ALS high threshold
0x1D	ALS HIGH THRESHOLD(15:8)	Upper part of ALS high threshold
0x20	PS GAIN	Gain control of PS
0x21	PS LED DRIVER	Control of LED driver current
0x22	PS INT FORM	Interrupt algorithms style select of PS
0x23	PS MEAN TIME	PS average time selector
0x24	PS SMART INT	Accelerate the INT response time of PS
0x25	PS / IR IntegrationTime	PS integration time setting
0x26	PS Persistence	Configure the Persist count of PS
0x28	PS CALIBRATION L	Offset value to eliminate the Cross talk effect

ADDR (HEX)	REGISTER NAME	DESCRIPTION
0x29	PS CALIBRATION H	Offset value to eliminate the Cross talk effect
0x2A	PS LOW THRESHOLD(7:0)	Lower part of PS low threshold
0x2B	PS LOW THRESHOLD(9:8)	Upper part of PS low threshold
0x2C	PS HIGH THRESHOLD(7:0)	Lower part of PS high threshold
0x2D	PS HIGH THRESHOLD(9:8)	Upper part of PS high threshold

SYSTEM CONTROL Register

0x00	SYSTEM CONTROL (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*					*System Mode*		

The SYSTEM CONTROL register is used to power up/down the device and to select the ALS and/or PS feature of the device.

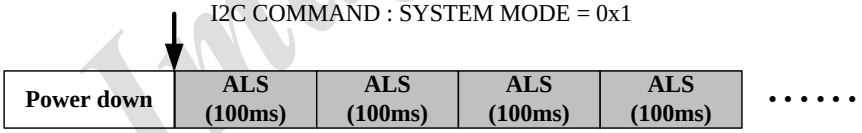
Field	BITS	Description
System mode	2:0	0x0: Power down (Default) 0x1: ALS function active 0x2: PS+IR function active 0x3: ALS and PS+IR functions active 0x4: SW reset 0x5: ALS function once 0x6: PS+IR function once 0x7: ALS and PS+IR functions once

For power down (0x0)

The device will stop operation. The registers will keep their setting at power down, despite the device being asleep. The ALS, PS and IR will be cleared.

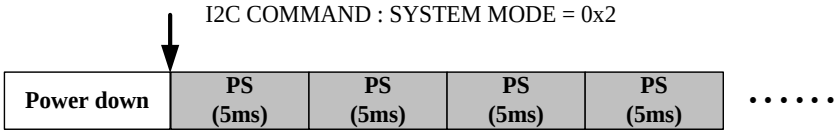
For ALS function active (0x1)

The device will operate only for ALS function. The typical conversion time of ALS is 100ms. The PS data will not work at this mode. The operation time is as follow:



For PS+IR function active (0x2)

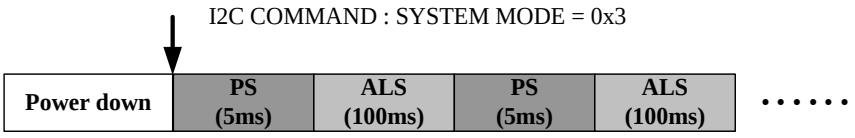
The device will operate only for PS+IR function. The default conversion time of IR is 5ms, and while the PS is decided by the PS waiting time. The ALS data will not work at this mode. The operation time is as follows:



Note: PS Integration Time=2T, waiting=0

For ALS and PS+IR function active (0x3)

The device will operate the ALS and PS+IR function alternately. The conversion time will be the sum of ALS and PXY mode. The operation time is as follows:



Note: PS Integration Time=2T, waiting=0, ALS set as default.

The conversion time of different modes are listed below:

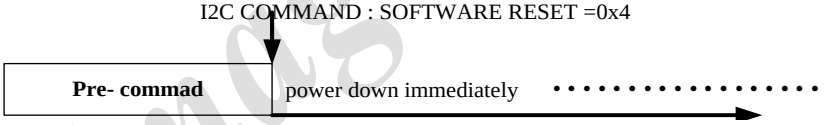
System mode	Conversion time (typical value)	
	ALS	PS + IR
ALS	100ms+waiting time	
PS+IR		PS Conversion + waiting time
ALS and PS+IR	100ms + PS Conversion + waiting time	

Note: ALS set as default

The PS Conversion refers to register 0x25 and the waiting time refers to register 0x24.

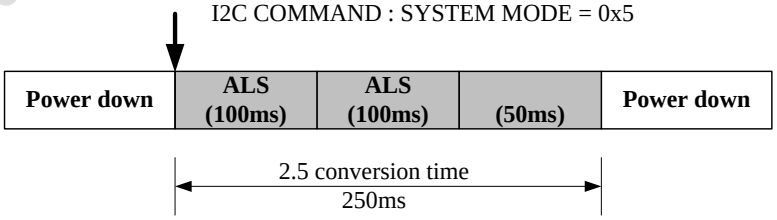
For SW reset (0x4)

Soft Reset Bit. If SWRST=1, all registers of the device will reset to default value and the PORINT flag is set and triggers the INT pin. The SWRST will be reset automatically after the initialization is finished. Write 0 to clear the PORINT.



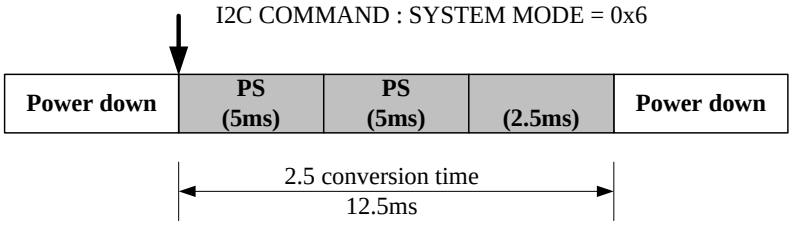
For ALS function once (0x5)

When the host writes this setting, the device will work at ALS mode in a short time frame (typically 2.5 conversion times) and after the device receives the ALS data, the device will automatically power down with the ALS data stored.



For PS function once (0x6)

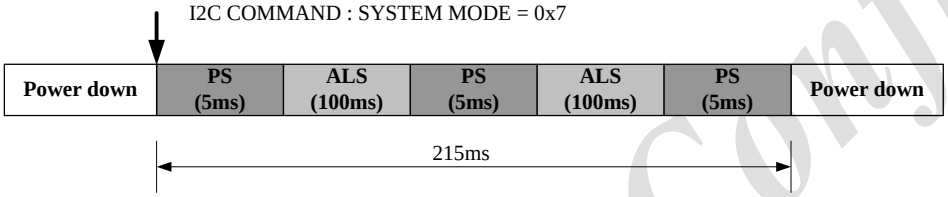
When the host writes this setting, the device will work at PS mode in a short time frame (typically 2.5 conversion times and is not affected by PS waiting time) and after the device receives the PS and IR data, the device will automatically power down with the PS and IR data stored.



Note: PS Integration Time=2T, waiting=0.

For ALS and PS + IR function once (0x7)

When the host writes this setting, the device will operate the ALS and PS+IR function alternately in a short time frame (typically 215ms and is not affected by PS waiting time) and after the device receives the ALS, PS and IR data, the device will automatically power down with the ALS, PS and IR data stored.



Note: PS Integration Time=2T, waiting=0, ALS set as default.

Interrupt Flag Register

0x01	Interrupt Flag Register (default = 0x80)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
W/R	*Reserved*		IR_OV	OBJ	*Reserved*		*PS INT*	*ALS INT*

IR overflow flag (IR_OV): This flag is used to indicate the validity of the PS data. If this bit is enabled, it is a warning that the IR light is at high intensity. *Please refer to description of IR DATA register.

OBJ: PS Object Detection Status Bit. This bit shows the position of the object and it is a read-only bit. Refer to PS_Algo (register 0x22, bit 0) for detailed definition of OBJ.

PS INT: This status bit register is set to 1 when the PS interrupt has been triggered. It will be cleared after 0x0F register has been read or 0x0 is written to the register of the corresponding bit (depending on INT Clear Manner flag).

ALS INT: This status bit register is set to 1 when the PS interrupt has been triggered. It will be cleared after 0x0D register has been read or 0x0 is written to the register of the corresponding bit (depending on INT Clear Manner flag).

INT Control Register

0x02	INT Clear Manner (default = 0x88)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
W/R	*PIEN*	*Reserved*			*AIEN*	*Reserved*		*CLR_MNR*

PIEN: PS Interrupt Enable Bit. This bit is used to enable/disable the INT pin when PS interrupt is asserted or de-asserted.

AIEN: ALS Interrupt Enable Bit. This bit is used to enable/disable the INT pin when ALS interrupt is asserted or de-asserted.

CLR_MNR: This bit is used select automatic/manual interrupt status flag clearing method. When CLR_MNR is set to 0, the interrupt flag is automatic clear by reading the data registers (0x0C, 0x0D, 0x0E, 0x0F). When CLR_MNR is set to 1, the interrupt status flag is cleared manually. For example, if PS_INT is asserted, it can be clear after I2C writes the address 0x01 with 0x00.

Waiting Time Register

0x06	Waiting Time (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Waiting Time*							

In order to decrease power consumption with ALS and PS mode enable. The waiting time can insert idle time frames to elongate the increment of time that the device turns on/off. The insertion of the waiting time slots will also extend the ALS and PS conversion time. Please refer to the table below:

Field	BITS	Description
Waiting Time (N) (Default=0x00)	7:0	Waiting time: Unit = ms 5.0 x N Note: N = 0~255

Waiting times counting rules:

0: non-waiting time slot inserted.

1: 1 consecutive waiting time slots inserted.

2: 2 consecutive waiting time slots inserted.

3: 3 consecutive waiting time slots inserted.

63: 63 consecutive waiting time slots inserted.

255: 255 consecutive waiting time slots inserted.

IR DATA Register

0x0A	IR DATA LOW							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*IR Data Low*							

0x0B	IR DATA HIGH							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*Reserved*						*IR Data High*	

The ADC channel data for IR are expressed as 10-bit data spread across two registers. The IR Data Low provides the lower bytes of the ADC value while Data High provides the upper. The IR DATA shows the magnitude of the environmental IR light. All channel data registers are read-only.

When the lower byte register is read, the upper byte is stored in a temporary register that gets read after the lower byte. Therefore, the upper byte data register will read the correct value regardless of additional integration cycles ending between the reading of the lower and upper byte data registers.

ALS DATA Register

0x0C	ALS DATA LOW							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*ALS Data Low*							

0x0D	ALS DATA HIGH							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*ALS Data High*							

The ADC channel data for ALS are expressed as 16-bit data spread across two registers. The ALS Data Low provides the lower bytes of the ADC value while Data High provides the upper. All channel data registers are read-only.

When the lower byte register is read, the upper byte is stored in a temporary register that gets read after the lower byte. Therefore, the upper byte data register will read the correct value regardless of additional integration cycles ending between the reading of the lower and upper byte data registers.

PS DATA Register

0x0E	PS DATA LOW							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*PS Data Low*							

0x0F	PS DATA HIGH							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*Reserved*						*PS Data High*	

The ADC channel data for PS are expressed as 10-bit data spread across two registers. The PS Data Low provides the lower bytes of the ADC value while Data High provides the upper. All channel data registers are read-only.

When the lower byte register is read, the upper byte is stored in a temporary register that gets read after the lower byte. Therefore, the upper byte data register will read the correct value regardless of additional integration cycles ending between the reading of the lower and upper byte data registers.

ALS Gain Register

0x10	ALS Gain (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*		*ALS Gain*		*Reserved*			

ALS Gain register selects the range and resolution of the device. It has four fixed ranges of gain with 32K/8K/2K/0.5K resolution. The ALS conversion time is 100ms regardless of the ALS gain setting.

Field	BITS	Description
ALS Gain (Default=00)	5:4	0x0:32768 lux / Resolution bit 0x1:8192 lux / Resolution bit 0x2:2048 lux / Resolution bit **(Default)** 0x3:512 lux / Resolution bit

ALS LOW THRESHOLD Register

0x1A	ALS LOW THRESHOLD (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS Low Threshold Lower Part*							

0x1B	ALS LOW THRESHOLD (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS Low Threshold Upper Part*							

The ALS LOW THRESHOLD registers store the values of the low threshold for comparing against ALS DATA (Registers 0x0C and 0x0D). If ALS DATA crosses below the ALS Low Threshold, an interrupt is asserted on the interrupt pin.

ALS HIGH THRESHOLD Register

0x1C	ALS HIGH THRESHOLD (default = 0xFF)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS High Threshold Lower part*							

0x1D	ALS LOW THRESHOLD (default = 0xFF)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS High Threshold Upper part*							

The ALS HIGH THRESHOLD registers store the values of the high threshold for comparing against ALS DATA (Registers 0x0C and 0x0D). If ALS DATA crosses above the ALS High Threshold, an interrupt is asserted on the interrupt pin.

PS GAIN Register

0x20	PS GAIN (default = 0x04)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*				*PS Gain*		*Reserved*	

PS Gain bit can adjust the PS gain. The PS gain will extend the detection range of the device. The IR data will not be affected.

Field	BITS	Description
PS Gain (Default=0x1)	3:2	0x0: 1 (The PS resolution * 1) 0x1: 2 (The PS resolution * 2) **(Default)** 0x2: 4 (The PS resolution * 4) 0x3: 8 (The PS resolution * 8)

PS LED DRIVER Register

0x21	PS LED DRIVER (default = 0x03)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*PS LED Driver*	

The PS LED Driver can select the peak current of the LED driver. The increase in PS LED Driver will increase the range of PS detection and LED current consumption.

Field	BITS	Description
PS LED Driver Based on=140mA @ typical (Default=0x3)	1:0	The LED current percent 0x0: 16.7% (External/Internal mode) 0x1: 33.3% 0x2: 66.7% 0x3: 100% **(Default)**

PS INT FORM Register

0x22	PS INT FORM(default = 0x01)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*							PS_algo

PSMODE: PS Interrupt Mode Bit. This bit is used to set interrupt mode of the PS.

Field	BITS	Description
PS_Algo	0	The PS INT algorithm 0x0: Zone Interrupt Mode 0x1: Hysteresis Interrupt Mode **(Default)**

0x0: Zone Interrupt Mode:

An out-of-range interrupt will be asserted on the interrupt pin in the following conditions

- PS DATA (register 0x0E/0F) < LOW Threshold (register 0x2A/2B) & PS persistence count has been reached. PS Object Status (OBJ) Detection Bit will be set to 0.
- PS DATA > HIGH Threshold (register 0x2C/2D) & PS persistence count has been reached. PS Object Status (OBJ) Detection Bit will be set to 0.

PS Object Status (OBJ) Detection Bit will be set to 1 when LOW Threshold <= PS DATA or PS Data >= High Threshold. Write 0 to clear PSINT (register 0x01, bit 0).

Zone Interrupt Mode

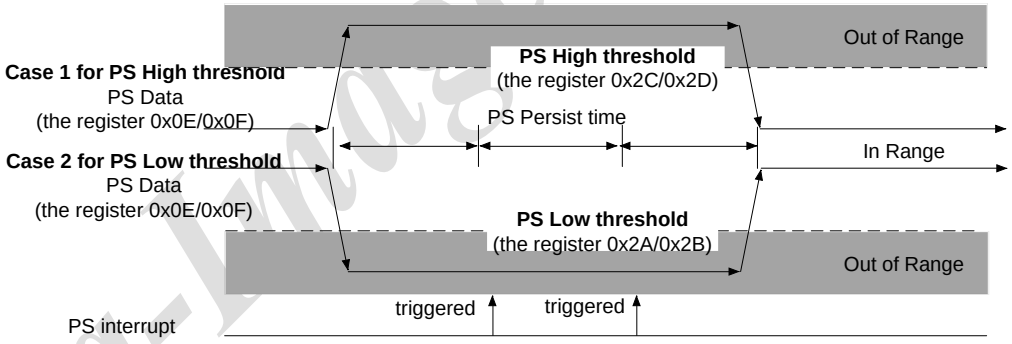


Figure 2. The behavior of PS Zone Interrupt Mode with control flow diagram.

0x1: Hysteresis Interrupt mode:

An interrupt is asserted on the interrupt pin in the following conditions

- PS DATA (register 0x26) < LOW Threshold (register 0x36) & PS persistence count has been reached. PS Object Status (OBJ) Detection Bit will be set to 0.
- PS DATA > HIGH Threshold (register 0x38) & PS persistence count has been reached. PS Object Status (OBJ) Detection Bit will be set to 1.

Write 0 to clear PSINT (register 0x01, bit 0).

Hysteresis Interrupt Mode

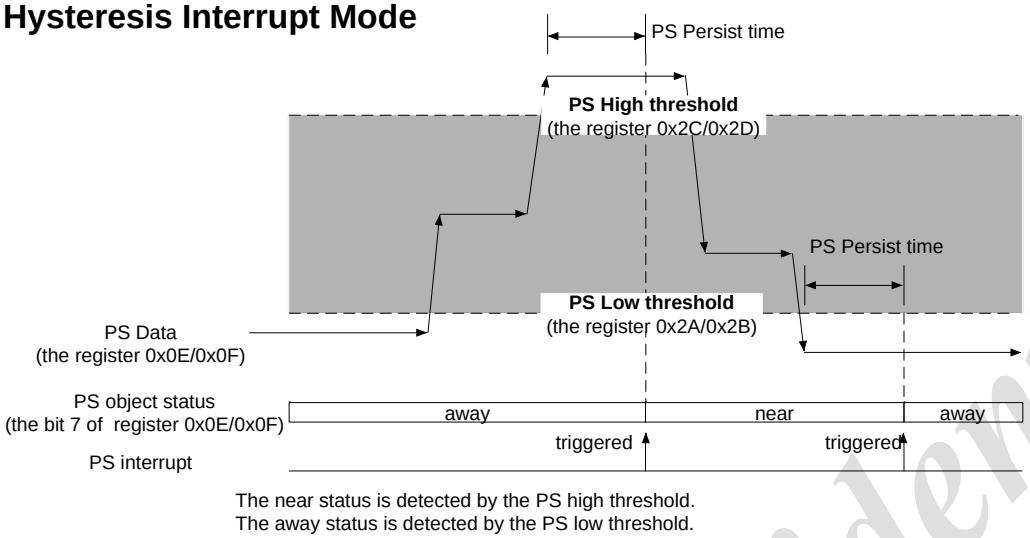


Figure 3. The behavior of PS Mobile INT with control flow diagram.

PS Mean Time Register

0x23	PS mean time (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*PS_Mean_time*	

PSMEAN: proximity mean time is used to configure response time of the proximity detection cycle. Short PSMEAN time increases random noises and decreases the detection sensitivity.

Field	BITS	Description
PS mean time (Default=0x00)	1:0	@ the PS / IR Integration Time = 2T 0x0: 1 time (1 conversion time =5ms) **(Default)** 0x1: 2 time (1 conversion time =9.6ms) 0x2: 3 time (1 conversion time =14.1ms) 0x3: 4 time (1 conversion time =18.7ms)

Smart PS INT Register

0x24	Smart PS persist (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W								*SMRTINT*

SMRTINT: Set this bit to 1 to speed up the PS interrupt response time by skipping waiting time in each conversion cycle.

PS / IR Integration Time Register

0x25	PS / IR Integration Time (default = 0x00)							
BIT	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
R/W	***Reserved***		***PS/IR Integration Time select***					

PS Integration Time selects the duration at which the device's ADC will sample the photodiode current signal. This duration will affect the resolution of the measurement. The longer integration time will increase the resolution of IR and PS data at the same time. The integration time will change the PS conversion time as well. If the PS/IR Integration Time select is "N", the PS conversion time is as follows:

Field	BITS	Description	
PS/IR Integration Time select (N) (Default=0x00)	5:0	PS conversion :	Unit = ms
		For PS mean = 1 :	5.0 + N x 0.0627
		For PS mean = 2 :	9.6 + 2 x N x 0.0627
		For PS mean = 3 :	14.1 + 3 x N x 0.0627
		For PS mean = 4 :	18.7 + 4 x N x 0.0627
		Note: N = 0 ~63	

For example: If the PS/IR Integration Time select is sets as 0x20 (32) and the PS mean time is set as 1.

The PS conversion time = 5.0 + 32 x 0.0627 = 7.0064 ms

The PS Integration Time selects will decide the LED pulse width T, as well. The unit of LED pulse width T is 11µs.

Field	BITS	Description
PS / IR Integration Time (Default=0x00)	5:0	0x00: 2T **(Default)** 0x01: 2T …….. 0x3f: 64T, T = 11µs Read out always 0x00, but data setting is the same as 2T.

PS Persistence Register

0x26	PS Persistence (default = 0x02)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*		*PS Persistense*					

The Proximity persistence register controls the device's ability to filter proximity interrupt. The PPERS (bit 5:0) controls the rate of proximity interrupts sent to the host processor. Interrupt is triggered after PS object status changes and keeps its state for the number of PPERS times. Write 0 to PPERS to disable proximity persistence function and proximity interrupt is asserted on every conversion cycle.

Field	BITS	Description
PS Persistence (Default=0x1)	5:0	PS Interrupt is triggered after (conversion time) : 0x00 : 1 force every conversion time 0x01 : 1 conversion time 0x02 : 2 conversion time **(Default)** 0x03 : 3 conversion time 0x04 : 4 conversion time …… 0x3f: 63 conversion time

PXY persistence counting rules:

0x00: force every conversion time to be trigger the interrupt.

0x01: 1 consecutive PS data before interrupting

0x02: 2 consecutive PS data before interrupting

0x03: 3 consecutive PS data before interrupting

:

X03f :63 consecutive PS data before interrupting

PS LOW THRESHOLD Register

0x2A	PS LOW THRESHOLD (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*PS Low Threshold Lower Part*							

0x2B	PS LOW THRESHOLD (default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*PS Low Threshold Upper Part*	

PS HIGH THRESHOLD Register

0x2C	PS HIGH THRESHOLD (default = 0xFF)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*PS High Threshold Lower Part*							

0x2D	PS HIGH THRESHOLD (default = 0x03)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*PS High Threshold Upper part*	

PS THRESHOLD registers store the values of the high and low trigger points for comparing against PS DATA (Registers 0x0E and 0x0F). The host can chose the method of the PS interrupt behavior by setting the PS INT FORM (Register 0x22) and the PS HIGH/LOW THRESHOLD (Register 0x2A / 0x2B / 0x2C / 0x2D).

The PS Low Threshold registers are expressed as 10-bit data spread across two registers, PS Low Threshold Lower part and PS Low Threshold upper part.

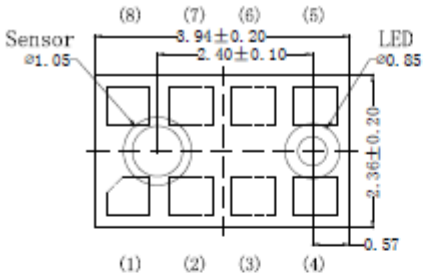
PS Low threshold = Reg_0x2B * 256 + Reg_0x2A

The PS High Threshold registers are expressed as 10-bit data spread across two registers, PS High Threshold Lower part and PS High Threshold upper part.

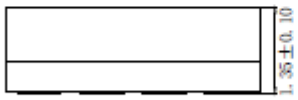
PS High threshold = Reg_0x2D * 256 + Reg_0x2C

Package Outline Dimensions (AP3426)

All dimensions are in mm, unless otherwise stated

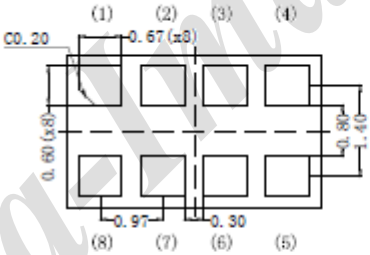


Top View



Front View

Right Side View

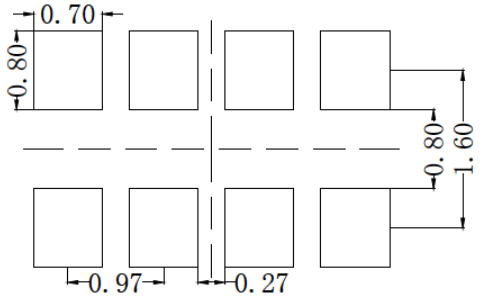


Bottom View

PINOUT

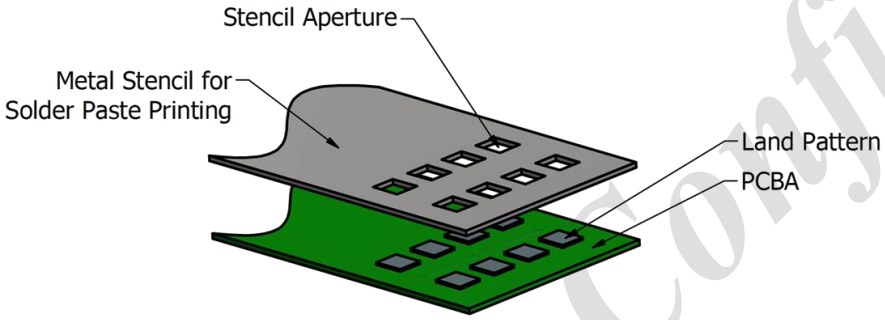
1. VDD
2. SCL
3. GND
4. LEDA
5. LEDC
6. LDR
7. INT
8. SDA

Recommended Land Pattern (AP3426) *All dimensions are in mm, unless otherwise stated*



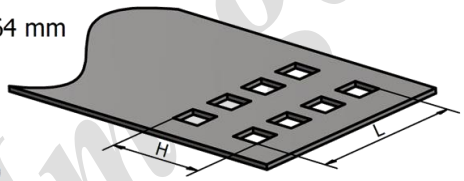
Note: AP3426 land pattern differs from that of AP3426--X

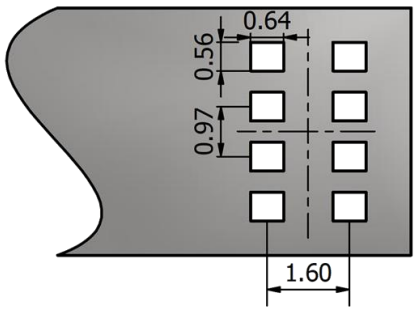
PCB Stencil (AP3426) *All dimensions are in mm, unless otherwise stated*



Stencil opening 0.56x0.64 mm
(80% of Land Pattern)

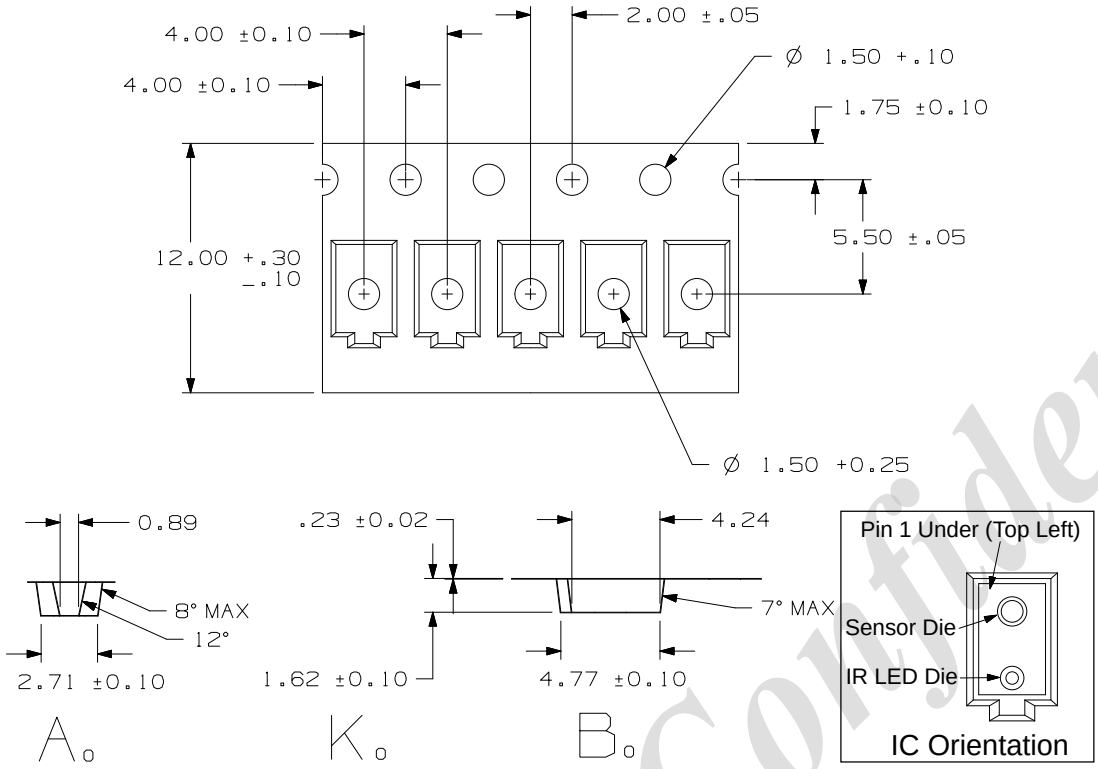
L=3.47 mm
H=2.24 mm
t=0.11 mm (4mils)



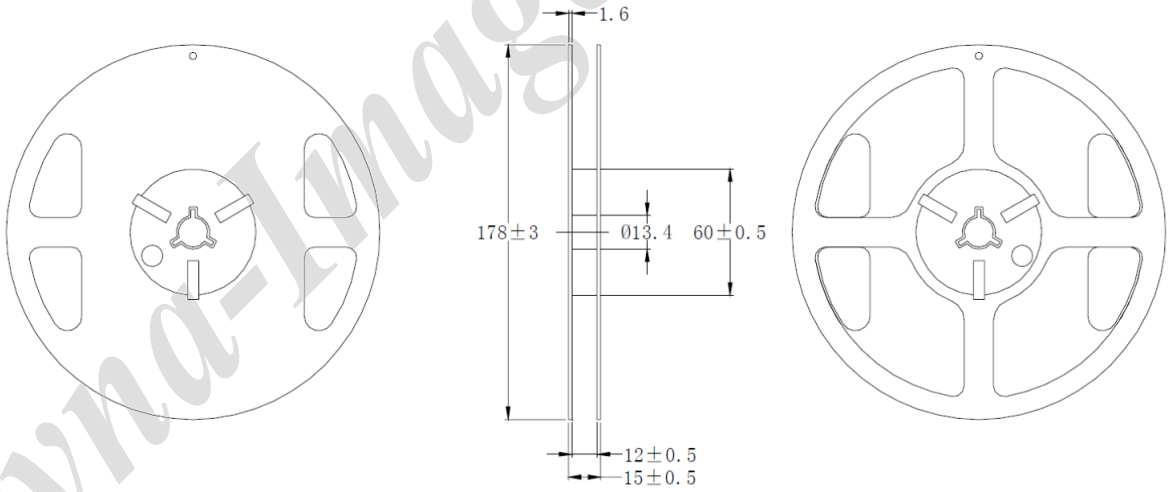


Note: The dimensions of stencil are designed based on the SMT process tolerance (less than+/-3°rotation and +/- 0.05mm offset).

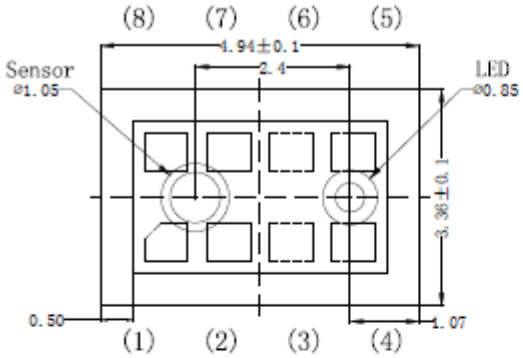
Package Dimension of Tape (AP3426) *All dimensions are in mm, unless otherwise stated*



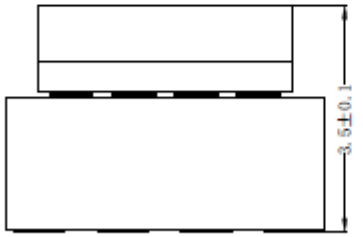
Package Dimension of 7" Reel (AP3426) *All dimensions are in mm, unless otherwise stated*



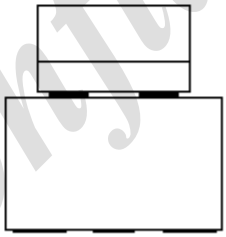
Package Outline Dimensions (AP3426-3.5) *All dimensions are in mm, unless otherwise stated*



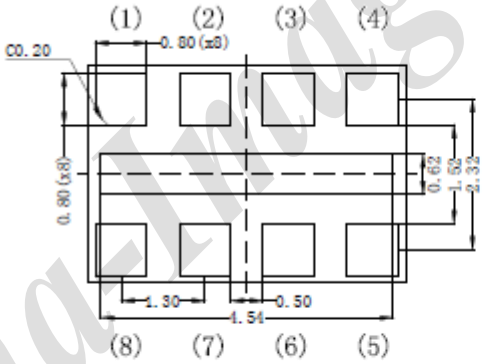
Top View



Front View



Right Side View

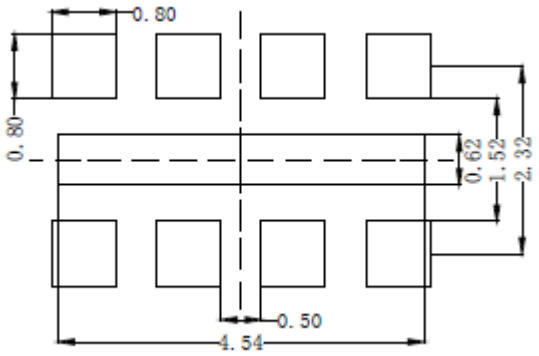


Bottom View

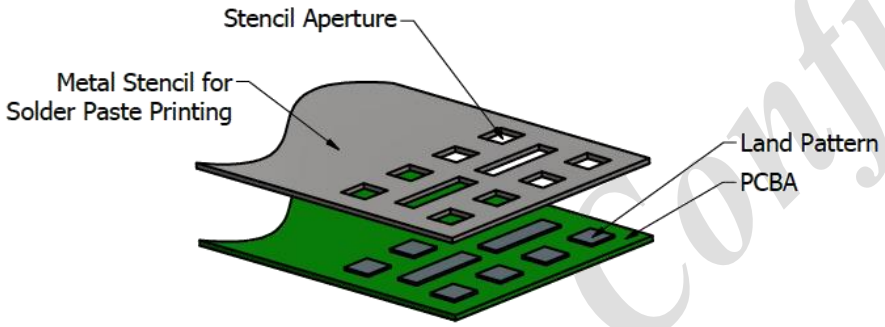
PINOUT

1. VDD
2. SCL
3. GND
4. LEDA
5. LEDC
6. LDR
7. INT
8. SDA

Recommended Land Pattern (AP3426-3.5) *All dimensions are in mm, unless otherwise stated*

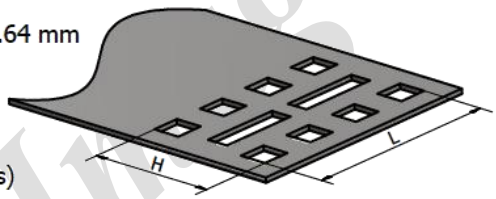


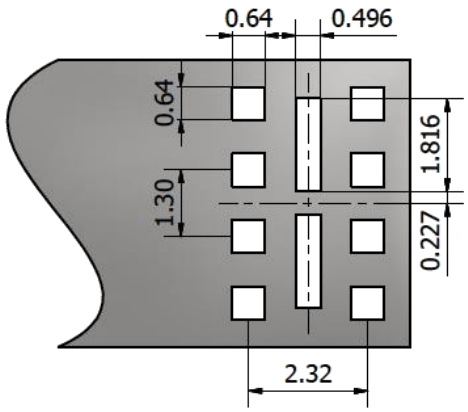
PCB Stencil (AP3426-3.5) *All dimensions are in mm, unless otherwise stated*



Stencil opening 0.64x0.64 mm
(80% of Land Pattern)

L=4.54 mm
H=2.96 mm
t=0.11 mm (4mils)

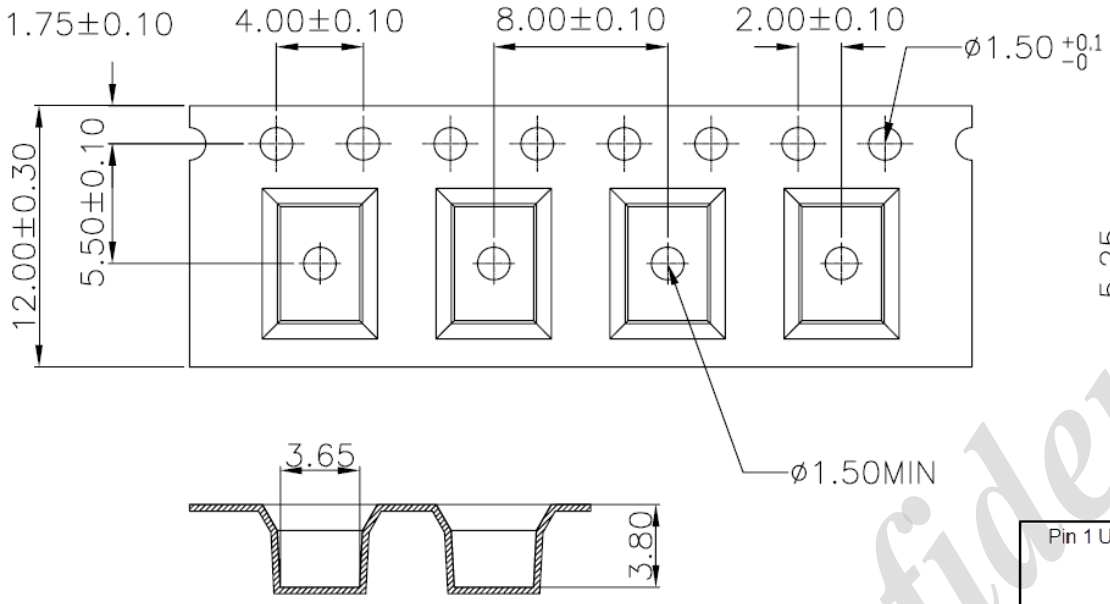


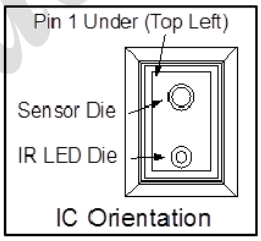


Note: The dimensions of stencil are designed based on the SMT process tolerance (less than+/-3°rotation and+/-0.05mm offset).

Package Dimension of Tape (AP3426-3.5)

All dimensions are in mm, unless otherwise stated

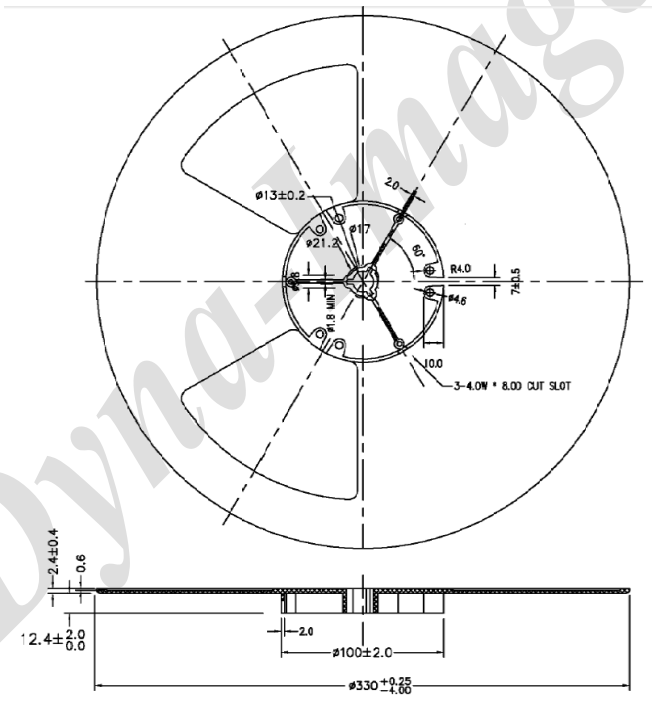


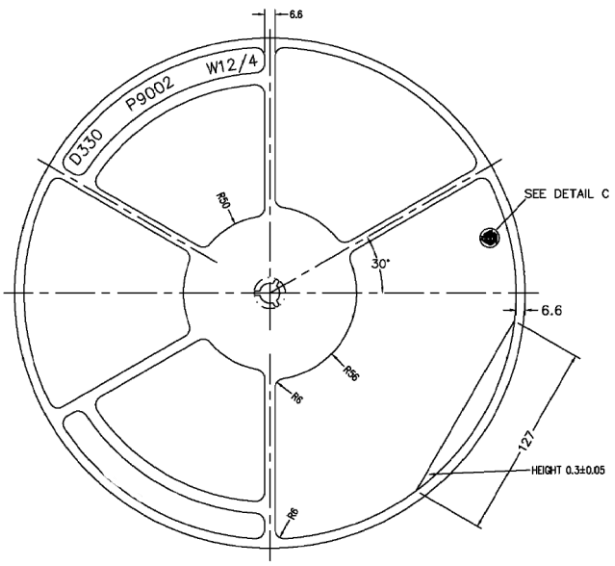


1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.

Package Dimension of 13" Reel

All dimensions are in mm, unless otherwise stated

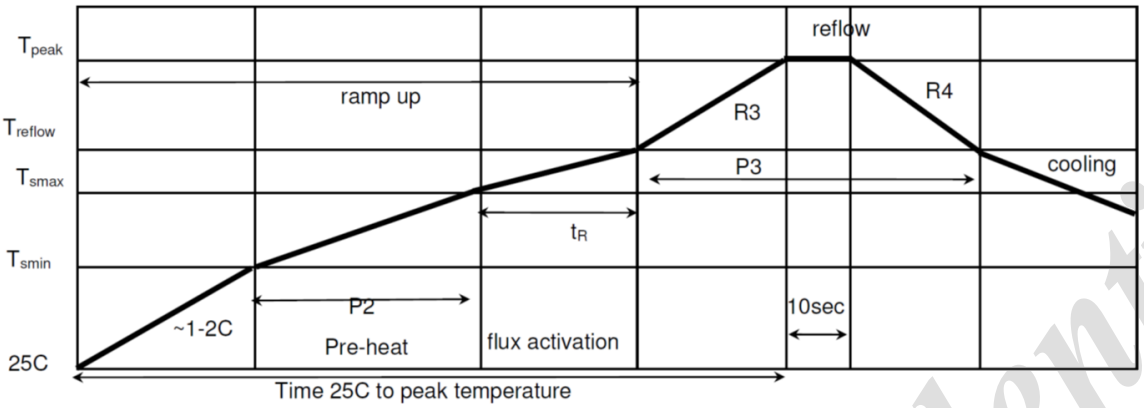




NOTES :
1. MATERIAL : POLYSTYRENE (WHITE)
2. ANTISTATIC COATED
3. FLANGE WARPAGE : 3 MM MAXIMUM
4. ALL DIMENSIONS ARE IN MM
5. ESD – SURFACE RESISTIVITY
– 10^5 TO 10^{11} OHMS/SQ.
6. GENERAL TOLERANCE : ±0.25 MM
7. TOTAL THICKNESS OF REEL: 18.4 MAX.

Recommended Reflow Profile

AP3426/AP3426-3.5 Reflow Profile



	Peak temperature (Tpeak)	255-260C (max) ; 10sec
Pre-Heat	Temperature min (Tsmin) Temperature max (Tsmax) P2: (Ts min to Ts max)	150C 2C/sec 150C-217C 100s to 180s 90-110s
Time maintain above	Temperature (T_{reflow}) Time (P3) R3 slope (from 217C -> peak) R4 slope (from peak -> 217C)	217C 60-90sec 2C/sec [typ] -> 2.5C/sec (max) -1.5C/sec [typ]-> -4C/sec (max)
	Time to peak temperature	480s max
	Cooling down slope (peak to 217C)	2-4C/ sec

Note for AP3426 and AP3426-3.5 the actual profile may need to be adjusted base on the actual layout. When parts are placed upside down, proper protection/support is recommended, max reflow should not exceed 3x max