Application Note for LPDDR2 Boundary Scan

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1. PREFACE

Winbond LPDDR2 device is built with boundary scan chain for users to test the connectivity between memory controller and memory device itself.

The boundary scan chain provide a simply way to check status of connection between memory controller and memory device itself. The boundary scan chain is able to be enabled by a SEN input. All the connection status of each IO between memory controller and memory device will be latched by the scan chain in parallel and be read out from a dedicated output pin serially.

2. PACKAGE BALL OUT

2.1 134 ball VFBGA

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU	B
C	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ	C
D	VSS	VDD2	ZQ0		VDDQ	DQ30 NC	DQ27 NC	DQS3_t NC	DQS3_c NC	VSSQ	D
E	VSSCA	CA9	CA8		DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ	E
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ	F
G	VDD2	CA5	vref(CA)		DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ	G
H	VDDCA	VSS	CK_c		DM1	VDDQ					H
J	VSSCA	NC	CK_t		VSSQ	VDDQ	VDD2	VSS	Vref(DQ)		J
K	CKE0	NC	NC		DM0	VDDQ					K
L	CS0_n	NC	NC		DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ	L
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ	M
N	VSSCA	VDDCA	CA1		DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ	N
P	VSS	VDD2	CA0		VDDQ	DQ17 NC	DQ20 NC	DQS2_t NC	DQS2_c NC	VSSQ	P
R	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ	R
T	DNU	NC	SEN		VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU	T
U	DNU	DNU							DNU	DNU	U

Note: The SEN input is assigned at ball T3.

2.2 168 ball VFBGA

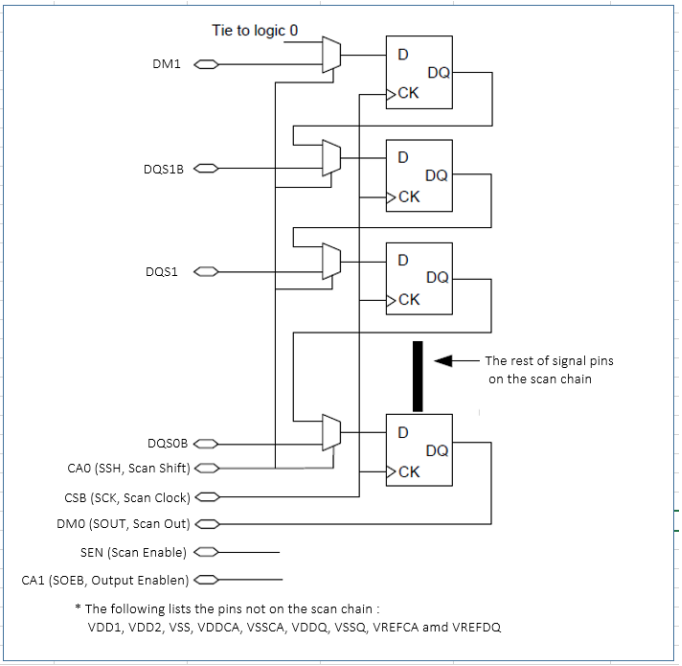
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_c	VDD1	VSS	NC	NC
B	NC	NC	VDD1	NC	VSS	NC	NC	VSS	NC	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	DM3	VDD2	NC	NC
C	VSS	VDD2																				DQ15	VSSQ
D	NC	NC																				VDDQ	DQ14
E	NC	NC																				DQ12	DQ13
F	NC	VSS																				DQ11	VSSQ
G	NC	NC																				VDDQ	DQ10
H	NC	NC																				DQ8	DQ9
J	NC	VSS																				DQS1_t	VSSQ
K	NC	NC																				VDDQ	DQS1_c
L	NC	NC																				VDD2	DM1
M	SEN	VSS																				Vref(DQ)	VSS
N	NC	VDD1																				VDD1	DM0
P	ZQ	Vref(CA)																				DQS0_c	VSSQ
R	VSS	VDD2																				VDDQ	DQS0_t
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	VSSQ
V	VSSCA	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CK_c	CK_t																				DQ1	VSSQ
AA	VSS	VDD2																				VDDQ	DQ0
AB	NC	NC	CS_n	NC	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_t	VDDQ	DM2	VDD2	NC	NC
AC	NC	NC	CKE	NC	VSS	CA0	CA2	VDDCA	VSS	NC	NC	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2_c	VDD1	VSS	NC	NC

Note: The SEN input is assigned at ball M1.

3. BALL OUT DESCRIPTION

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. CS_n is sampled at the positive Clock edge.
CA[n:0]	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ[n:0]	I/O	**Data Inputs/Output:** Bi-directional data bus. n=15 for 16 bits DQ; n=31 for 32 bits DQ.
DQSn_t, DQSn_c	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15; DQS2_t and DQS2_c to the data on DQ16-23; DQS3_t and DQS3_c to the data on DQ24-31.
DMn	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
SEN	Input	**Scan Enable:** SEN must be asserted HIGH for enabling boundary scan ifunction. Must be tied to Ground when not in use.
V_{DD1}	Supply	**Core Power Supply 1:** Power supply for core.
V_{DD2}	Supply	**Core Power Supply 2:** Power supply for core.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
$V_{REF(CA)}$	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for CA Input Receivers**
V_{SSQ}	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

4. BLOCK DIAGRAM OF BOUNDARY SCAN CHAIN



5. CONTROL SIGNALS OF BOUNDARY SCAN

Pin Name	Type	Function	Description
SEN	Input	SEN	Scan Enable: H: Scan enable L: Scan disable
CSB	Input	SCK	Scan Clock: For latching scan data in front of the can register. All scan inputs will be referred to rising edge of CSB.
CA0	Input	SSH	Scan Shift: H: For shifting data on the chain L: For latching data on the chip pad
CA1	Input	SOEB	Scan Output Enable: H: Scan output disabled L: Scan output enabled
DM0	Output	SOUT	Scan Output: All latched scan data will serially output from DM0 referred to rising edge of CSB.

Notes:

1. When SEN is asserted, no commands are to be executed by the LPDDR2 device. This applies both to user commands and manufacturing commands which may exist while CA0 is deasserted.
2. The Scan Function can be used right after bringing up V_{DD} / V_{DDQ} of the device. No initialization sequence of the device is required. After leaving the Scan Function it is required to run through the complete initialization sequence.
3. In Scan Mode all terminations for CMD/ADD and DQ, DM, DQSn_t and DQSn__c are switched off.

6. BOUNDARY SCAN OUTPUT ORDER

6.1 Sequence of scan data output (32 IOs mode)

BIT#	PAD	BIT#	PAD	BIT#	PAD	BIT#	PAD	BIT#	PAD
1	DQS0_c	13	DQS2_t	25	CKE	37	DQ28	49	DQ11
2	DQS0_t	14	DQ23	26	CK_t	38	DQ27	50	DQ10
3	DQ7	15	DQ22	27	CK_c	39	DQ26	51	DQ9
4	DQ6	16	DQ21	28	CA5	40	DQ25	52	DQ8
5	DQ5	17	DQ20	29	CA6	41	DQ24	53	DQS1_t
6	DQ4	18	DQ19	30	CA7	42	DQS_t	54	DQS1_c
7	DQ3	19	DQ18	31	CA8	43	DQS_c	55	DM1
8	DQ2	20	DQ17	32	CA9	44	DM3		
9	DQ1	21	DQ16	33	ZQ	45	DQ15		
10	DQ0	22	CA2	34	DQ31	46	DQ14		
11	DM2	23	CA3	35	DQ30	47	DQ13		
12	DQS2_c	24	CA4	36	DQ29	48	DQ12		

6.2 Sequence of scan data output (16 IOs mode)

BIT#	PAD	BIT#	PAD	BIT#	PAD
1	DQS0_c	13	CA4	25	DQ13
2	DQS0_t	14	CKE	26	DQ12
3	DQ7	15	CK_t	27	DQ11
4	DQ6	16	CK_c	28	DQ10
5	DQ5	17	CA5	29	DQ9
6	DQ4	18	CA6	30	DQ8
7	DQ3	19	CA7	31	DQS1_t
8	DQ2	20	CA8	32	DQS1_c
9	DQ1	21	CA9	33	DM1
10	DQ0	22	ZQ	34	
11	CA2	23	DQ15	35	
12	CA3	24	DQ14	36	

7. BOUNDARY SCAN OPERATION

There are two modes of boundary scan operations

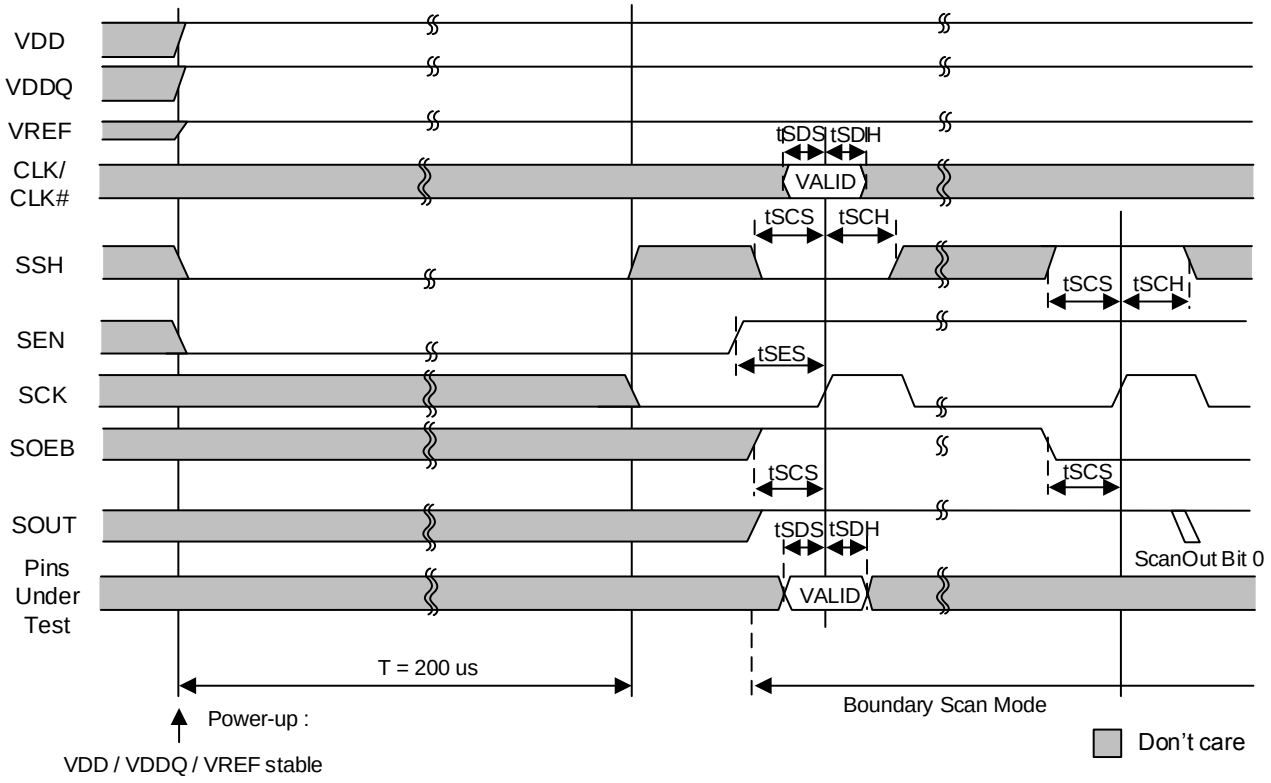
- The first mode is the Stand-Alone mode. In the Stand-Alone mode the LPDDR2 device is supposed to support the Boundary Scan functionality only, the user does not intend to operate the DRAM in its ordinary functionality after or prior to the entering of the Boundary Scan functionality. The purpose of the Stand-Alone mode could be a connectivity test at the manufacturing site.
- The second mode is the regular LPDDR2 device functionality. With this common mode the boundary scan functionality can be enabled after the LPDDR2 device has been initialized by the regular power-up and LPDDR2 device Initialization sequence. When the boundary scan functionality is left, the regular LPDDR2 device initialization sequence has to be re-iterated.

7.1 Scan Initialization for Stand-Alone Mode

The LPDDR2 device needs to follow the given sequence below to support the boundary scan functionality in the Stand-Alone mode. There is no external clock for the whole sequence needed.

1. External Voltages (VDD/VDDQ/VREF) need to be stable for 200µs, SEN has to be kept low.
2. Bring SEN up to high state to enter boundary scan functionality.
3. Operate boundary scan functionality.
4. Boundary scan can be exited by bringing SEN to LOW or simply by switching power off.

Scan Initialization for Stand-Alone mode



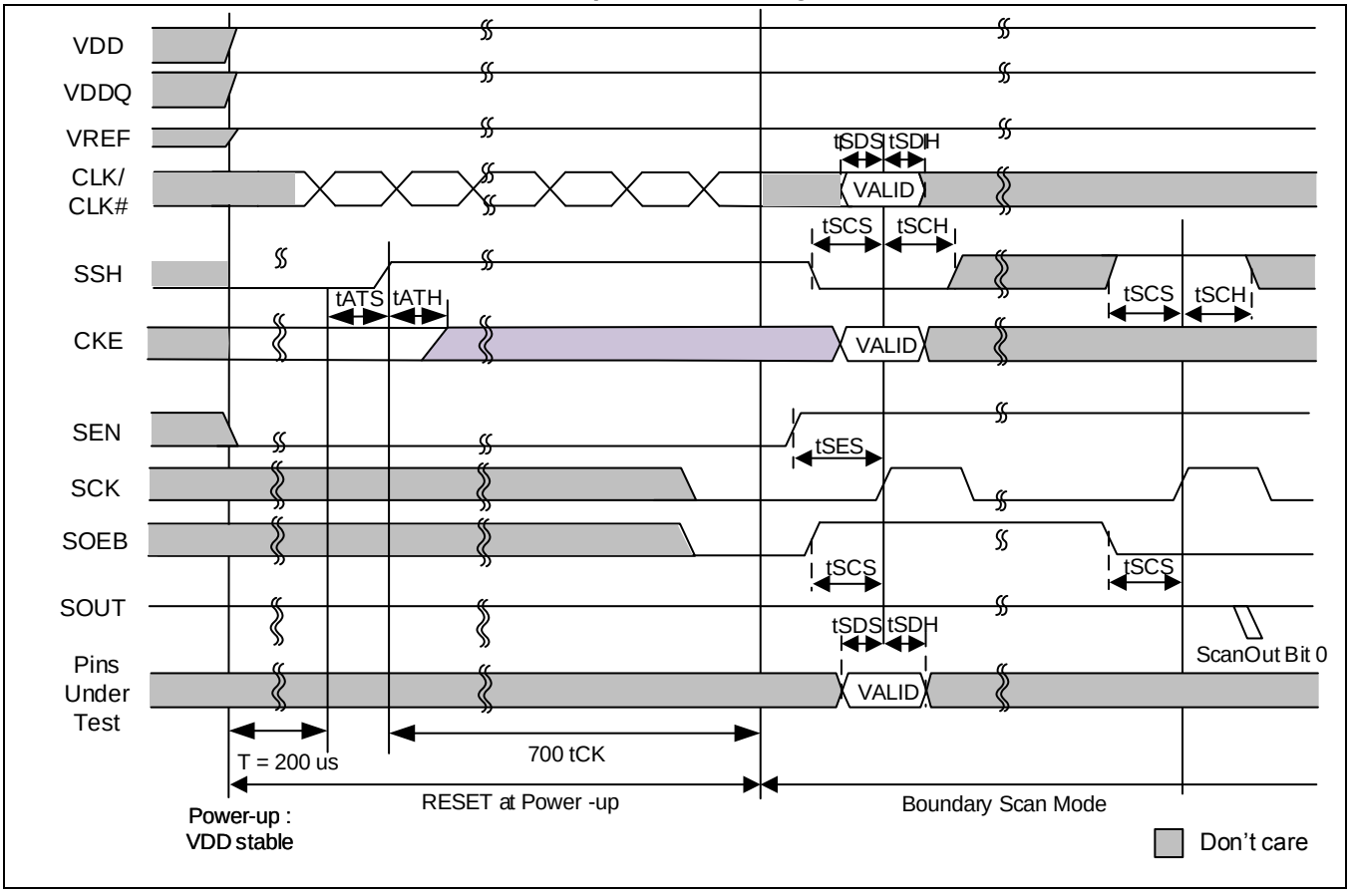
7.2 Scan Initialization in regular LPDDR2 operation

The Initialization sequence of the boundary scan functionality in regular LPDDR2 operation has to follow the given sequence below:

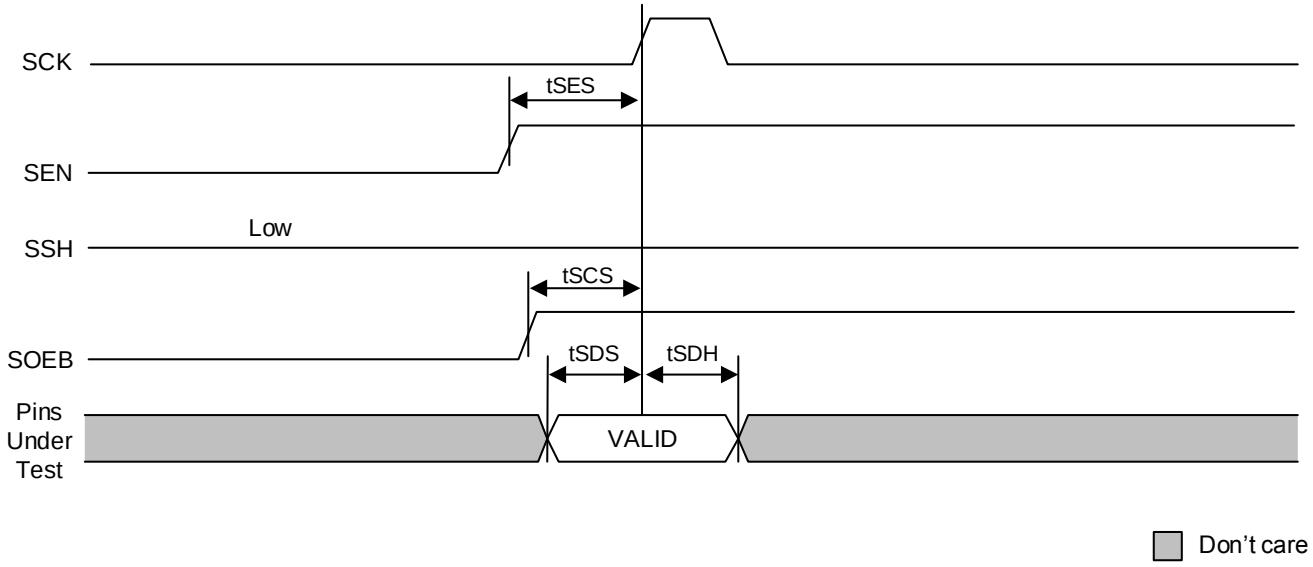
1. External Voltages (VDD/VDDQ/VREF) need to be stable for 200 µs, SSH has to be kept low, external clock has to be stable prior to SSH goes high
2. Bring SSH high and keep clock stable for 700tcks, CKE will be latched by rising SSH edge, keep tATH/tATS
3. Bring SEN up to high state to enter boundary scan functionality
4. Operate boundary scan functionality
5. Boundary scan can be exited by bringing SEN low
6. Wait tSN for bringing up SSH, prior to bringing SSH to high state, external clock has to be stable.
7. After SSH is at high state wait 700tck
8. Continue with regular Initialization sequence

The steps 1 and 2 are necessary to enable the termination for the command/address pins. They are part of the regular LPDDR2 Initialization. They are required if the user wants to issue commands between entering of the boundary scan functionality and the power-up sequence. The entering of the boundary scan mode is resetting the command/address termination values and all MRS settings. Therefore, they have to be initialized again after the boundary scan functionary has been left.

Scan Initialization Sequence within regular LPDDR2 device



7.3 Scan Capture Timing

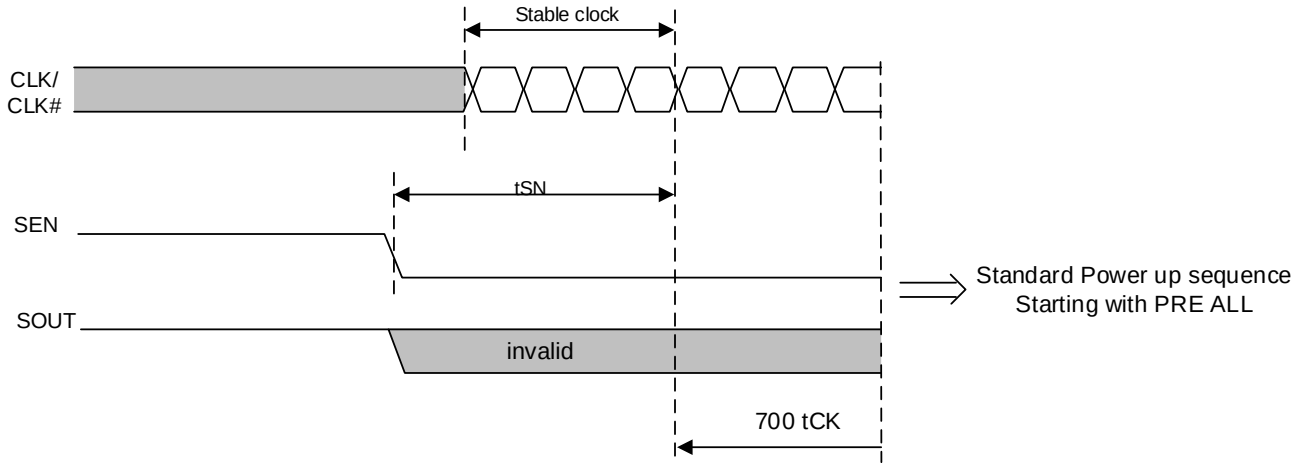


Note:
For complementary pins (CLK/CLKB and DQS<i>/DQSB<i>) during BSC test, complementary pin must have different level of input for scan capture. For example, CLK=H / CLKB=L or CLK=L / CLKB=H. Condition of CLK=H / CLKB=H or CLK=L / CLKB=L is not allowed.

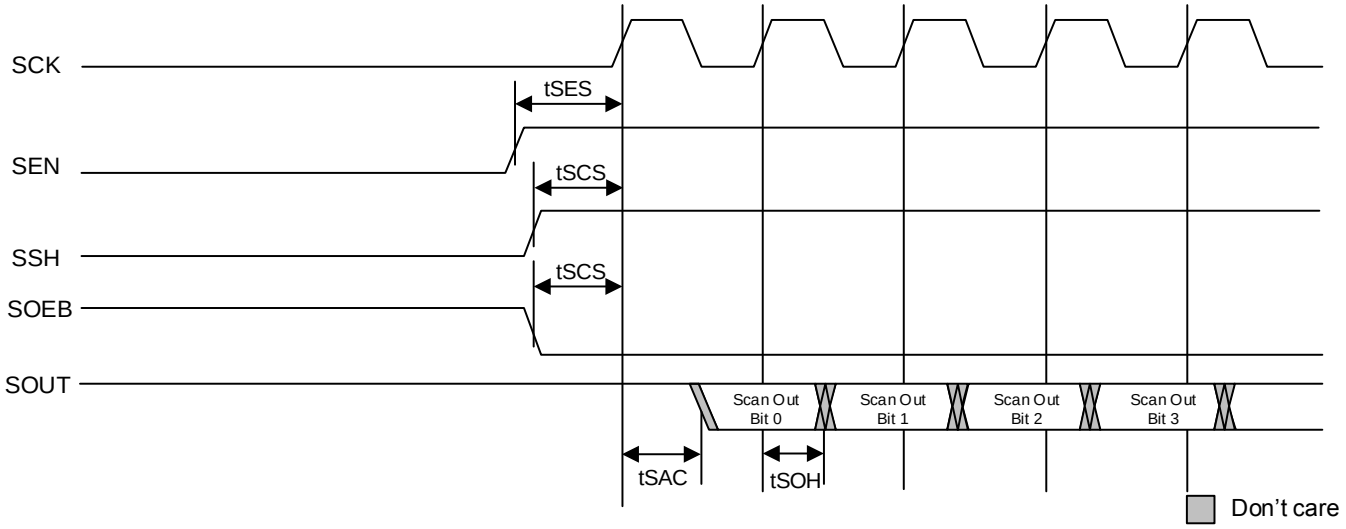
7.4 Exit Sequence

The figure below shows the Scan exit Sequence. This figure show the exiting of the boundary scan functionality in conjugation with the regular LPDDR2 initialization sequence to bring the LPDDR2 again in a well defined state.

Boundary Scan Exit Sequence



7.5 Scan Shift Timing



8. DC ELECTRICAL CHARACTERISTICS CONDITION

PARAMETER/CONDITION	Symbol	Min.	Max.	Units	Note
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF}+0.15	—		1,2
Input Low (Logic 0) Voltage -	V_{IL}(DC)	—	V_{REF}-0.15		1,2

Notes:
1. The parameter applies only when SEN is asserted.
2. All voltages referenced to GND

9. AC ELECTRICAL CHARACTERISTICS CONDITION

Parameter/Condition	Symbol	Min.	Max.	Units	Note
Clock					
Clock cycle time	t_{SCK}	40	—	ns	1
Scan Command Time					
Scan enable setup time	t_{SES}	20	—	ns	1,2
Scan enable hold time	t_{SEH}	20	—	ns	2
Scan command setup time for SSH, SOE# and SOUT	t_{SCS}	14	—	ns	1
Scan command hold time for SSH, SOE# and SOUT	t_{SCH}	14	—	ns	1
Scan Capture Time					
Scan capture setup time	t_{SDS}	10	—	ns	1
Scan capture hold time	t_{SDH}	10	—	ns	1
Scan Shift Time					
Scan clock to valid scan output	t_{SAC}	—	10	ns	1
Scan clock to scan output hold	t_{SOH}	1.5	—	ns	1
Scan Exit Time					
SEN low time	tSN	20	--	ns	

Notes:
1. The parameter applies only when SEN is asserted.
2. Scan Enable should be issued earlier than other Scan Commands by 6 ns.

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
P01	Sep. 6, 2017	All	Initiate the first version