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| --- | --- | --- |
| **Physical category** | | |
| Design Stage | Description | Value |
| Gate-level  Simulation | Cycle time for Gate-level Simulation  (ex. 10ns) |  |
| P&R | Number of DRC violation (ex: 0)  (Verify -> Verify Geometry…) |  |
| Number of LVS violation (ex: 0)  (Verify -> Verify Connectivity…) |  |
| Core area (um2) |  |
| Die area (um2) |  |
| Post-layout  Simulation | Cycle time for Post-layout Simulation  (ex. 10ns) |  |