I^{2}S to PCM Converter Board V2.0 User's Guide

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A. Descriptions

Many people still like the sound of traditional MULTIBIT audio DACs, such as AD1865/62, PCM1704/02, PCM63, TDA1541/A, and many others, because they convert digital music into analog in a different way than popular DELTA-SIGMA DACs.

However, most of those MULTIBIT DACs were designed having to work with digital filter chip through an interface we called "PCM", which transmits left and right data simultaneously. In this case, the problem would be that the sound quality and the maximum Fs of MULTIBIT DACs can be limited by the performance of the hardware based over sampling digital filter chip due to the low internal calculating accuracy, the resource saving interpolating algorithm, and the old higher jitter hardware technology.

In order to boost the sound quality by introducing low jitter technology and to play higher Fs music, we need to get rid of the limitation of that digital filter chip by driving the MULTIBIT DAC from higher performance software base real-time up-sampling filter or high Fs music stream directly. So, we need a jitter optimized device to run MULTIBIT DAC at NOS mode from an I^{2}S bus.

This I^{2}S to PCM converter board was developed exactly for this purpose under the requirement of audiophiles.

B. Features

1. Support 16,18,20,24 bit PCM format output

2. Accept 16 to 32bit I^{2}S input signals with SCK from 32*Fs to 64*Fs

3. Pure NOS mode with bit-perfect format converting

4. High speed design capable for 384KHz Fs with maximum MCLK up to 100MHz

5. Support PCM63,AD1865,AD1862,PCM1704,PCM1702,TDA1541/A and many other classical MULTIBIT DACs

6. Support TDA1541/A working at offset binary mode

7. Jumper selectable full-speed mode and half-speed mode

8. L,R simultaneous timing, launching D/A conversion at same latching edge to eliminate L/R phase difference

9. In order to reduce DAC noise floor, bit clock can be stopped after data shifted into DAC (default)

10. Delayed falling edge of latch enable signal (LLLR) applied to stop clock mode

11. Support dual mono DAC configuration

12. Jitter optimized synchronize logic architecture with last stage high speed low noise re-clocking flip-flops driven by original MCLK

13. With same physical dimensions, it can be assembled stacking on top of the FIFO clock board to save space

C. Principles

I^{2}S to PCM converter board accepts standards I^{2}S signals as input. SCK range can be 32*Fs to 64*Fs. Effective data length can be 16 to 24 bit. MCLK of the I^{2}S is required as well. MCLK range can be 128*Fs to 2048*Fs.

Data length of PCM output can be 16, 18, 20 and 24 bit according to corresponding jumper settings. Frequency of CLK can be set as same as SCK which is full-speed mode (default) or SCK/2 which is half-speed mode.

At STOP CLOCK mode (default), CLK starts at MSB and stops at LSB, it will keep low for the rest of time to silence the PCM interface more. Data will be shifted into DAC register at rising edge of CLK. In order to launch the DAC conversion at a quiet moment, the falling edge of LLLR will be delayed for two clock cycles after CLK stops.
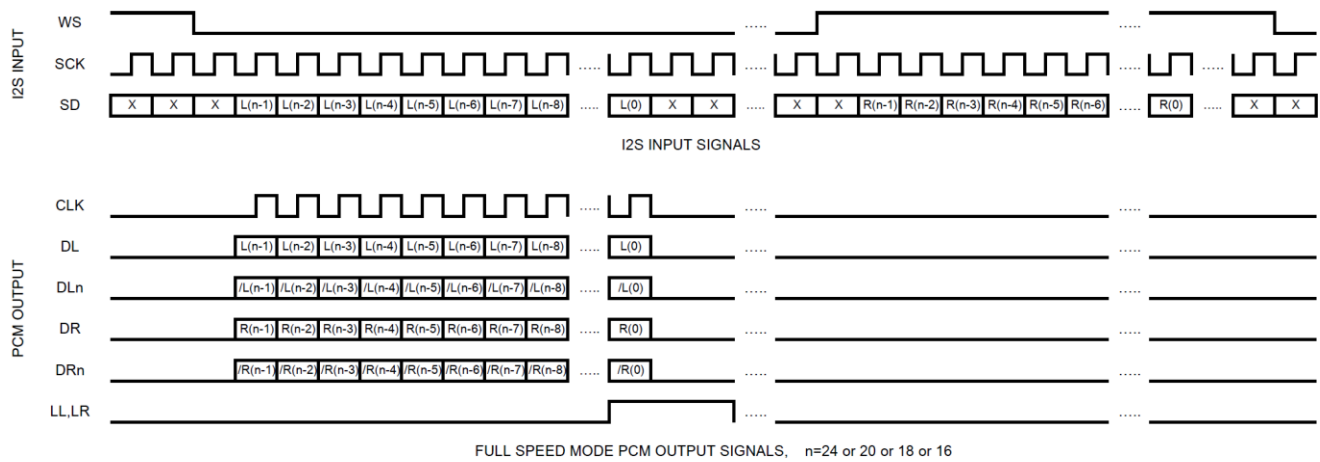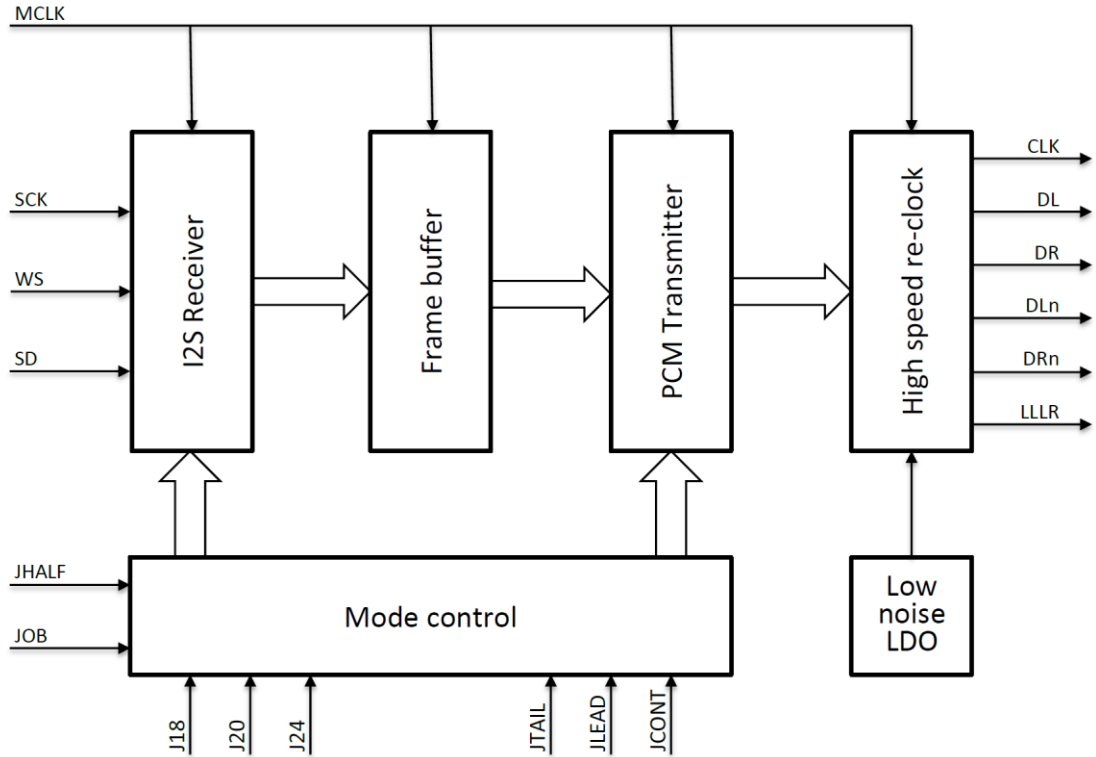
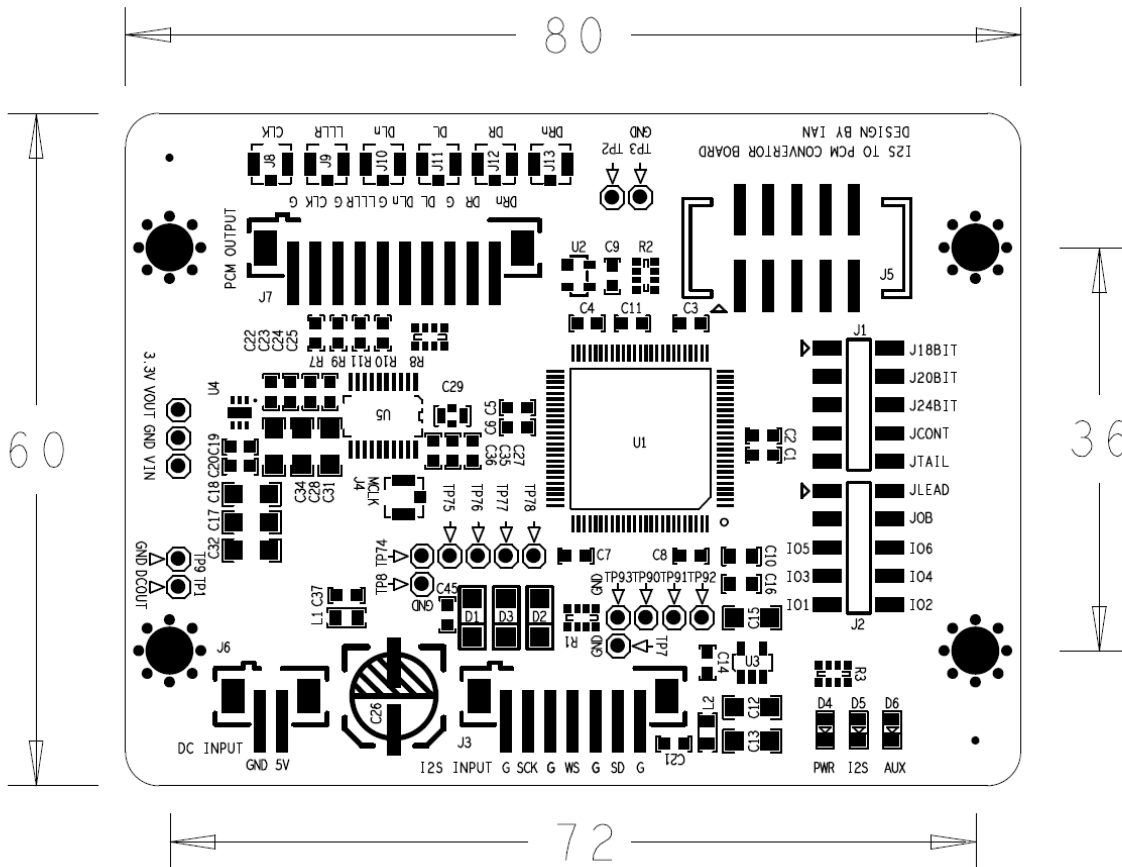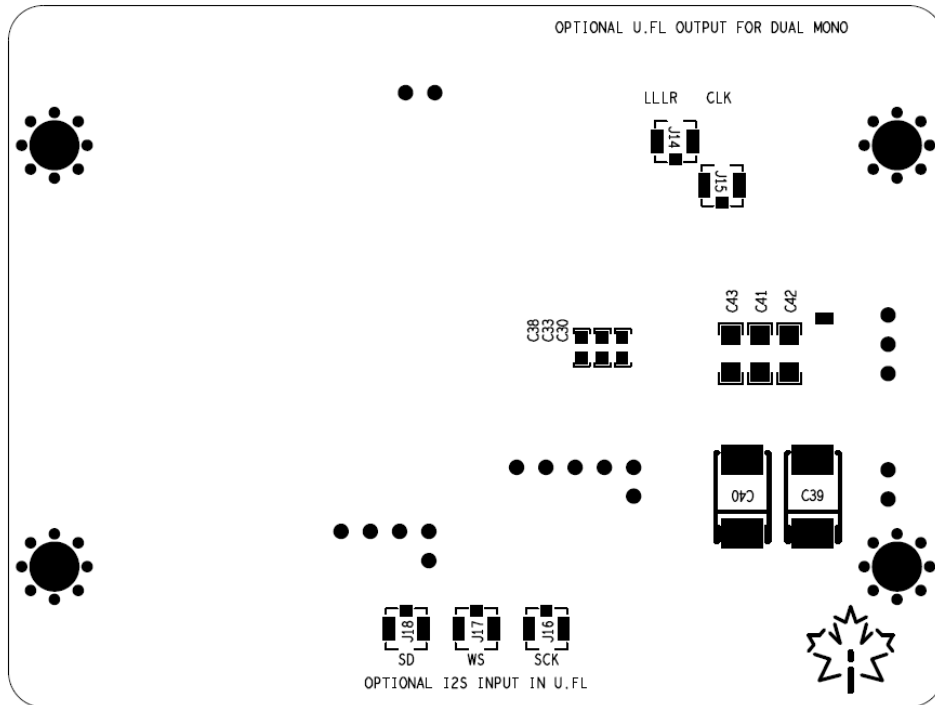Input and output waveform at full-speed mode (default)
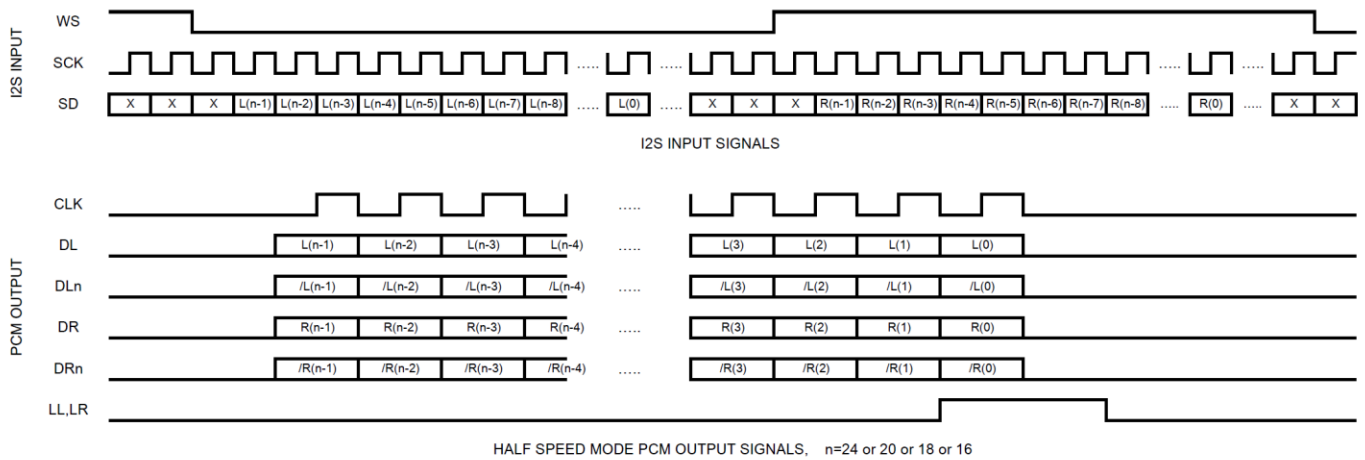
Input and output waveform at half-speed mode

D. Block diagrams

E. Layout and Dimensions (in mm)

（Bottom side）

F. Connectors

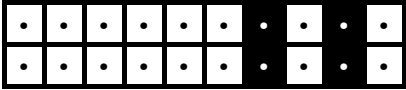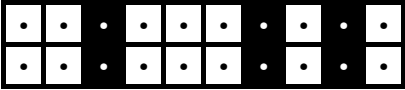| Connector	Description	Notes	Type	Comments
J4	MCLK input	MCLK of I^{2}S source, Frequency range:128*Fs – 2048*Fs	U.FL	3.3V LVTTL logic level
J3	I^{2}S input 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Connecting to I^{2}S source	7P PH2.0mm	3.3V LVTTL logic level Tolerance with 5V TTL logic
J16,J17,J18	Optional I^{2}S input in U.FL connectors	Functional equivalent to J3, just as alternative for better signal quality	U.FL	Optional
J6	DC input 1 – GND 2 – Vcc	Voltage Range: 4V-6V Maximum working current : 50mA	2P PH2.0mm	Need low noise power
J7	PCM output 2 – CLK 4 – LLLR 6 – DLn 7 – DL 9 – DR 10 – DRn 1,3,5,8 – GND	CLK: Data clock LLLR: Latch enable for both left and right DL: Left data DLn: Inverted left data DR: Right daga DRn: Inverted right data	10P PH2.0mm	3.3V LVTTL logic level
J8,J9,J10, J11,J12,J13	PCM output in U.FL connectors	Functional equivalent to J7, just for better signal quality	U.FL	Optional, but recommended
J14,J15	Additional LLLR and CLK in U.FL for dual mono configuration	Functional equivalent to J9 and J8, But come from separate matching resistors	U.FL	Optional, but recommended

G. Jumper settings

Jumper	Descriptions	Settings	Functions	Comments
J18BIT J20BIT J24BIT	PCM data length setting	J18BIT jumped only	18 bit PCM output	
		J20BIT jumped only	20 bit PCM output	
		J24BIT jumped only (default)	20 bit PCM output	
		All three keep open	16 bit PCM output	
		All other settings	Invalid	Avoid
JHALF (IO5 & IO6)	Full/Half speed mode setting	Open (default)	Full-speed	Preferred
		Jumped	Half-speed	Only for low speed DAC
JOB	Output format setting	Open (default)	Two's complement	Apply for most of DACs
		Jumped	Offset binary	For TDA1541/A only
JCONT	STOP or continuous CLK mode	Open (default)	STOP CLK mode	
		Jumped	Continuous CLK mode	Not recommended /For PCM1702 only
JTAIL	Optional CLK extension	Open (default)	Disable	
		Jumped	Add two more clocks before CLK stopped	For PCM1704 only
JLEAD	Optional warm-up CLK	Open (default)	Disable	
		Jumped	Add one more clock before CLK starts	Not recommended

H. LED indicators

| Jumper	Descriptions	Notes
PWR	Power indicator	'On' indicates the board is powered
AUX	MCLK status at start up	'Off' indicates no MCLK signal after power up (Will not back to off if the MCLK is gone later on)
I^{2}S	I^{2}S input status	'On' indicates I^{2}S input signals are good

I. Possible jumper settings for MULTIBIT DACs

| DACs	Full-speed mode jumper settings	Half-speed mode jumper settings
AD1865	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT
AD1862	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT
PCM1704	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT
PCM63	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT
PCM58	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT
TDA1541 TDA1541A	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT	IO1-2, IO3-4, JHALF, JOB, JLEAD, JTAIL, JCONT, J24BIT, J20BIT, J18BIT

DACs	Full-speed mode jumper settings	Half-speed mode jumper settings
PCM1702	IO1-2 IO3-4 JHALF JOB JLEAD JTAIL JCONT J24BIT J20BIT J18BIT	IO1-2 IO3-4 JHALF JOB JLEAD JTAIL JCONT J24BIT J20BIT J18BIT

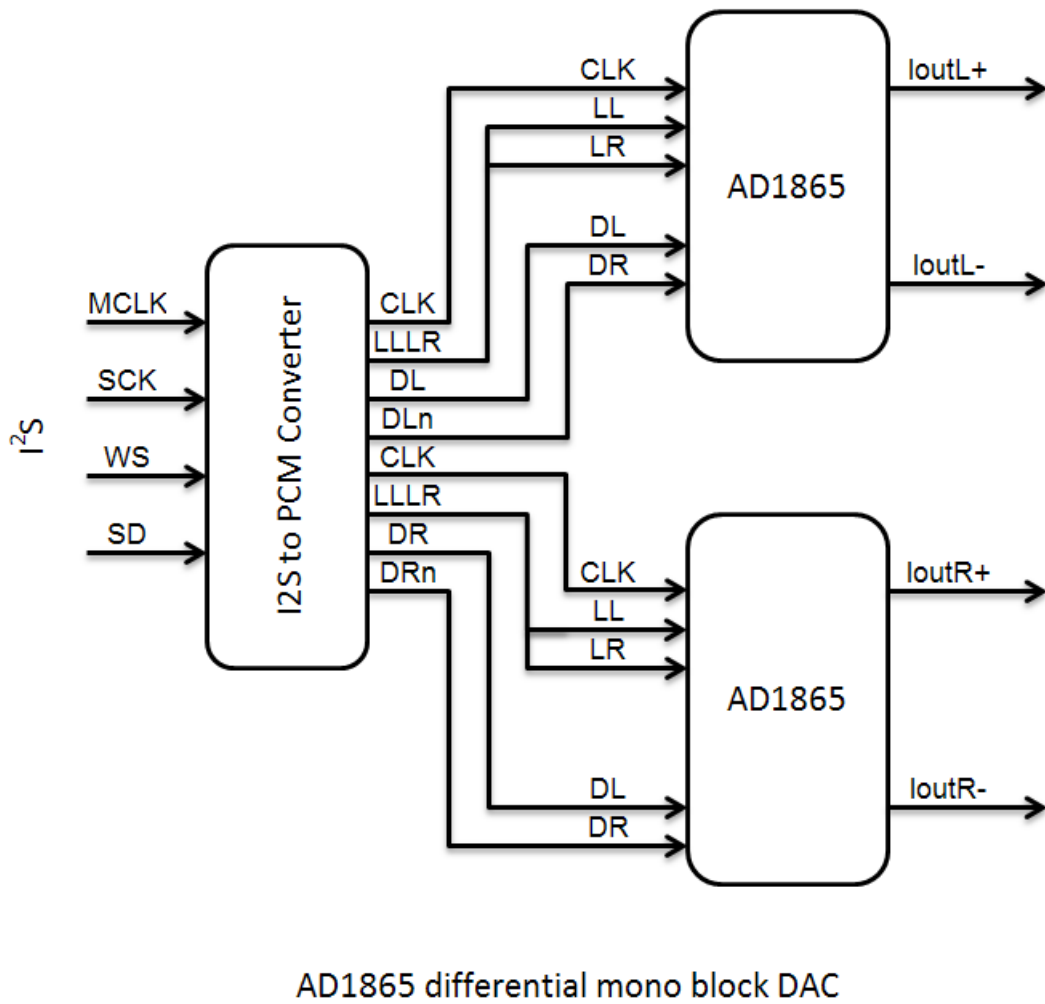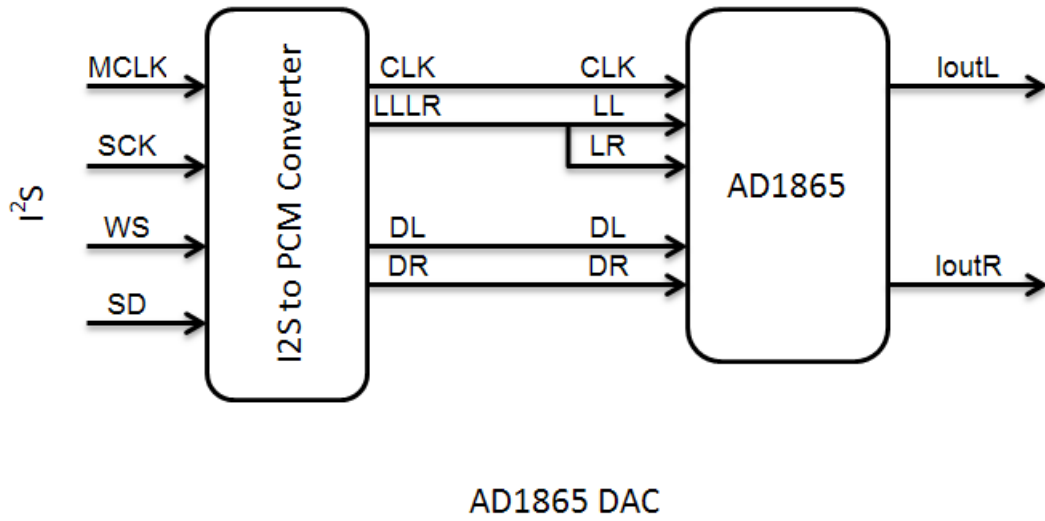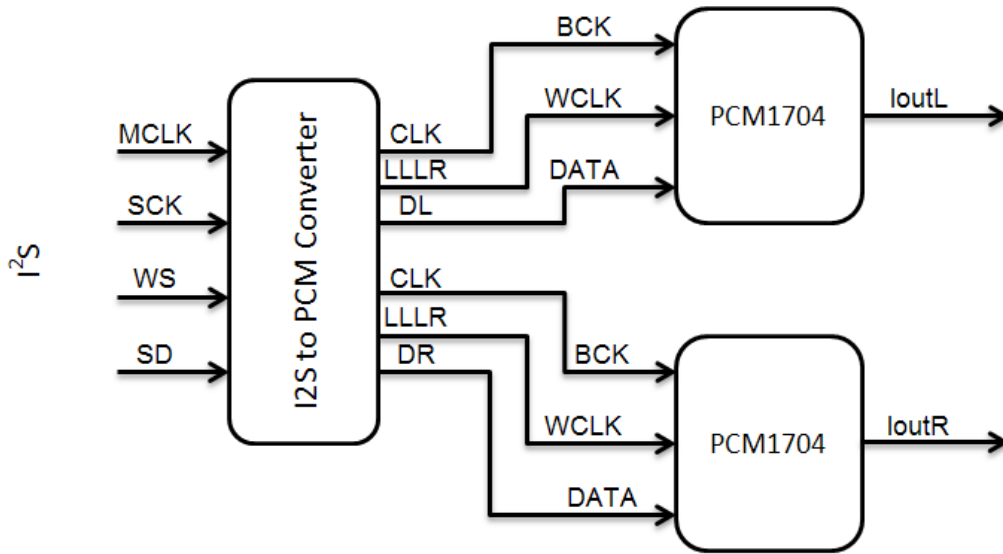## J. How to Integrate I^{2}S to PCM converter board into DAC system
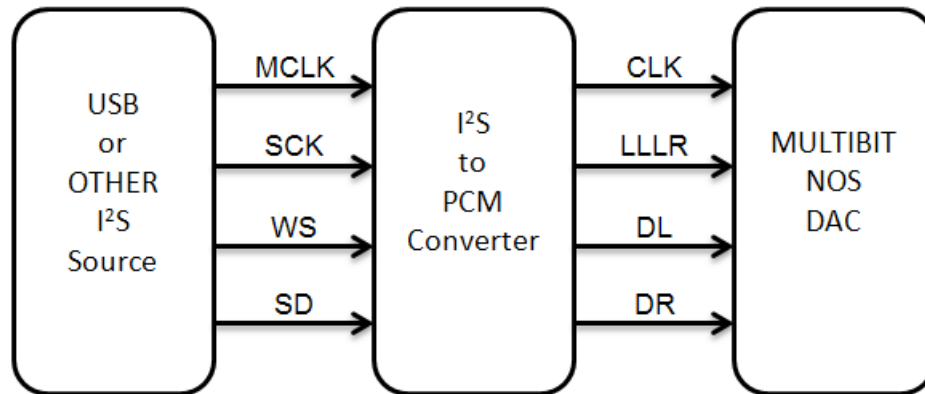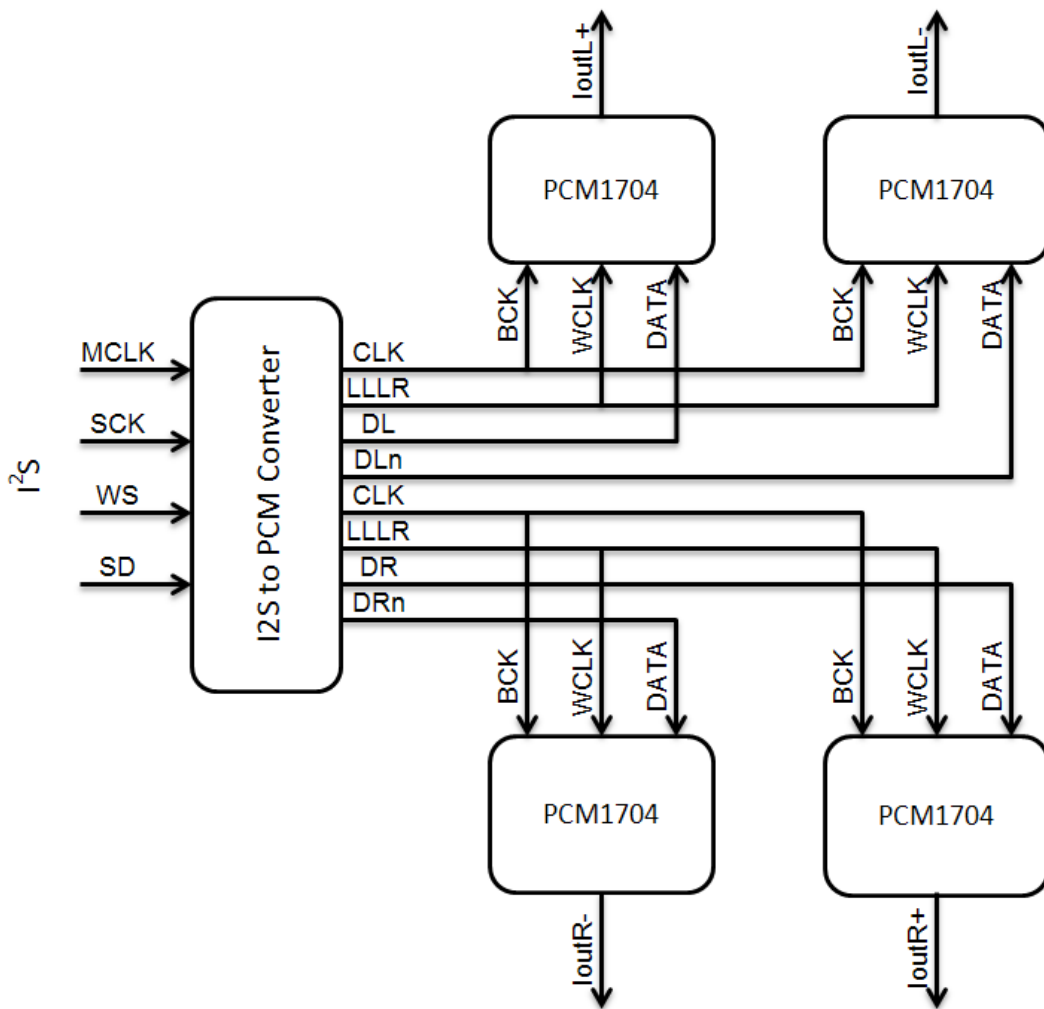
Integrated with USB or other I^{2}S source directly
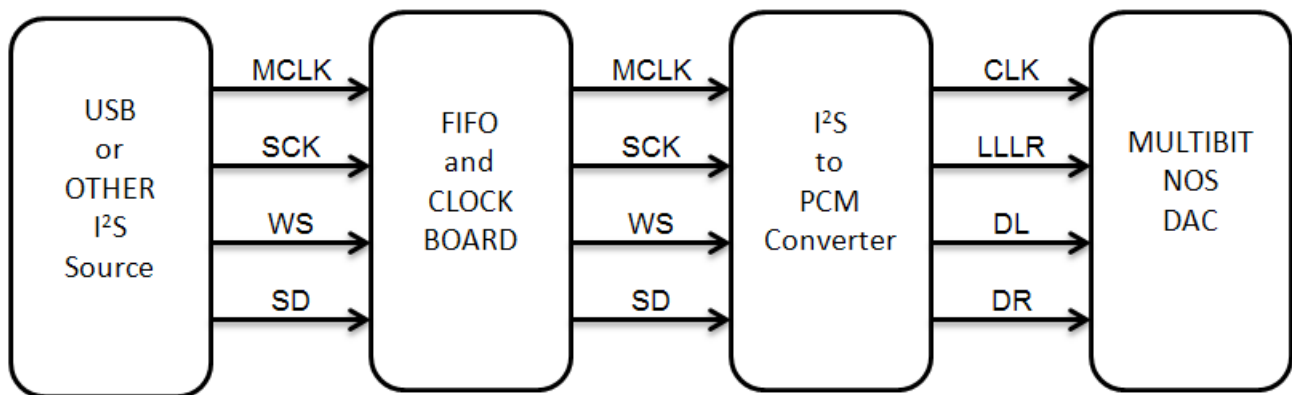
Integrated with USB or other I^{2}S source through FIFO KIT

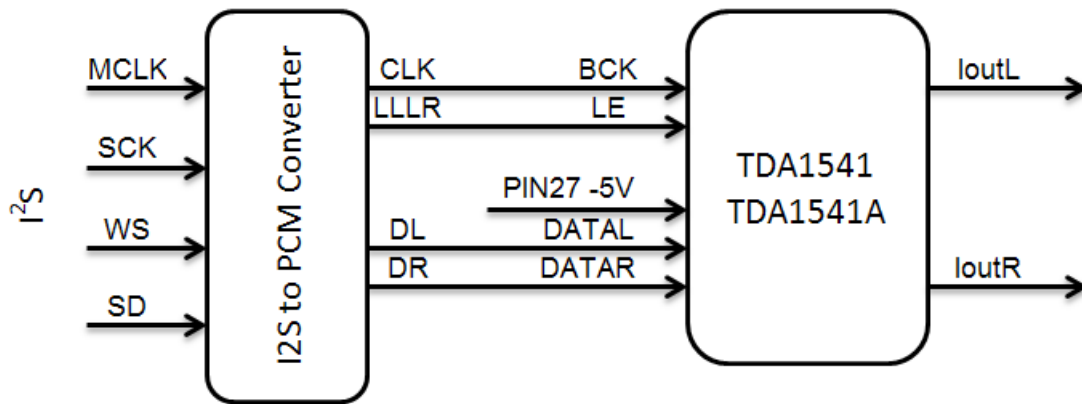## K. Possible connections to some typical NOS MULTIBIT DACs

AD1865 DAC

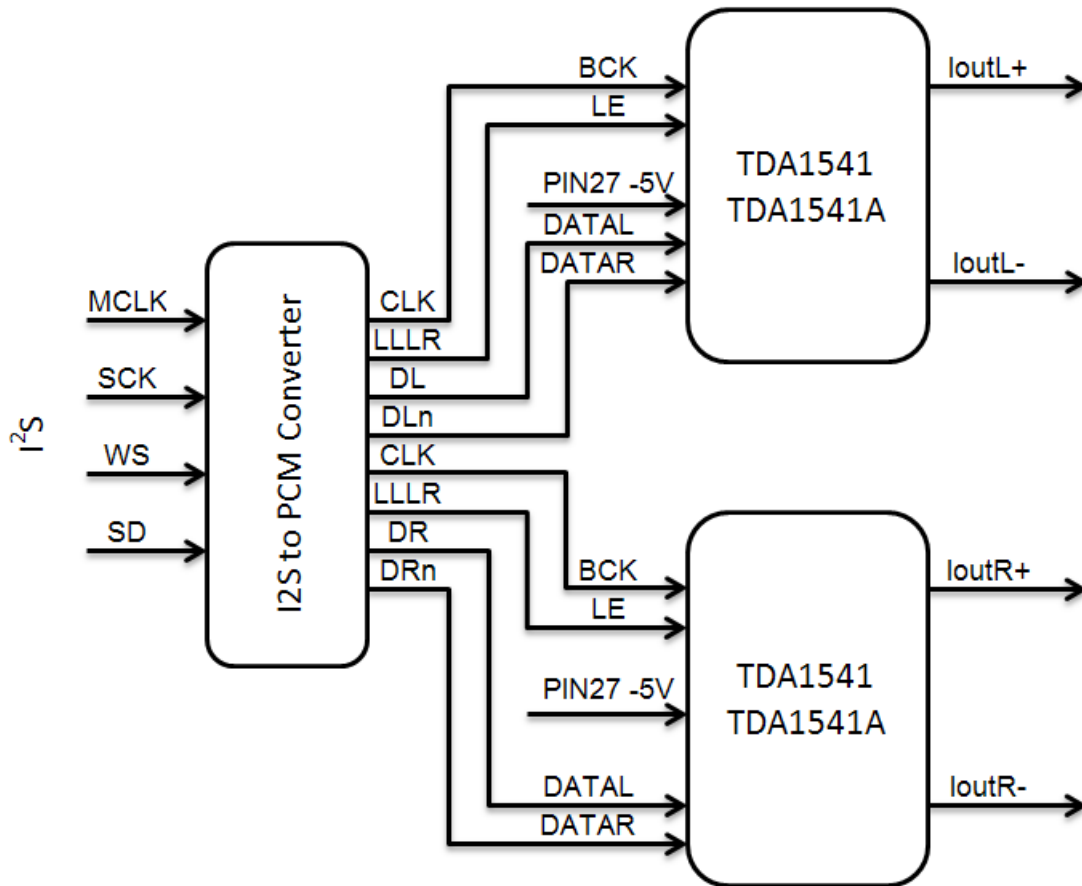
AD1865 differential mono block DAC
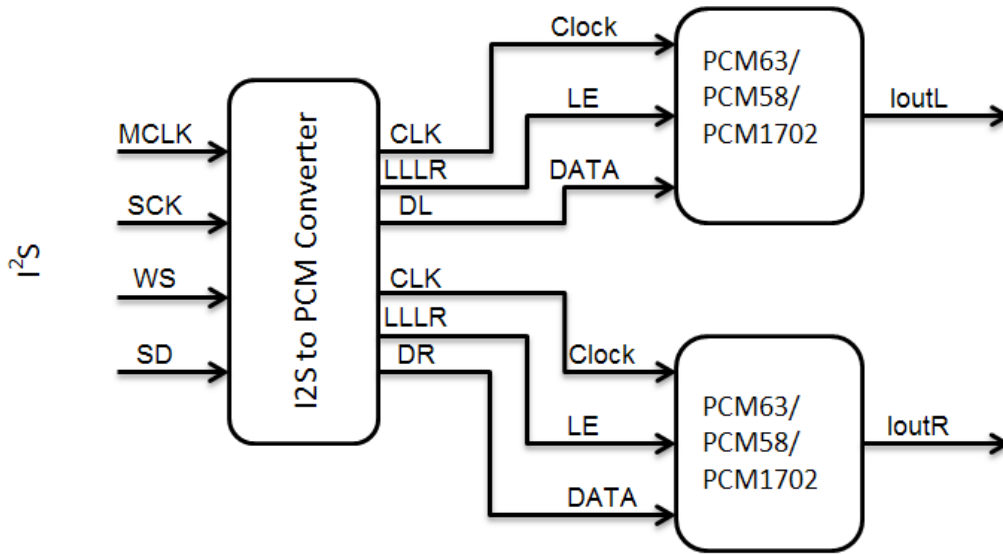
PCM1704 mono block DAC

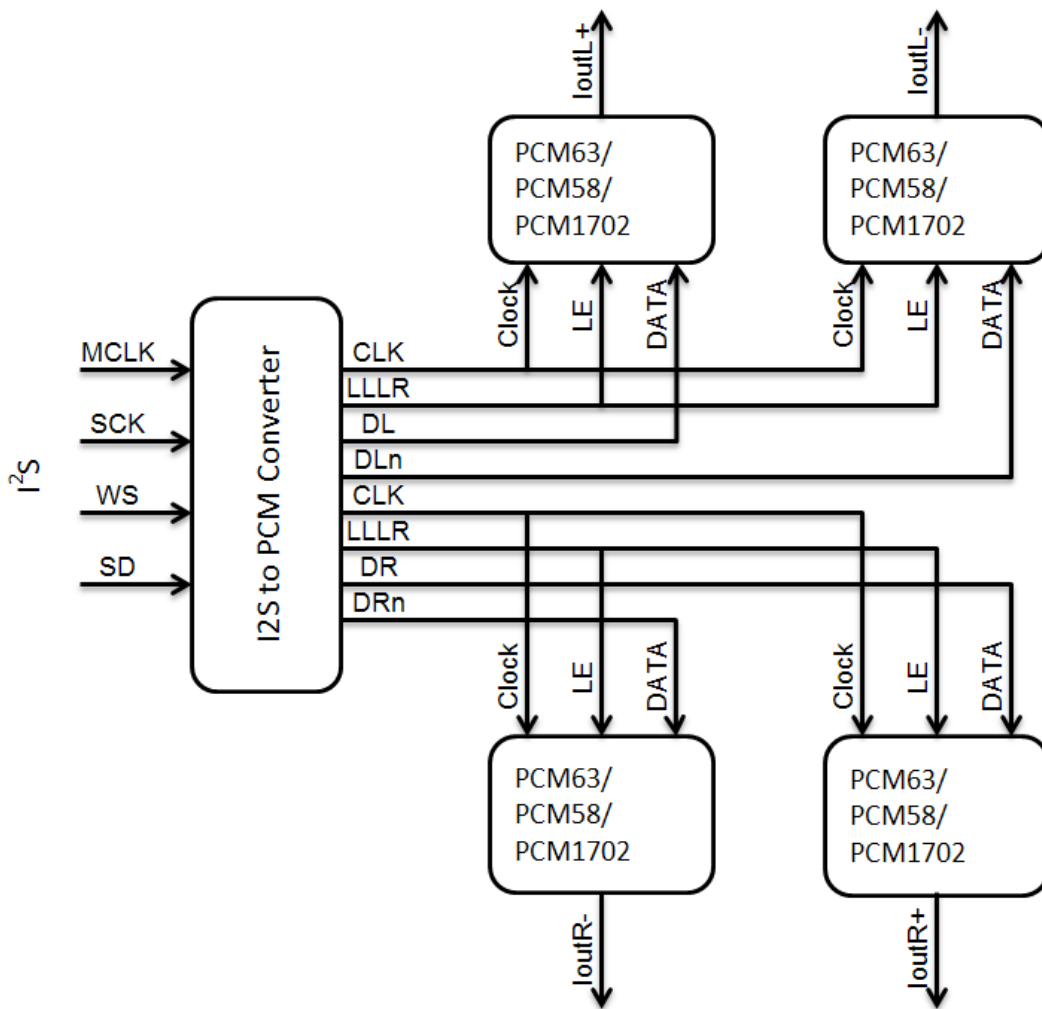PCM1704 differential dual mono block DAC

TDA1541/A DAC

TDA1541/A differential mono block DAC
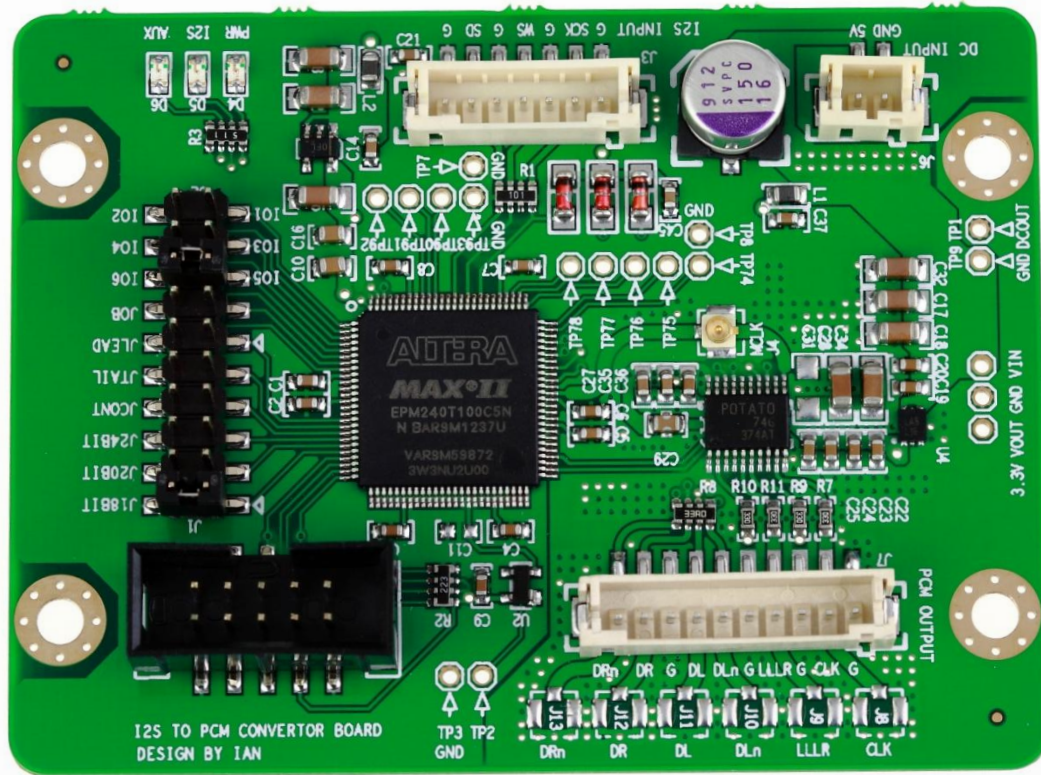
PCM63/PCM58/PCM1702 mono block DAC

PCM63/PCM58/PCM1702 differential dual mono block DAC

L. Application Notes and Tips

1. Though the I²S to PCM converter board works with most of standard I²S sources, including a FIFO KIT with low jitter clock into system is still highly recommended to optimize sound quality. Clock board should be placed as close as possible to the converter board.

2. Half-speed mode was specially designed to run some old MULTIBIT DACs at higher Fs. If both half-speed mode and full-speed mode work for your DAC in your application, please choice the full-speed for more silence time on PCM signal.

3. Please note that the minimal frequency of MCLK is limited to 128*Fs. If you want to run 384KHz Fs, the MCLK has to be 49.152MhzMHz or 98.304MHz, and so on.

4. The maximum BCK or CLK frequency of your DAC may limit the highest Fs of your system. Some of those DAC can be over clock a little bit, but it would be highly up to specific DAC chips, your system design, layout, power supply and the clock signal quality.

5. This I²S to PCM converter board was designed running MULTIBIT NOS DACs in an innovative way for last drop of juice. New technologies were introduced to maximize the sound quality, such as stopping clock and delayed latching enable. Although we confirmed AD1865, PCM1704 and TDA1541/A running perfectly with it, but I still couldn't guarantee it works with all kind of old MULTIBIT DACs.

6. Jumpers of continuous clock, lead clock and tail clock were reserved for some special case or debugging purpose. They are not recommended for normal applications.

7. For better signal quality, U.FL cables are recommended connecting to DAC. Please use cables with same length for dual mono configuration to reduce the skew between channels.

8. The on-board low noise LDO is LP5900SD-3.3/NOPB. VIN, GND and 3.3V VOUT pins are reserved for external regulator. Please disassemble the LP5900 in advance if you want to use the external low noise regulator.

9. You can also run this I²S to PCM board by a 3.2V LifePO4 battery cell. By shorting VIN and VOUT with a jumper, you can feed the battery power directly from DC input J6.

10. The logic level of all output signals of this I²S to PCM board is 3.3V LVTTL. Though all of 5V DACs we tested allow LVTTL levels on their digital inputs, you have to make sure yours too: in your DAC data sheet check if digital input VIH (High) minimum level is +2.0V.

11. Names of I²S signals in this document are from 'I²S bus specification'. Other possible names may apply to same signals.

Signal descriptions	Signal names in this Document	Other possible signal names
Master clock	MCLK	SCK
Bit clock	SCK	BCK
Word clock	WS	LR, LRCK
Serial data	SD	DATA,DIN

M. Picture of I²S to PCM converter board