McFIFO multi-channel I2S/DSD FIFO user's guide

By Ian Jin, May 30, 2017 Ver. 1.0b

A. Introduction

The digital audio stream consists of two parts: the data and the clock. Usually we don't have any problems with data. However, the clock is not perfect (there are no ideal clocks in the real world); it comes with jitter (or phase noise). Jitter is the main reason why different digital audio sources sound different even when they are played from the same audio stream.

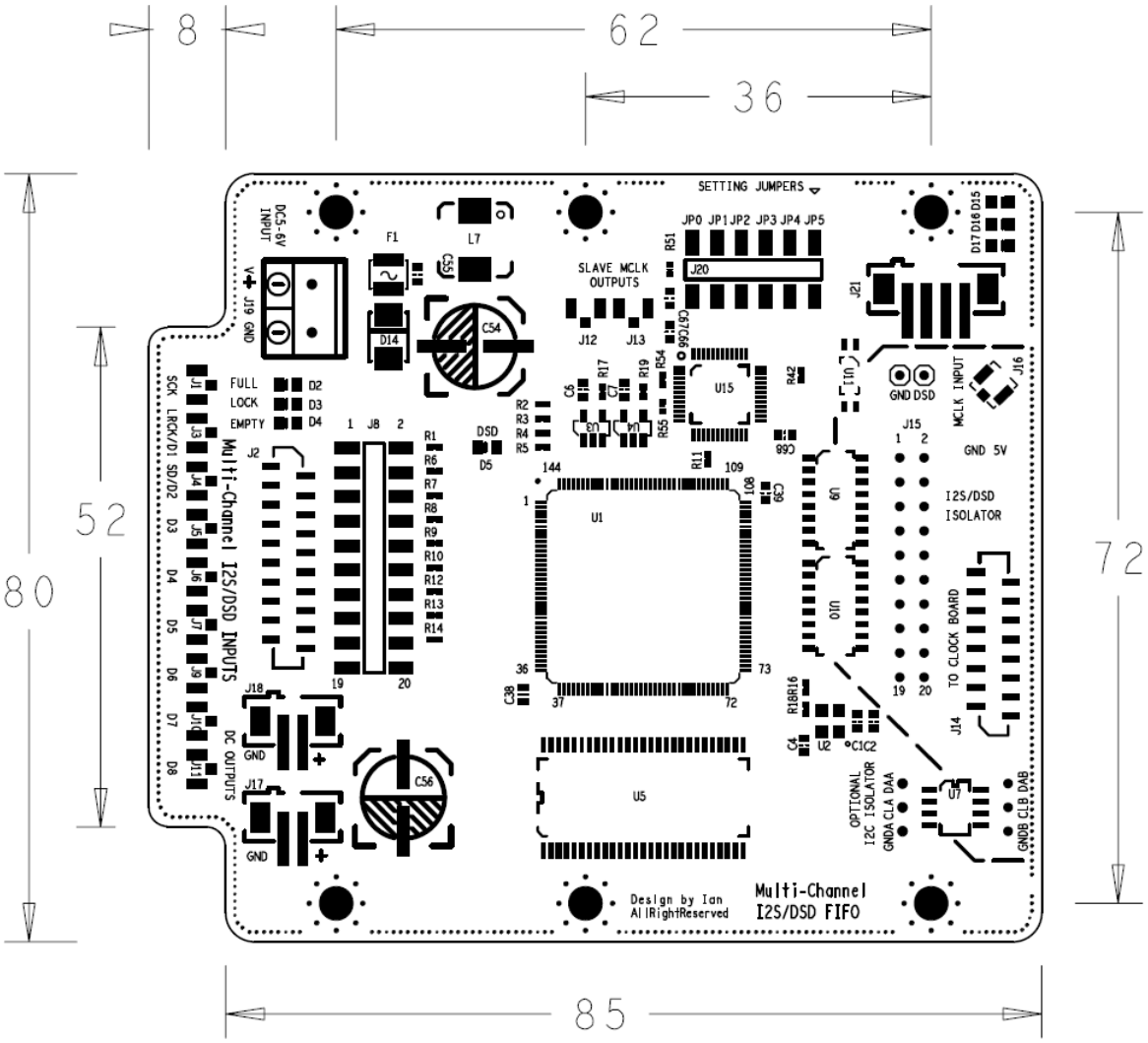
McFIFO is an asynchronous multi-channel I2S/DSD FIFO. It is a kind of logic device which can buffer the digital audio stream, allowing the audio data to pass through while isolating the original clock and replacing it with a new secondary clock. If the new clock has less phase noise than the old one, the digital audio stream after the McFIFO will have less jitter and that will make the DAC or other digital audio device playing the stream sound better. Moreover, the sound quality of the playback will be independent from the digital audio source.

This McFIFO II KIT is based on the third generation of Ian FIFO technology. So, together with good low jitter audio clocks, it is firmly believed to be one of the most effective solutions to improve sound quality of digital audio applications such as home theatre, digital crossover, multi-DAC system and stereo I2S/DSD DAC.

B. Features and Specifications

- 256Mb buffer memory.
- Audio MCLK up to 98.3040 MHz.
- Multi-channel I2S support from 44.1KHz/16bit to 384 KHz/32bit; Multi-channel DSD support from DSD64 to DSD512. Automatically detecting I2S/DSD.
- Seven data signals for I2S and eight data signals for DSD. Capable for 14 channels when play I2S and 8 channels when play DSD.
- Built in multi-channel digital isolator.
- Adjustable McFIFO delay time. Can be set to 0.1, 0.2, 0.4 and 0.8 second by setting jumpers, or continue adjustment by external control panel. Delay time keeps the same for different Fs.
- Has both master and slave clock control mode, slave MCLK is available to be fed back to digital sources such as USB streamer, S/PDIF receiver, RaspberryPi and BeagleBone Black.
- Support optional external display/control panel. It can be an open source Arduino based project.
- Isolated DSD detecting signal.
- Optional I2C isolator for DAC control.
- Works with McDualXO clock board, third party clock board or DAC local XOs.

C. Layout and Dimensions (in mm)



D. Connectors

-DC power input: J1,

A 5V-6V DC power supply must be connected to this 2-pin 5.0mm terminal for the McFIFO to operate. McFIFO consumes around 160mA average current with 49.1520MHz MCLK. It could be a little bit higher when works with higher frequency MCLK, for example 98.3040MHz. You MUST add this to the current required by devices powered from McFIFO to determine the minimum current output for your power supply. Generally use a supply that provides 500mA as a minimum.

-Three multi-channel I2S/DSD input ports

1. U.FL multi-channel coaxial cable sockets, configured as:

J1	J3	J4	J5	J6	J7	J9	J10	J11
SCK	LRCK/D1	SD/D2	D3	D4	D5	D6	D7	D8

2. J8, 20pin 2.54mm multi-channel input connector

1	3	5	7	9	11	13	15	17	19
SCK	LRCK/D1	SD/D2	D3	D4	D5	D6	D7	D8	SLEN*
2	4	6	8	10	12	14	16	18	20
GND	GND	GND	GND	GND	GND	GND	GND	GND	XOSEL*

*see master and slave clock control section for details.

3. J2, 20pin 1mm FFC/FPC connector
   Reserved for multi-channel interface board

Notes:

- All input signals are in LVTTL (3.3V) logic level with 5V TTL tolerant
- McFIFO detects I2S/DSD automatically. They share same input port.
- Three multi-channel input ports are identical, so only one input port can be used at same time.

- Isolated MCLK input in U.FL: J16

Input isolated MCLK from McDualXO clock board, other clock board or DAC.

MCLK frequency range: from 5.6448MHz to 98.3040Mhz

MCLK level: LVTTL (3.3V) logic level

- SLAVE MCLK output in U.FL: J12, J13

Output SLAVE MCLK to digital music sources.

SLAVE MCLK frequency can be set by jumpers range from 2.8224MHz to 98.3040Mhz

SLAVE MCLK level: LVTTL (3.3V) logic level

-Two isolated multi-channel I2S/DSD output ports

1. J14, 16pin 1mm FFC/FPC connector
   Dedicated for McDualXO multi-channel clock board

2. J15, 20pin 2.54mm isolated multi-channel output connector

1	3	5	7	9	11	13	15	17	19
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
2	4	6	8	10	12	14	16	18	20
SCK	LRCK/D1	SD/D2	D3	D4	D5	D6	D7	D8	XOSEL

Notes:

- All multi-channel I2S/DSD signals are isolated from McFIFO ground and signals.
- Output signals are in LVTTL (3.3V) logic level
- J14 and J15 are identical, so only one can be used at same time. Basically J14 is for McDualXO while J15 is for third party clock board or DAC
- J15 is not installed as supplied, please install a 20-pin 2.54mm connector or separate pins as needed.
- If don't use J14, an isolated 5V DC power supply has to be applied to the reserved 5V and GND pins in the I2S/DSD isolator section to provide power for isolator chip.

-Isolated DSD detecting output

This DSD signal is in isolator section. It's isolated from McFIFO ground and with open drain output. Logic high means McFIFO is running in DSD mode. This signal will be used only when DAC cannot detect DSD format.

-External Display/Control Panel connector J21

4pin PH2.0mm connector

1	2	3	4
GND	RXd	5V	TXd

-5V DC power output J17, J18

2pin PH2.0mm connector.

J17 and J18 are identical. They are from DC power input with CLC filter.

1	2
GND	5V

E. Jumper settings

JP0, JP1: FIFO delay time

JP0	JP1	Delay (s)
OPEN	OPEN	0.2s (default)
OPEN	SHORT	0.1s
SHORT	OPEN	0.4s
SHORT	SHORT	0.8s

JP3, JP4: SLAVE MCLK frequency

JP3	JP4	SLAVE MCLK frequency
OPEN	OPEN	MCLK/1
OPEN	SHORT	MCLK/2
SHORT	OPEN	MCLK/4
SHORT	SHORT	MCLK/8

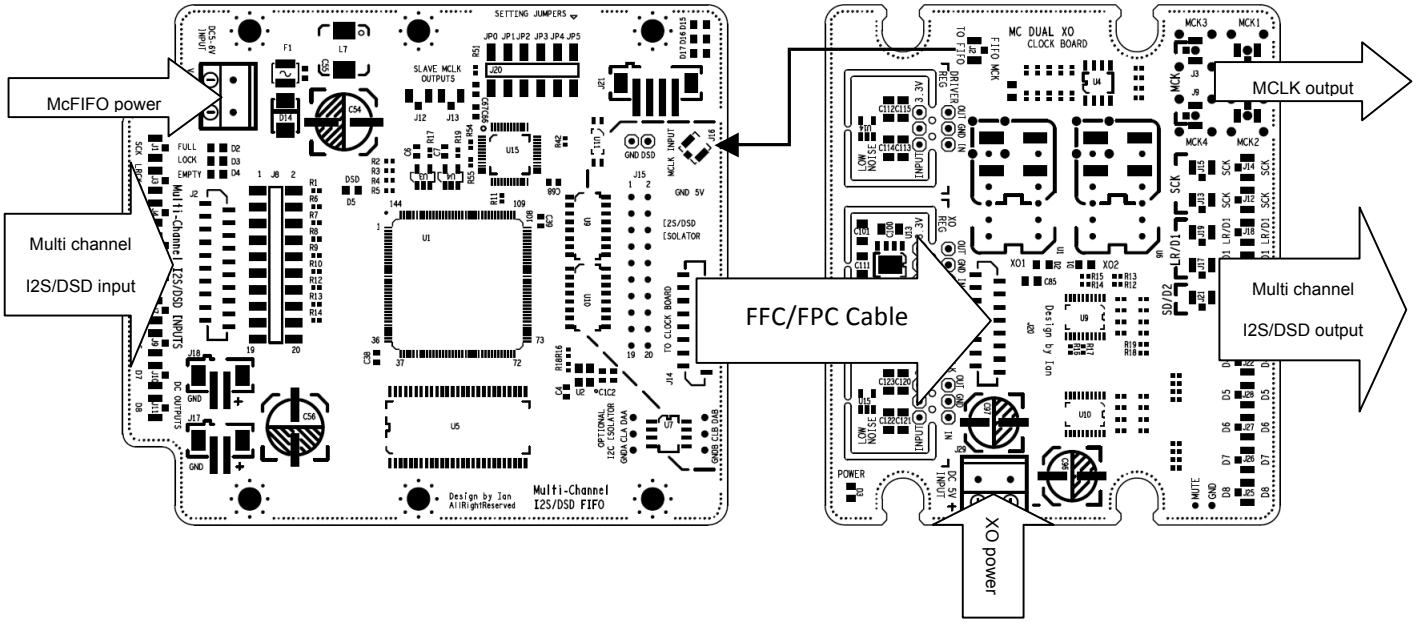
JP2, JP5: Reserve for later upgrade, keep open for now

F. LED indicators

LED	Descriptions	Notes
D2	FULL	On or flashing when McFIFO is full
D3	LOCK	On when McFIFO is locked with the input music stream
D4	EMPTY	On when McFIFO is empty
D15	POWER	On when McFIFO is powered
D16	STATUS	Reserved for future upgrade
D17	STATUS	Reserved for future upgrade

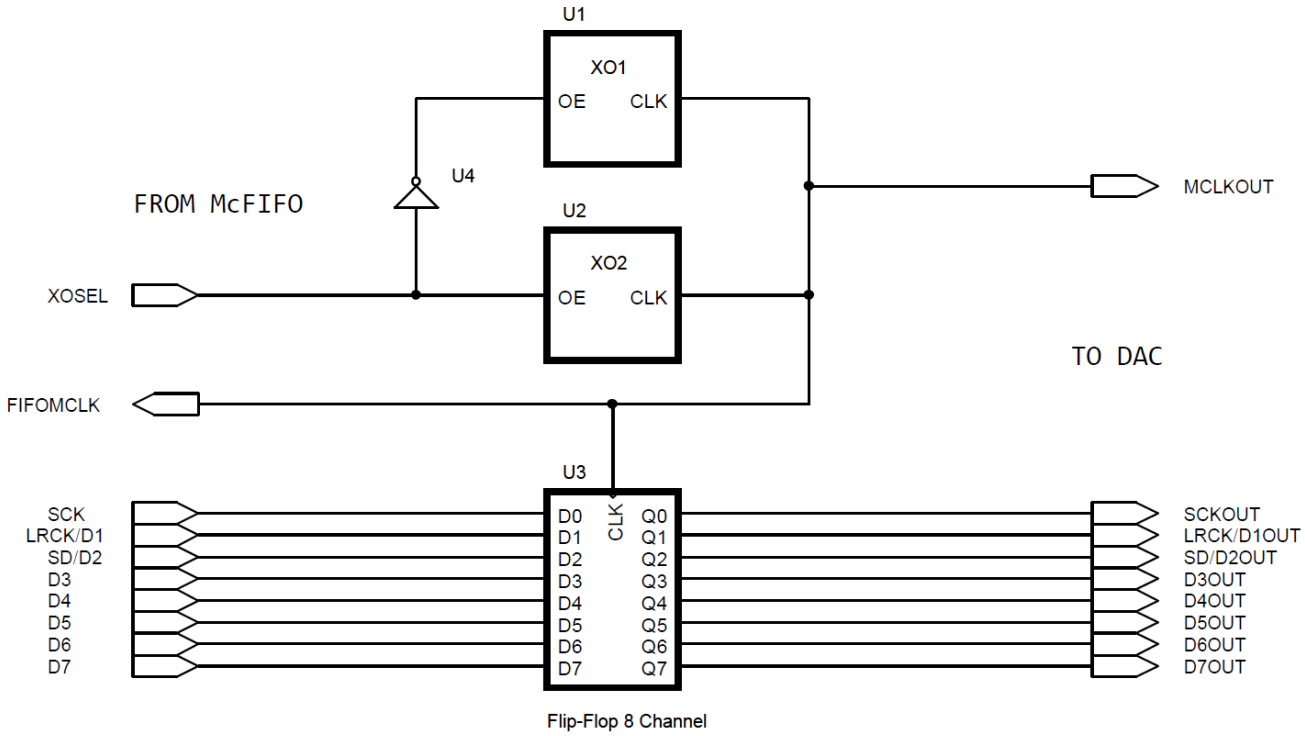
G. Working principle

-Working with McDualXO clock board (default)



-Working with third party clock board

McFIFO can work with third party clock board. Please refer to the schematic blow for the operating logic of that clock board. In this case, a 5V DC power supply must be connected to TP9(5V) and TP11(GND) to power the right side of the on-board isolator. Third party clock board normally connects to McFIFO through J15.



Flip-Flop 8 Channel

-Working with DAC that has local XOs

McFIFO can also work with DAC that equipped with local XOs. In this case, the above clock board logic has to be integrated into DAC design. Please make sure a 5V DC power supply is connected to TP9 (5V) and TP11 (GND) to power the right side of the on-board isolator.

H. Application Notes and Tips

-McFIFO delay time

Based on the most advanced FIFO memory management technologies, McFIFO is capable for the adjustable delay time. Four delay time settings can be set by jumpers. Continuous adjustment is also possible by external control panel upon later on upgrade. Delay time decides by FIFO buffer memory size. Shorter delay time is good for audio/video applications; while longer delay time will have more tolerance with input music stream frequencies thus better sound quality is expected. The delay time settings will be applied the same to different sample frequencies and formats. For example, if we set the delay time to 0.2 second, music no matter in 44.1 KHz, 384 KHz or in DSD256, will all have the same 0.2 second delay time. Please choose the most suitable delay time according to your preference and your application.

-Music formats support

McFIFO supports almost all kinds of music formats. Such as, but not limited to I2S 16bit, I2S 24bit, I2S 32bit, DSD, left-justified, right-justified. McFIFO is a pure bit-perfect device. It follows "What input is what output" principle. McFIFO will focus on its main business without doing any additional converting or processing to the original music format.

-External display/control panel

An external McFIFO display/control panel can be connected to J21 to display information or perform control.
The following information will be shown on the display:

1. XO1 and XO2 frequency measurement results.
2. Current XO selection.
3. Input format(I2S or DSD).
4. Input Fs measurement result.
5. McFIFO status: LOCKED,UN-LOCKED,EMPTY,NO SIGNAL.
6. Delay time.

An open source Arduino based McFIFO display project is available for download on GitHub
https://github.com/iancanada/McFIFOdisplay
Dedicated McFIFO display/control panel is also possible to be developed for future upgrade.
*Internal frequency measurement result accuracy has 15ppm tolerance

-Master and slave controlled MCLK

McFIFO was set to master controlled MCLK mode by default. This is the normal operating mode of the McFIFO. In this mode, McFIFO will decide which XO is selected for MCLK according to input music.

However, McFIFO can also work with digital audio sources that have master clock mode. For example, USB streamer with two on board XOs. To implement this, we need to enable McFIFO's slave controlled MCLK mode. In this mode,

XO selections will be controlled by digital audio source. SLAVE MCLK will be fed back to digital audio source from McFIFO as world master clock. Frequencies of SLAVE MCLK can be set by jumper settings. To do so, we need a couple of steps :

1. Enable slave controlled MCLK mode by driving SLEN pin on J8 to logic high.
   SLEN=0 (OPEN without connection, default): master controlled MCLK mode
   SLEN=1: slave controlled MCLK mode
2. Connect XO selection signal from digital audio source to XOSEL pin on J8.
   XOSEL=0: XO1 is selected
   XOSEL=1: XO2 is selected
   (XOSEL pin can be left open if not in slave controlled mode by default)
3. Remove the two XOs from digital audio source. Connecting SLAVE MCLK from McFIFO to the finial output for that two XOs. J12 and J13 are equivalent (but with different driver), so either of them can be used for this purpose. U.fl coaxial cable is used to improve clock quality.

*Very short delay time can be used for this slave controlled MCLK mode because McFIFO and digital audio source have already been synchronized in between.

-Re-map input channels

Besides of the SCK and LRCK/D1, all other data channels are equivalent in functions. So all of those input data channels can be re-mapped or duplicated if required by applications. Re-mapping can be implemented either by multi-channel digital source or by input cables. Duplicating channels can be easily done by wire jumpers on J8. Please make sure all outputs are connected correctly corresponding to the input signals.

-Stereo applications

Of course McFIFO works for stereo applications. Since more data channels are available, McFIFO will have more flexibility and easier setup on stereo applications such as dual mono block DACs, multiple DACs and DSP based digital crossover project.

-I2C isolator

McFIFO has a reserved I2C isolator to provide isolated digital control path for DACs such as ES9018 and many others. To use this I2C isolaotr, you need to connect I2C bus of DAC to CLB, DAB and GNDB, I2C bus of the controller to CLA, DAA, and GNDA.

I2C isolator chip U7 is not installed as supplied. You have to do SMT assemble of it if you want this function. The part number is I2C isolator is: Si8600AB-B-IS

I. McFIFO picture