CYCLONE V GPU SCHEMATICS

RE	EVISIONS
.0 -	Initial draft
.1 -	Replaced MAX5101 DAC with PCM5101A. Replaced wire-wound chokes with fixed inductors.
2	Added decoupling and supply isolation for TFP410.
3 -	Removed decoupling and supply isolation for TFP410. Added external memory.
	10u caps and 100k pull-downs added to audio DAC output. Fixed micro-SD pullups. Corrected DDR-RAM clock pins. Variable-voltage added to U19.

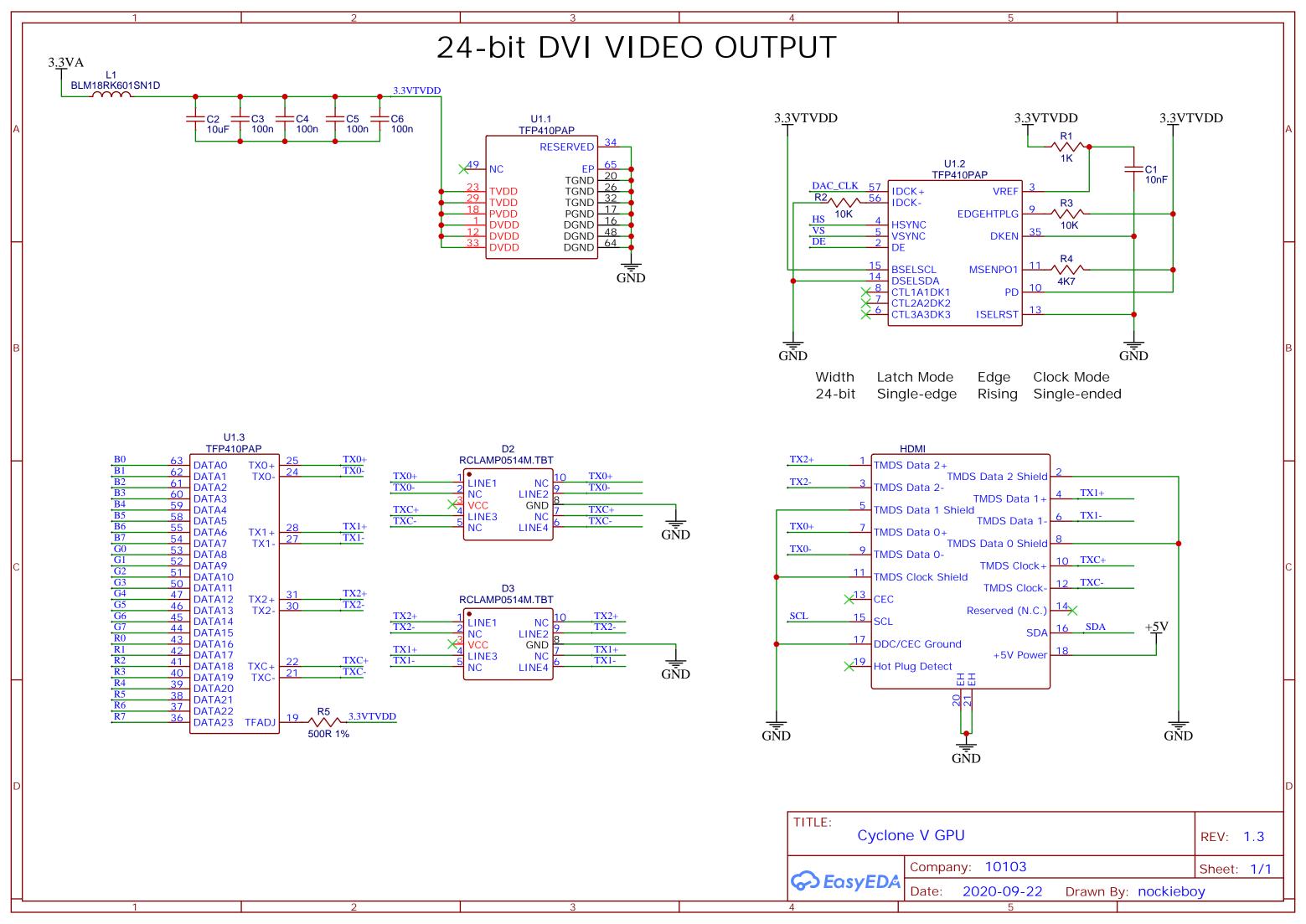
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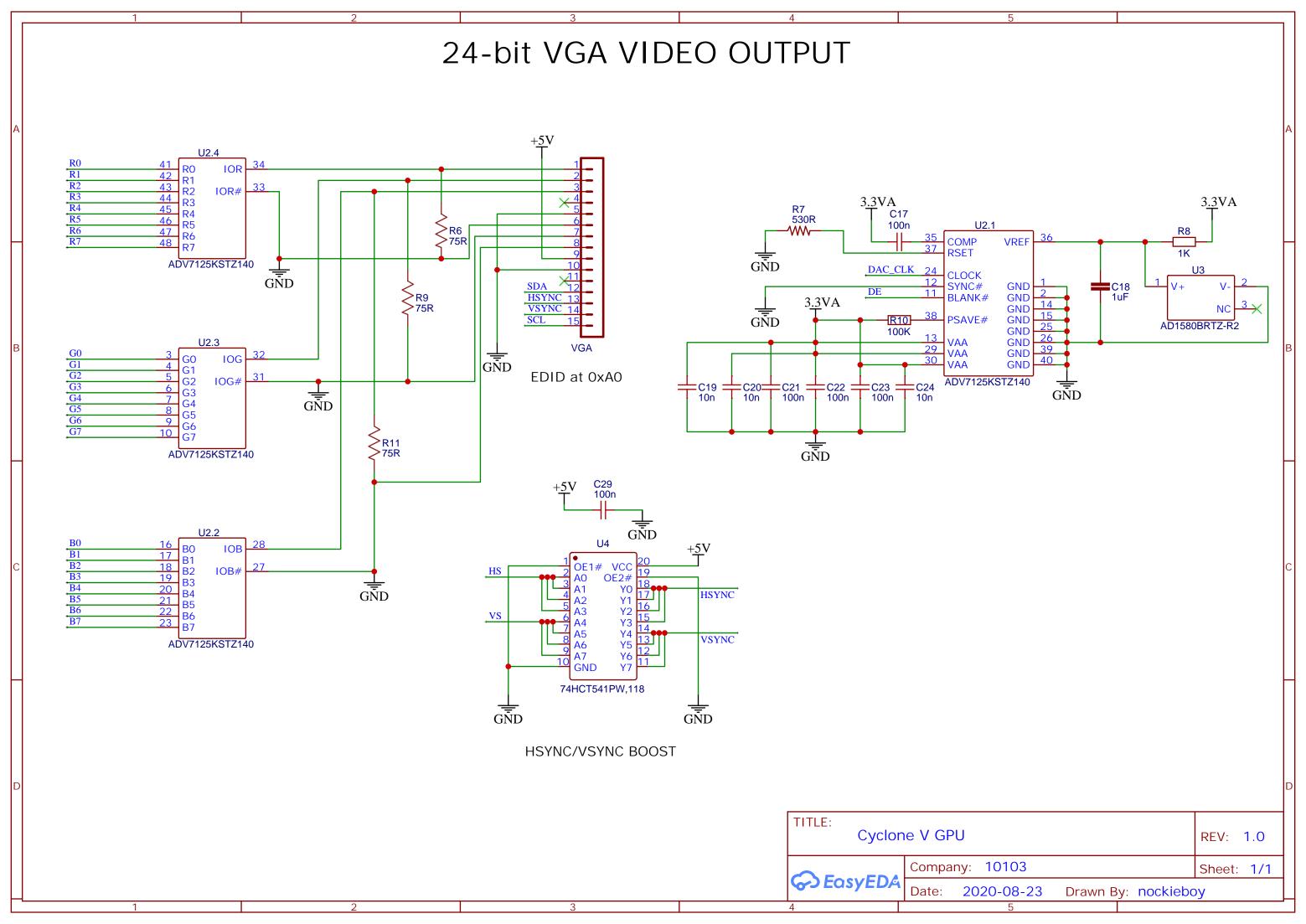
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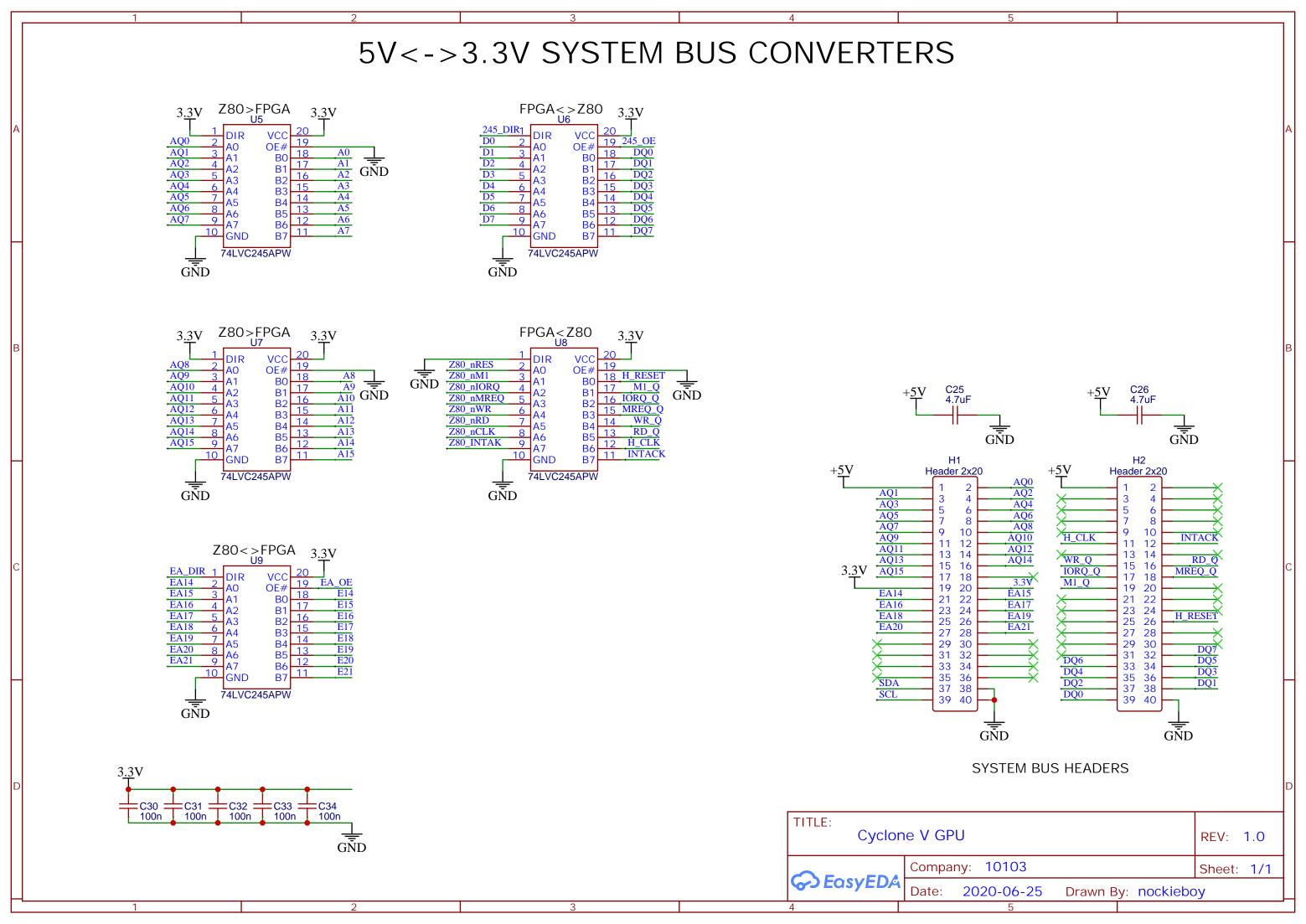
Drawn By: nockieboy

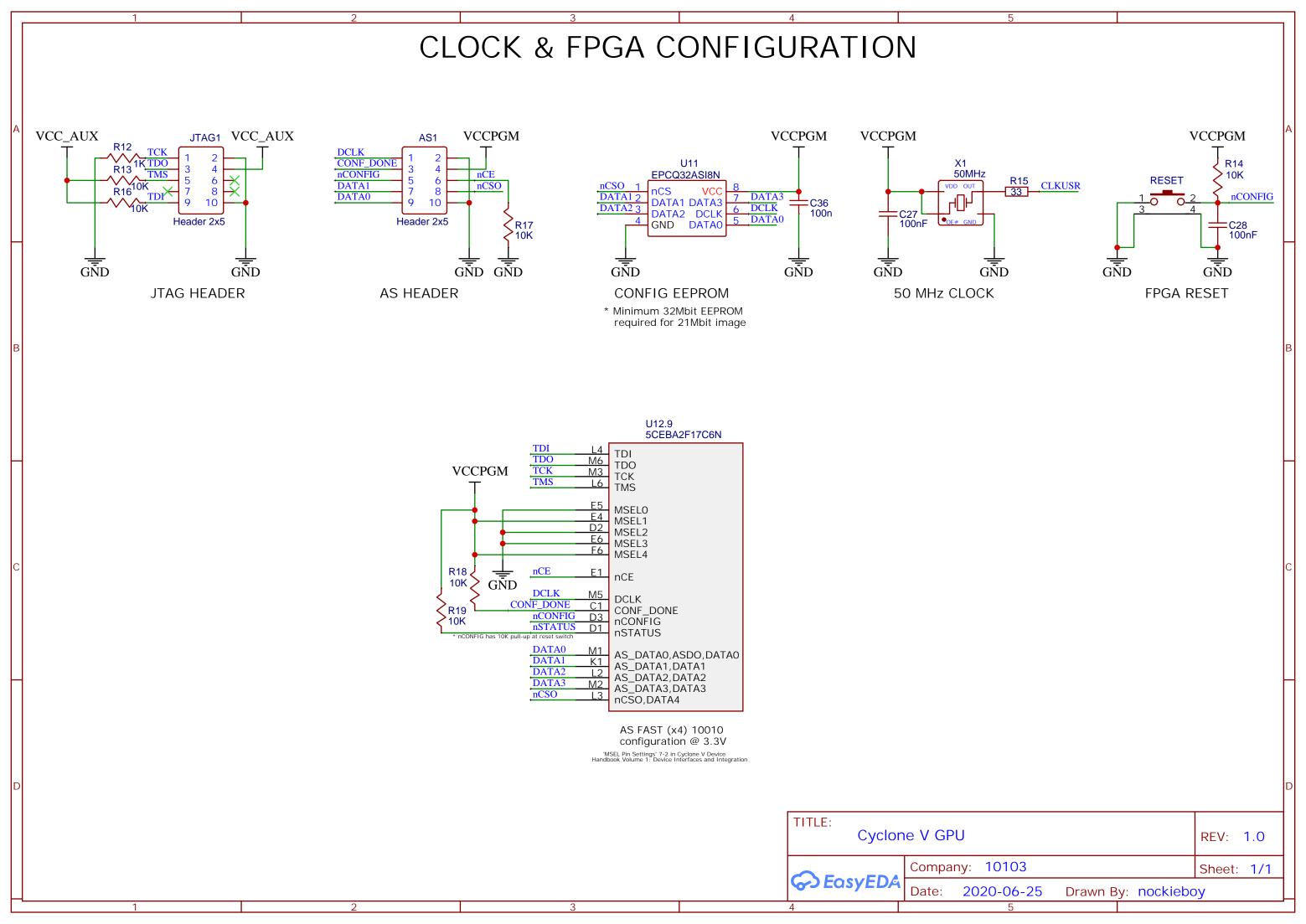
Date: 2020-10-20

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Cyclone V FPGA

NOTE: Cyclone V A2 and A4 versions are pin-compatible and interchangeable on this PCB design.

U12.1

5CEBA2F17C6N	_
IO, (DIFFIO_TX_L9p, DIFFOUT_L9p, DQ1L) IO, (DIFFIO_TX_L9n, DIFFOUT_L9n) IO, (DIFFIO_RX_L10p, DIFFOUT_L10p, DQ1L) IO, (DIFFIO_RX_L10n, DIFFOUT_L11p, DQS1L) IO, (DIFFIO_RX_L11p, DIFFOUT_L11p, DQS1L) IO, (DIFFIO_RX_L11n, DIFFOUT_L11n, DQSn1L) IO, (DIFFIO_TX_L12p, DIFFOUT_L12p) IO, (DIFFIO_TX_L12n, DIFFOUT_L12n, DQ1L) IO, (DIFFIO_TX_L13p, DIFFOUT_L13p, DQ1L) IO, (DIFFIO_TX_L13n, DIFFOUT_L13n, DQ1L) IO, (DIFFIO_RX_L14p, DIFFOUT_L14p, DQ1L) IO, (DIFFIO_RX_L14n, DIFFOUT_L14n, DQ1L) IO, (DIFFIO_RX_L15p, DIFFOUT_L15p) IO, (DIFFIO_RX_L16p, DIFFOUT_L16p, DQ1L) IO, (DIFFIO_TX_L16p, DIFFOUT_L16p, DQ1L) IO, (DIFFIO_TX_L16n, DIFFOUT_L16n, DQ1L)	F4 PC_RTS F3 PC_CTS H3 PC_RXD G3 PC_TXD H5 H4 F2 UART_TX E2 UART_RX G2 G1 A_BCK J3 J2 K5 K4 J1 A_DIN H1 A_LRCK

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SCEBAZE I / CON		
IO DATAO (DIFFIO DV D1» DIFFOUT D1» DO1D)	P4	SD_CMD
IO,DATA8, (DIFFIO_RX_B1p,DIFFOUT_B1p,DQ1B)	N4	SD_D3
IO,DATA6,(DIFFIO_RX_B1n,DIFFOUT_B1n,DQ1B)	P1	SD D1
IO,DATA7,(DIFFIO_TX_B2p,DIFFOUT_B2p,DQ1B)	N1	SD D2
IO,DATA5,(DIFFIO_TX_B2n,DIFFOUT_B2n)	17	IOR
IO,DATA12,(DIFFIO_RX_B3p,DIFFOUT_B3p,DQS1B)	M7	SD CLK
IQDATA10, (DIFFIO_RX_B3n, DIFFOUT_B3n, DQSn1B)	P2	$\frac{BD_{-}CER}{A0}$
IO,DATA11,(DIFFIO_TX_B4p,DIFFOUT_B4p)		SD D0
\neq IO,DATA9,(DIFFIO_TX_B4n,DIFFOUT_B4n,DQ1B)	R1	CLKUSR
JO, CLKUSR, (DIFFIO_RX_B5p, DIFFOUT_B5p, DQ1B)	N3	
PO, DATA14, (DIFFIO_RX_B5n, DIFFOUT_B5n, DQ1B)	<u>P3</u>	A3
IO, DATA15, (DIFFIO_TX_B6p, DIFFOUT_B6p, DQ1B)	R2	<u>A1</u>
IO,DATA13,(DIFFIO_TX_B6n,DIFFOUT_B6n,DQ1B)	T2	A2
IO,PR_ERROR,(DIFFIO_RX_B7p,DIFFOUT_B7p)	P7	A11
IO,PR DONE,(DIFFIO RX B7n,DIFFOUT B7n)	R6	A8
	R4	A5
IO, (DIFFIO_TX_B8p, DIFFOUT_B8p, DQ1B)	T3	A4
IO,PR_READY,(DIFFIO_TX_B8n,DIFFOUT_B8n,DQ1B)		

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IO,(DIFFIO_TX_B17p,DIFFOUT_B17p,DQ2B)	T4 A6
IO,(DIFFIO_TX_B17p,DUZ2b)	<u>T5 A7</u>
IO,(DIFFIO_RX_B18p,DIFFOUT_B18p,DQ2B)	P8 A13
IO,(DIFFIO_RX_B18n,DIFFOUT_B18n,DQ2B)	R7 A10
IO,(DIFFIO_RX_B19p,DIFFOUT_B19p,DQS2B)	L9 IOB
IO,(DIFFIO_RX_B19p,DIFFOUT_B19p,DQSp2B)	M8 IOG
IO,(DIFFIO_TX_B20p,DIFFOUT_B20p)	T8 A12
IO,(DIFFIO_TX_B20p,DIFFOUT_B20p	T7 A9
O,FRLL_BL_CLKOUTO,FPLL_BL_CLKOUTp,FPLL_BL_FB,(DIFFIO_TX_B21p,DIFFOUT_B21p,DQ2B)	R12 E19
IO,FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn,(DIFFIO_TX_B21n,DIFFOUT_B21n,DQ2B)	R11 E14
IO,(PEE_BE_CEROOTT,(PEE_BE_CEROOTT),(DITTIO_TX_B2TI),DITTOOT_B2TI,DQ2B)	T13 E20
IO,(DITTIO_RX_B22P,DITTOUT_B22P,DQ2B)	T12 E18
IO,(BITTO_IX_B22II,BITTOUT_B22II,BQ2B)	P9 A15
IO,CLK1p,(DIFFIO_RX_B23p,DIFFOUT_B23p)	R9 A14
IO,(DIFFIO_TX_B24p,DIFFOUT_B24p,DQ2B)	R10 EA_OE
IO.(DIFFIO TX_B24p,DIFFOUT_B24p,DQ2B)	T10 EA_DIR

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IO,(DIFFIO_TX_B25p,DIFFOUT_B25p,DQ3B)	P16	HS
IO,RZQ_0,(DIFFIO_TX_B25n,DIFFOUT_B25n)	R15	PS2_KCLK
IO,(DIFFIO_RX_B26p,DIFFOUT_B26p,DQ3B)	R16	DE
IO,(DIFFIO_RX_B26n,DIFFOUT_B26n,DQ3B)	T15	PS2_MDAT
IO,(DIFFIO_RX_B27p,DIFFOUT_B27p,DQS3B)	L10	
LO,(DIFFIO_RX_B27p,DIFFOUT_B27p,DQSn3B)	M10	
≥ IO,(DIFFIO_TX_B28p,DIFFOUT_B28p)	N14	
IO,(DIFFIO_TX_B28n,DIFFOUT_B28n,DQ3B)	M13	
4 IO,(DIFFIO_TX_B29p,DIFFOUT_B29p,DQ3B)	P13	E21
IO,(DIFFIO_TX_B29n,DIFFOUT_B29n,DQ3B)	P14	VS
IO,(DIFFIO RX B30p,DIFFOUT B30p,DQ3B)	M11	E17
IO,(DIFFIO_RX_B30n,DIFFOUT_B30n,DQ3B)	M12	
IO,CLK2p,(DIFFIO_RX_B31p,DIFFOUT_B31p)	N11	E16
IO,CLK2p,(DIFFIO_RX_B31p,DIFFOUT_B31p)	P11	E15
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B)	R14	PS2_KDAT
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B)	T14	PS2_MCLK
10,(011110_17_03211,0111001_03211,0030)		

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SCEBAZE I / CON		
10 D70 1 (DIFFIO TV D1 - DIFFOUT D1 - D01D)	N15	B1
IO,PR_REQUEST,(DIFFIO_IX_RIN,DIFFOOT_RIN,DQTR) - IO,INIT_DONE,(DIFFIO_RX_R2p,DIFFOUT_R2p) -	N16	B0
	L13	B4
	K14	B6
IO,CRC_ERROR,(DIFFIO_RX_R2n,DIFFOUT_R2n)	H16	G3
IO,nCEO,(DIFFIO_TX_R3p,DIFFOUT_R3p,DQ1R)		G0
mIO,CvP_CONFDONE,(DIFFIO_TX_R3n,DIFFOUT_R3n,DQ1R)	<u>J16</u>	B3
IO, (DIFFIO_RX_R4p, DIFFOUT_R4p, DQ1R) IO, (DIFFIO_RX_R4n, DIFFOUT_R4n, DQ1R)	L14	
IO,(DIFFIO_RX_R4n,DIFFOUT_R4n,DQ1R)	L15	B2
IO,DEV_OE,(DIFFIO_TX_R5p,DIFFOUT_R5p)	G15	G7
IO,DEV_CLRn,(DIFFIO_TX_R5n,DIFFOUT_R5n,DQ1R) IO,(DIFFIO_RX_R6p,DIFFOUT_R6p,DQS1R)	G16	G6
	K12	B7
	J12	G2
IO, (DIFFIO_RX_R6n, DIFFOUT_R6n, DQSn1R)	J14	G1
IO, (DIFFIO_TX_R7p, DIFFOUT_R7p, DQ1R)	H15	G 4
IO,(DIFFIO_TX_R7n,DIFFOUT_R7n)	K15	DAC CLK
IO,(DIFFIO_RX_R8p,DIFFOUT_R8p,DQ1R)	K16	B5
IO,(DIFFIO_RX_R8n,DIFFOUT_R8n,DQ1R)	K I O	<u></u>
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U12.12 5CEBA2F17C6N A2 DNU DNU DNU DNU RREF_TL R53 2K

U12.6

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5CEBA2F17C6N	_	
IO,CLK6p,(DIFFIO_RX_R9p,DIFFOUT_R9p) IO,CLK6n,(DIFFIO_RX_R9n,DIFFOUT_R9n) IO,(DIFFIO_TX_R10p,DIFFOUT_R10p,DQ2R) IO,(DIFFIO_TX_R11p,DIFFOUT_R10n,DQ2R) IO,(DIFFIO_RX_R11p,DIFFOUT_R11p,DQ2R) IO,(DIFFIO_RX_R11n,DIFFOUT_R11p,DQ2R) O,FPPL_BR_CLKOUTO,FPLL_BR_CLKOUTp,FPLL_BR_FB,(DIFFIO_TX_R12p,DIFFOUT_R12p,DQ2R) IO,FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn,(DIFFIO_TX_R12p,DIFFOUT_R12n,DQ2R) IO,(DIFFIO_RX_R13p,DIFFOUT_R13p,DQS2R) IO,(DIFFIO_RX_R13n,DIFFOUT_R13n,DQSn2R) IO,(DIFFIO_TX_R14p,DIFFOUT_R14p) IO,(DIFFIO_TX_R14p,DIFFOUT_R14p) IO,(DIFFIO_TX_R14n,DIFFOUT_R15p,DQ2R) IO,(DIFFIO_RX_R15p,DIFFOUT_R15n,DQ2R) IO,(DIFFIO_RX_R15n,DIFFOUT_R16p,DQ2R) IO,(DIFFIO_TX_R16p,DIFFOUT_R16p,DQ2R) IO,(DIFFIO_TX_R16p,DIFFOUT_R16p,DQ2R) IO,(DIFFIO_TX_R16p,DIFFOUT_R16p,DQ2R)	F12 G12 E16 D16 E12 D13 B16 C16 H13 G13 B15 C15 F14 F15 D14 E15	D4 R0 R5 R7 D5 Z80_nRES Z80_INTAK Z80_nCLK G5 R1 Z80_nWR Z80_nMREQ R2 R3 R6 R4

U12.7

U12.8

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IO,CLK9p,(DIFFIO_RX_I25p,DIFFOUT_I25p) IO,CLK9n,(DIFFIO_RX_T25n,DIFFOUT_T25n) IO,(DIFFIO_TX_T26p,DIFFOUT_T26p,DQ2T) IO,(DIFFIO_TX_T26n,DIFFOUT_T26n,DQ2T) IO,(DIFFIO_RX_T27p,DIFFOUT_T27p,DQ2T) IO,(DIFFIO_RX_T27n,DIFFOUT_T27n,DQ2T) PLL_TL_CLKOUTp,FPLL_TL_FB,(DIFFIO_TX_T28p,DIFFOUT_T28p,DQ2T) CLKOUT1,FPLL_TL_CLKOUTn,(DIFFIO_TX_T28n,DIFFOUT_T28n,DQ2T) IO,(DIFFIO_RX_T29p,DIFFOUT_T29p,DQS2T) IO,(DIFFIO_RX_T29p,DIFFOUT_T29p,DQS2T) IO,(DIFFIO_RX_T29n,DIFFOUT_T30p,DIFFOUT_T30p) IO,(DIFFIO_TX_T30n,DIFFOUT_T30n,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31n,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31n,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31n,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T) IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T)	F8 F7 A8 A9 B8 A7 A5 A4 D8 D7 B3 A3 B7 B6 C3	DDR_D6 DDR_D7 DDR_D5 DDR_D3 DDR_CKp DDR_CKn DDR_D1 DDR_RST DDR2_CSn DDR_D2 DDR_D0 DDR1_CSn DDR_D4

TITLE:

Cyclone V GPU

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