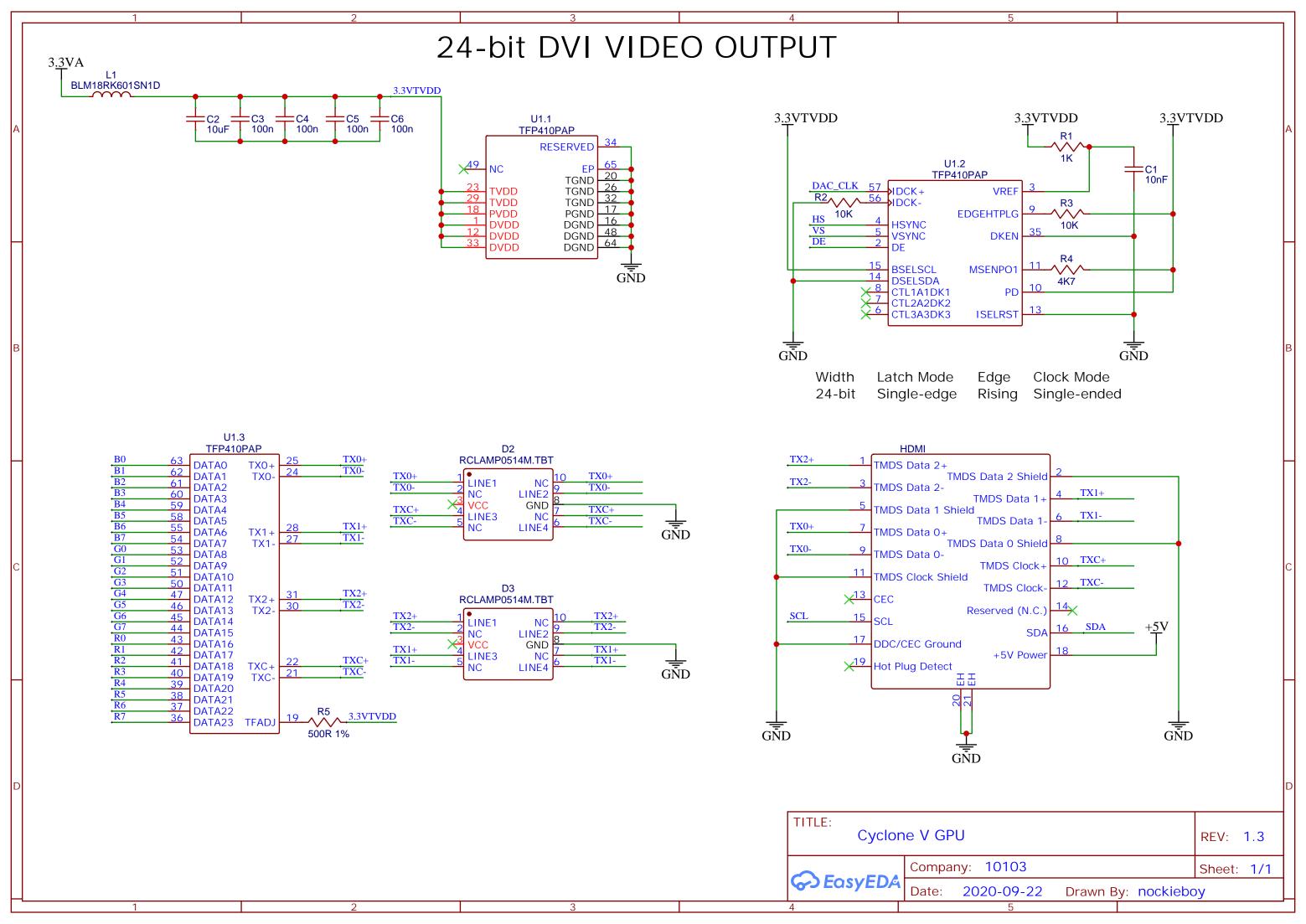
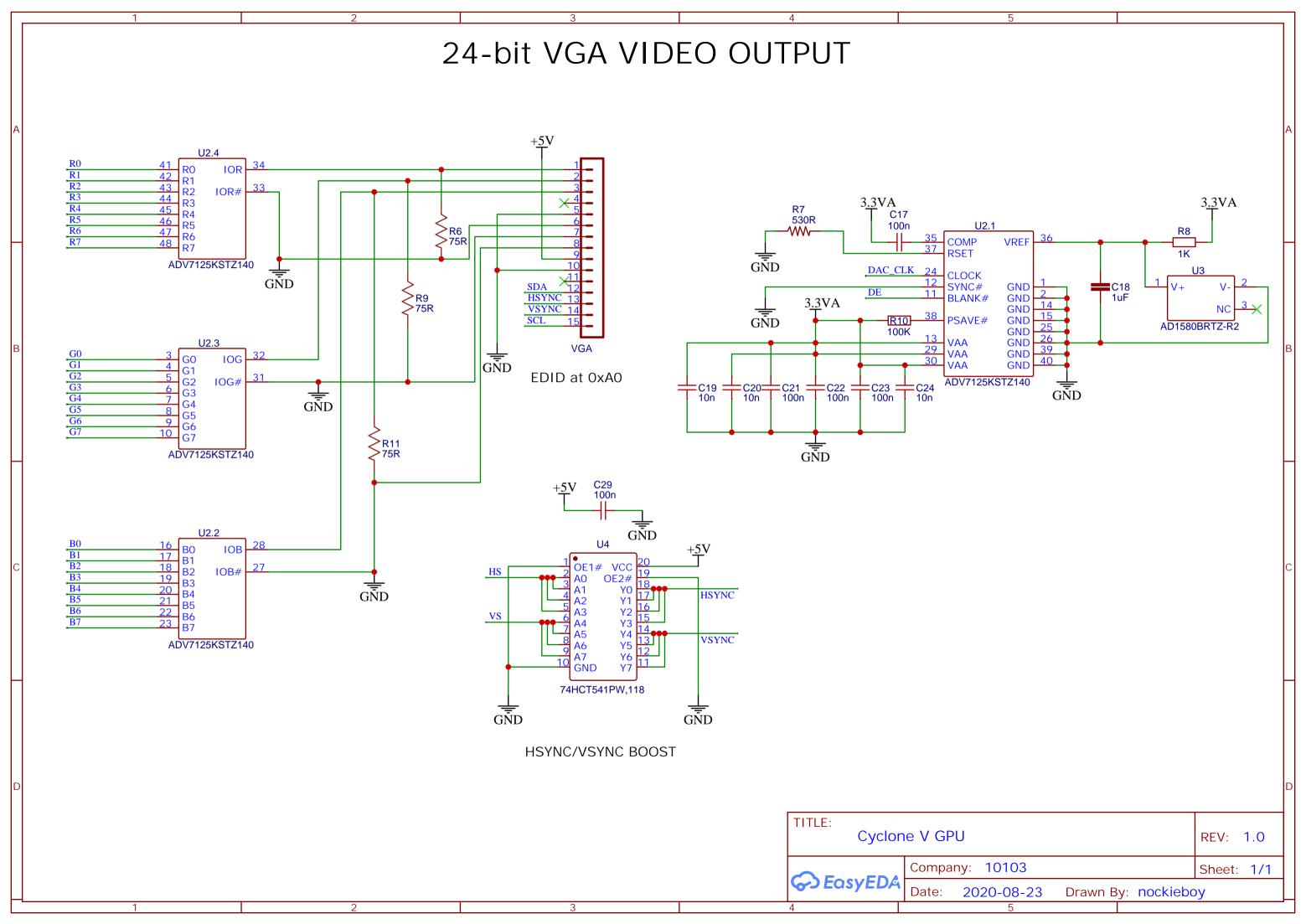
CYCLONE V GPU SCHEMATICS

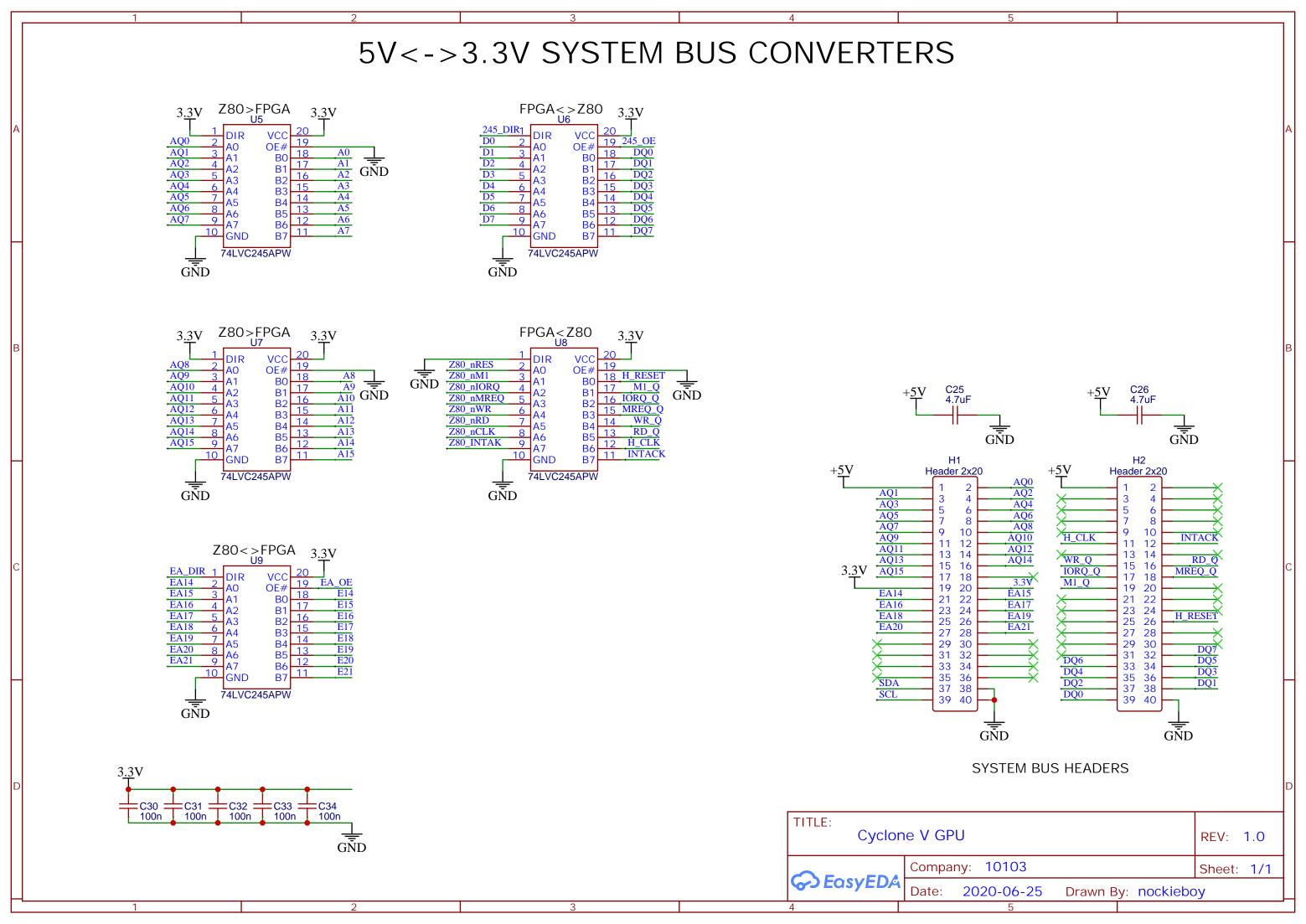
REVISIONS
1.0 - Initial draft
1.1 - Replaced MAX5101 DAC with PCM5101A. Replaced wire-wound chokes with fixed inductors.
1.2 - Added decoupling and supply isolation for TFP410.
1.3 - Removed decoupling and supply isolation for TFP410. Added external memory.

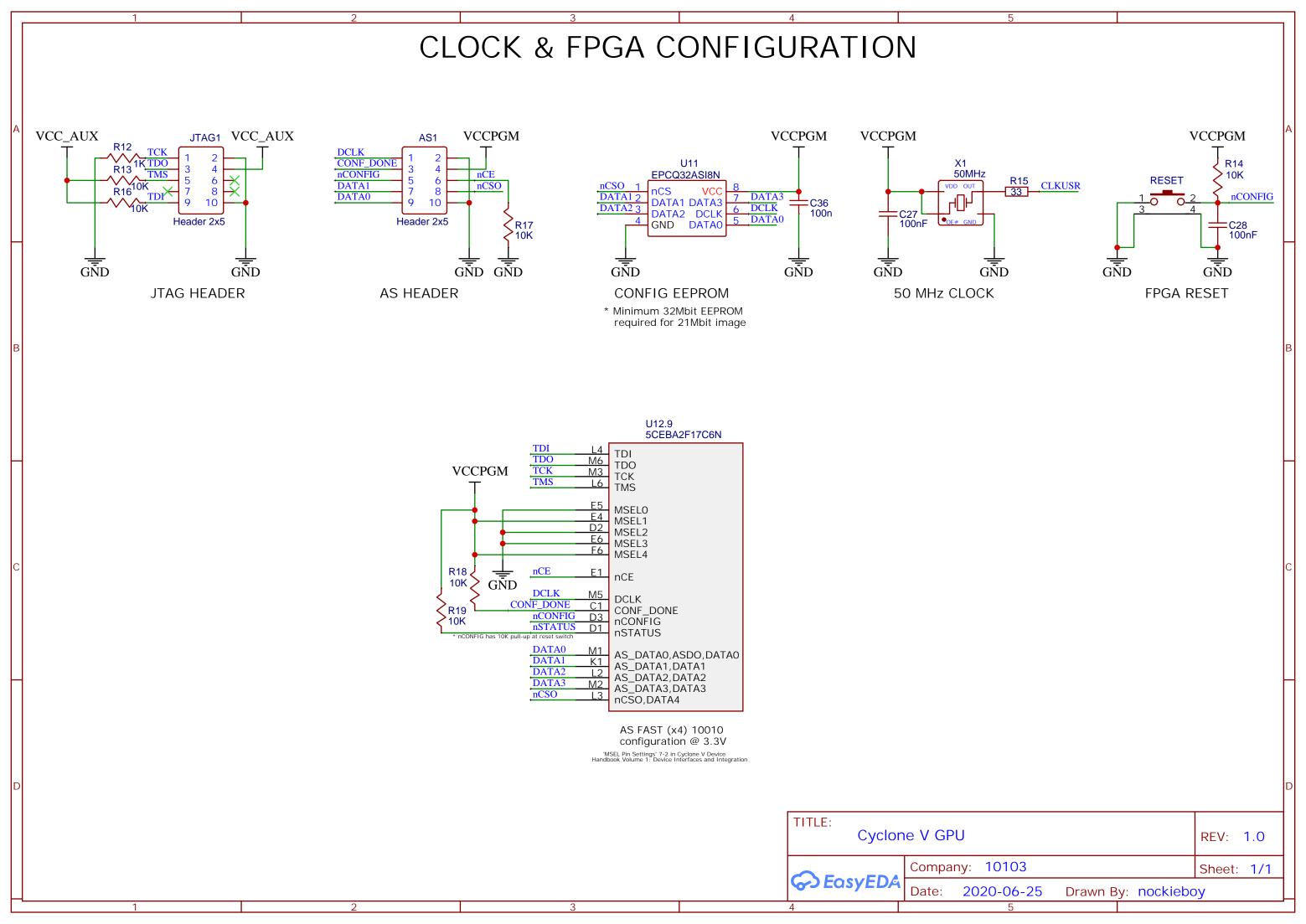
PAGE	CONTENT
1.	INDEX
2.	DVI OUTPUT
3.	VGA OUTPUT
4.	5V TO 3.3V BUS CONVERSION
5.	CLOCK & FPGA CONFIGURATION
6.	FPGA CONNECTIONS
7.	GPU BOARD PERIPHERALS
8.	POWER SUPPLIES
9.	DECOUPLING
10.	FPGA EXTERNAL MEMORY

TITLE: Cyclone V GPU					REV:	1.3
O = ===	Compa	ny: 10103			Sheet:	1/1
EasyEDA	Date:	2020-10-20	Drawn By	ı: nockiebo	ру	
1		5				









Cyclone V FPGA NOTE: Cyclone V A2 and A4 versions are pin-compatible and interchangeable on this PCB design. U12.5 U12.1 5CEBA2F17C6N U12.12 5CEBA2F17C6N 5CEBA2F17C6N IO,RZQ_1,(DIFFIO_TX_R1p,DIFFOUT_R1p,DQ1R) IO,(DIFFIO_TX_L9p,DIFFOUT_L9p,DQ1L)
IO,(DIFFIO_TX_L9n,DIFFOUT_L9n) IO,PR_REQUEST,(DIFFIO_TX_R1n,DIFFOUT_R1n,DQ1R) DNU DNU IO, INIT_DONE, (DIFFIO_RX_R2p, DIFFOUT_R2p) L13 DNU DNU IO,(DIFFIO_RX_L10p,DIFFOUT_L10p,DQ1L)
IO,(DIFFIO_RX_L10n,DIFFOUT_L10n,DQ1L) IO,CRC_ERROR,(DIFFIO_RX_R2n,DIFFOUT_R2n) G3 IO,nCEO,(DIFFIO_TX_R3p,DIFFOUT_R3p,DQ1R) RREF_TL IO, (DIFFIO_RX_R4p, DIFFOUT_R4p, DQ1R) IO, (DIFFIO_TX_L12p, DIFFOUT_L12p, DIFFOUT_L12p)
IO, (DIFFIO_TX_L12p, DIFFOUT_L12p, DQ1L)
IO, (DIFFIO_TX_L13p, DIFFOUT_L13p, DQ1L)
IO, (DIFFIO_TX_L13n, DIFFOUT_L13n, DQ1L)
IO, (DIFFIO_TX_L13n, DIFFOUT_L13n, DQ1L)
IO, (DIFFIO_RX_L14p_DIFFOUT_L14p_DQ1L)
IO, (DIFFIO_RX_L14p_DIFFOUT_L14p_DQ1L)
IO IO, (DIFFIO_RX_R4n, DIFFOUT_R4n, DQ1R) IO,DEV_OE,(DIFFIO_TX_R5p,DIFFOUT_R5p)
IO,DEV_CLRn,(DIFFIO_TX_R5n,DIFFOUT_R5n,DQ1R) IO, (DIFFIO_RX_R6p, DIFFOUT_R6p, DQS1R) GND IO,(DIFFIO_RX_L14p,DIFFOUT_L14p,DQ1L)
IO,(DIFFIO_RX_L14n,DIFFOUT_L14n,DQ1L) IO, (DIFFIO_RX_R6n, DIFFOUT_R6n, DQSn1R)
IO, (DIFFIO_TX_R7p, DIFFOUT_R7p, DQ1R) IO, (DIFFIO_RX_L14II, DIFFOUT_L14N, DQ1L)

IO, (DIFFIO_RX_L15p, DIFFOUT_L15p)

IO, (DIFFIO_RX_L15n, DIFFOUT_L15n)

IO, (DIFFIO_TX_L16p, DIFFOUT_L16p, DQ1L)

IO, (DIFFIO_TX_L16n, DIFFOUT_L16n, DQ1L) IO,(DIFFIO_TX_R7n,DIFFOUT_R7n) H15 IO,(DIFFIO_RX_R8p,DIFFOUT_R8p,DQ1R)
IO,(DIFFIO_RX_R8n,DIFFOUT_R8n,DQ1R)

K15 DAC_CLK
K16 B5 U12.2 U12.6 5CEBA2F17C6N IO, DATA8, (DIFFIO_RX_B1p, DIFFOUT_B1p, DQ1B) IO,CLK6p,(DIFFIO_RX_R9p,DIFFOUT_R9p) < IO,CLK6n,(DIFFIO_RX_R9n,DIFFOUT_R9n) IO,DATA6,(DIFFIO_RX_B1n,DIFFOUT_B1n,DQ1B) IO, (DIFFIO_TX_R10p, DIFFOUT_R10p, DQ2R) IO, DATA7, (DIFFIO_TX_B2p, DIFFOUT_B2p, DQ1B) \overline{SD} D2 IO, DATA5, (DIFFIO_TX_B2n, DIFFOUT_B2n) IO, (DIFFIO_TX_R10n, DIFFOUT_R10n, DQ2R) IO,DATA12,(DIFFIO_RX_B3p,DIFFOUT_B3p,DQS1B) IO, (DIFFIO_RX_R11p, DIFFOUT_R11p, DQ2R) SD_CLK Z80_nRES IQDATA10, (DIFFIO_RX_B3n, DIFFOUT_B3n, DQSn1B) IO, (DIFFIO_RX_R11n, DIFFOUT_R11n, DQ2R) IO, FPE_BR_CLKOUTO, FPLL_BR_CLKOUTD, FPLL_BR_FB, (DIFFIO_TX_R12p, DIFFOUT_R12p, DQ2R) IO, DATA11, (DIFFIO_TX_B4p, DIFFOUT_B4p) SD_D0 C16 Z80_nCLK IO,FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn,(DIFFIO_TX_R12n,DIFFOUT_R12n,DQ2R) ₹ IO,DATA9,(DIFFIO_TX_B4n,DIFFOUT_B4n,DQ1B) JO,CLKUSR,(DIFFIO_RX_B5p,DIFFOUT_B5p,DQ1B) 🗲 IO, (DIFFIO_RX_R13p, DIFFOUT_R13p, DQS2R) A3 A1 O,DATA14,(DIFFIO_RX_B5n,DIFFOUT_B5n,DQ1B) IO, (DIFFIO_RX_R13n, DIFFOUT_R13n, DQSn2R) B15 Z80_nWR IO,DATA15,(DIFFIO_TX_B6p,DIFFOUT_B6p,DQ1B) IO, (DIFFIO_TX_R14p, DIFFOUT_R14p) A2 A11 IO, (DIFFIO_TX_R14n, DIFFOUT_R14n, DQ2R) IO, DATA13, (DIFFIO_TX_B6n, DIFFOUT_B6n, DQ1B) IO,PR_ERROR,(DIFFIO_RX_B7p,DIFFOUT_B7p) IO, (DIFFIO_RX_R15p, DIFFOUT_R15p, DQ2R) A8 R3 IO,PR_DONE, (DIFFIO_RX_B7n, DIFFOUT_B7n) IO, (DIFFIO_RX_R15n, DIFFOUT_R15n, DQ2R) IO, (DIFFIO_TX_R16p, DIFFOUT_R16p, DQ2R)
IO, (DIFFIO_TX_R16n, DIFFOUT_R16n) IO,(DIFFIO_TX_B8p,DIFFOUT_B8p,DQ1B)
IO,PR_READY,(DIFFIO_TX_B8n,DIFFOUT_B8n,DQ1B) U12.7 U12.3 IO,CLK10p,(DIFFIO_RX_T17p,DIFFOUT_T17p) F10 IO,CLK10n,(DIFFIO_RX_T17n,DIFFOUT_T17n) IO, (DIFFIO_TX_B17p, DIFFOUT_B17p, DQ2B) IO, (DIFFIO_TX_B17n, DIFFOUT_B17n) IO, (DIFFIO_TX_T18p, DIFFOUT_T18p, DQ1T) IO,(DIFFIO_RX_B18p,DIFFOUT_B18p,DQ2B) IO, (DIFFIO_TX_T18n,DIFFOUT_T18n,DQ1T) A14 Z80_nIORQ IO, (DIFFIO_RX_B18n, DIFFOUT_B18n, DQ2B) IO, (DIFFIO_RX_T19p, DIFFOUT_T19p, DQ1T) IO,(DIFFIO_RX_B19p,DIFFOUT_B19p,DQS2B)
IO,(DIFFIO_RX_B19n,DIFFOUT_B19n,DQSn2B) IOG IO, (DIFFIO_RX_T19n, DIFFOUT_T19n, DQ1T) IO,(DIFFIO_TX_T20p,DIFFOUT_T20p,DQ1T)
IO,(DIFFIO_TX_T20n,DIFFOUT_T20n,DQ1T) IO, (DIFFIO_TX_B20p, DIFFOUT_B20p) IO,(DIFFIO_TX_B20n,DIFFOUT_B20n,DQ2B)
O,FRUL_BL_CLKOUTO,FPLL_BL_CLKOUTp,FPLL_BL_FB,(DIFFIO_TX_B21p,DIFFOUT_B21p,DQ2B) IO, (DIFFIO_RX_T21p, DIFFOUT_T21p, DQS1T) PO,(DIFFIO_RX_T21n,DIFFOUT_T21n,DQSn1T)
IO,(DIFFIO_TX_T22p,DIFFOUT_T22p) IO,FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn, (DIFFIO_TX_B21n, DIFFOUT_B21n, DQ2B) IO,(DIFFIO_RX_B22p,DIFFOUT_B22p,DQ2B)
IO,(DIFFIO_RX_B22n,DIFFOUT_B22n,DQ2B) IO, (DIFFIO_TX_T22n, DIFFOUT_T22n, DQ1T) IO,(DIFFIO_RX_T23p,DIFFOUT_T23p,DQ1T) IO,CLK1p,(DIFFIO_RX_B23p,DIFFOUT_B23p) IO, (DIFFIO_RX_T23n, DIFFOUT_T23n, DQ1T) IO,CLK1n,(DIFFIO_RX_B23p,DIFFOUT_B23p) R9
IO,(DIFFIO_TX_B24p,DIFFOUT_B24p,DQ2B) R10
IO,(DIFFIO_TX_B24n,DIFFOUT_B24n,DQ2B) T10 IO, (DIFFIO_TX_T24p, DIFFOUT_T24p, DQ1T) IO,RZQ_2,(DIFFIO_TX_T24n,DIFFOUT_T24n) U12.8 U12.4 5CEBA2F17C6N 5CEBA2F17C6N IO,CLK9p,(DIFFIO_RX_T25p,DIFFOUT_T25p) F8
IO,CLK9n,(DIFFIO_RX_T25n,DIFFOUT_T25n) A8
IO,(DIFFIO_TX_T26p,DIFFOUT_T26p,DQ2T)
IO,(DIFFIO_TX_T26n,DIFFOUT_T26p,DQ2T)
B8 IO,RZQ_0,(DIFFIO_TX_B25n,DIFFOUT_B25n)
IO,(DIFFIO_RX_B26p,DIFFOUT_B26p,DQ3B) IO, (DIFFIO_RX_T27p, DIFFOUT_T27p, DQ2T) IO, (DIFFIO_RX_B26n, DIFFOUT_B26n, DQ3B) IO,(DIFFIO_RX_B27p,DIFFOUT_B27p,DQS3B) L10 LO,(DIFFIO_RX_B27n,DIFFOUT_B27n,DQSn3B) N14 IO,(DIFFIO_RX_T27n,DIFFOUT_T27n,DQ2T)
IO,FPLL_TL_CLKOUTO,FPLL_TL_CLKOUTp,FPLL_TL_FB,(DIFFIO_TX_T28p,DIFFOUT_T28p,DQ2T) IO, (DIFFIO_TX_B28p, DIFFOUT_B28p)

M14

M13 IO,FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn,(DIFFIO_TX_T28n,DIFFOUT_T28n,DQ2T) IO,(DIFFIO_RX_T29p,DIFFOUT_T29p,DQS2T)
IO,(DIFFIO_RX_T29n,DIFFOUT_T29n,DQSn2T) IO, (DIFFIO_TX_B28n, DIFFOUT_B28n, DQ3B) P13
IO, (DIFFIO_TX_B29p, DIFFOUT_B29p, DQ3B) 10,(DIFFIO_TX_B29n,DIFFOUT_B29n,DO3B) P14
10,(DIFFIO_TX_B29n,DIFFOUT_B29n,DO3B) M11 IO,(DIFFIO_TX_T30p,DIFFOUT_T30p) IO, (DIFFIO_RX_B30p, DIFFOUT_B30p, DQ3B) 10,(DIFFIO_1X_130n,DIFFOU1_130n,DQ21) IO, (DIFFIO_RX_B30n,DIFFOUT_B30n,DQ3B) M12 IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T)

B7 IO,(DIFFIO_RX_B30N,DIFFOUT_B30N,DQ3B)
IO,CLK2p,(DIFFIO_RX_B31p,DIFFOUT_B31p)
IO,CLK2n,(DIFFIO_RX_B31n,DIFFOUT_B31n)
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B)
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B)
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B) IO, (DIFFIO_RX_T31n, DIFFOUT_T31n, DQ2T) IO, (DIFFIO_TX_T32p, DIFFOUT_T32p, DQ2T)
IO, (DIFFIO_TX_T32n, DIFFOUT_T32n)

C3 DDR1_CSr
C4 DDR_CKn IO, (DIFFIO_TX_B32n, DIFFOUT_B32n, DQ3B) TITLE: Cyclone V GPU **REV:** 1.0 Company: 10103 Sheet: 1/1 GD EasyEDA 2020-06-19 Date: Drawn By: nockieboy

