CYCLONE V GPU SCHEMATICS

REVISIONS
1.0 - Initial draft
1.1 - Replaced MAX5101 DAC with PCM5101A. Replaced wire-wound chokes with fixed inductors.

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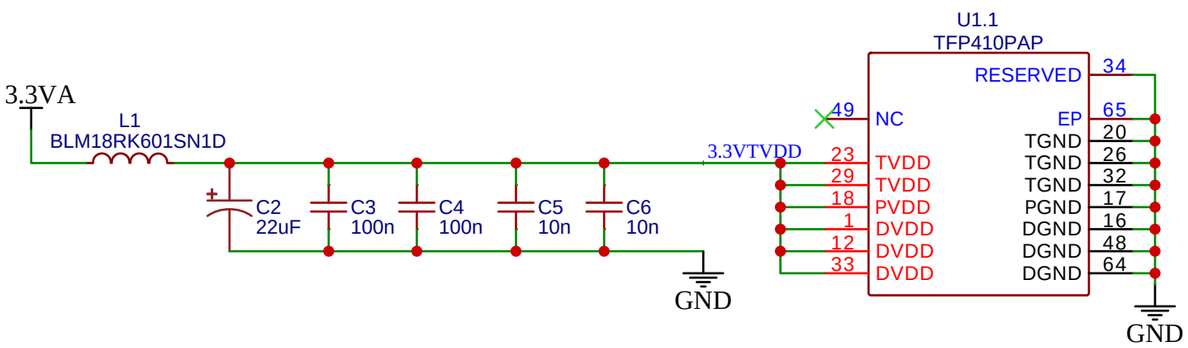
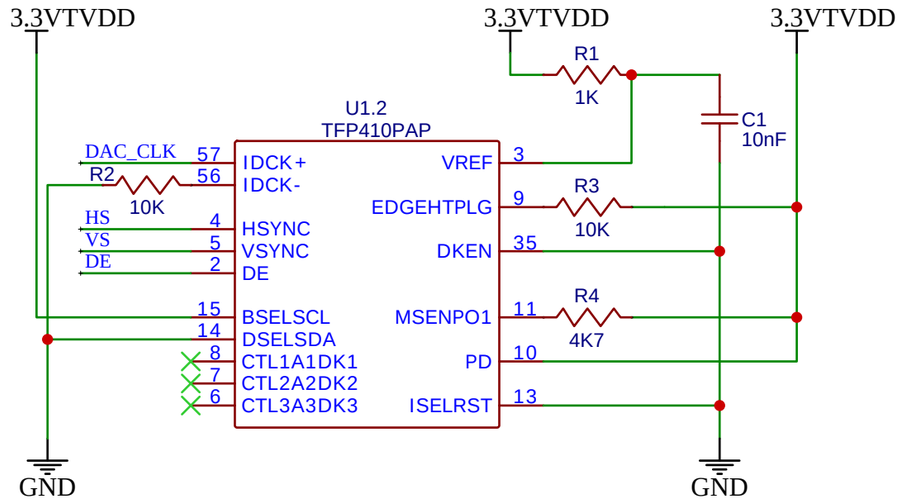
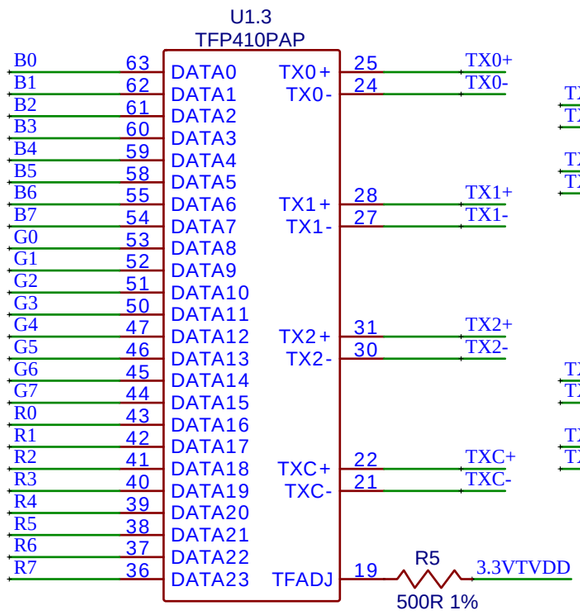
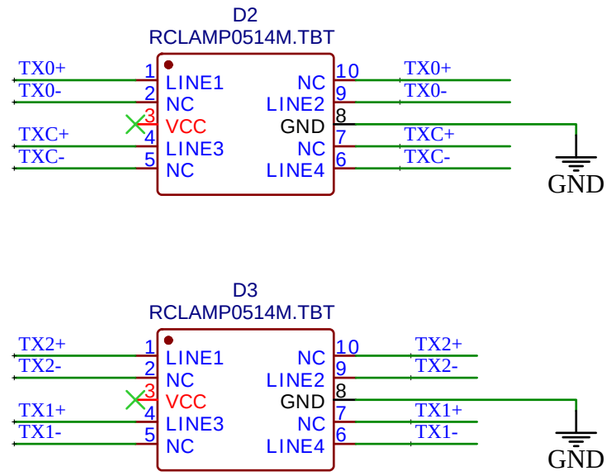
TITLE: Cyclone V GPU		REV: 1.0
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-10-20 Drawn By: nockieboy	

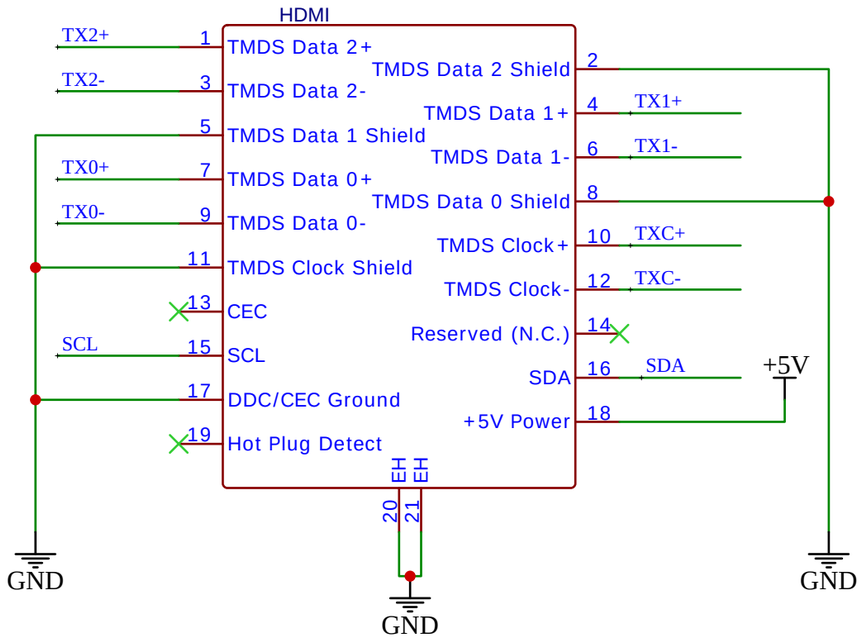
24-bit DVI VIDEO OUTPUT





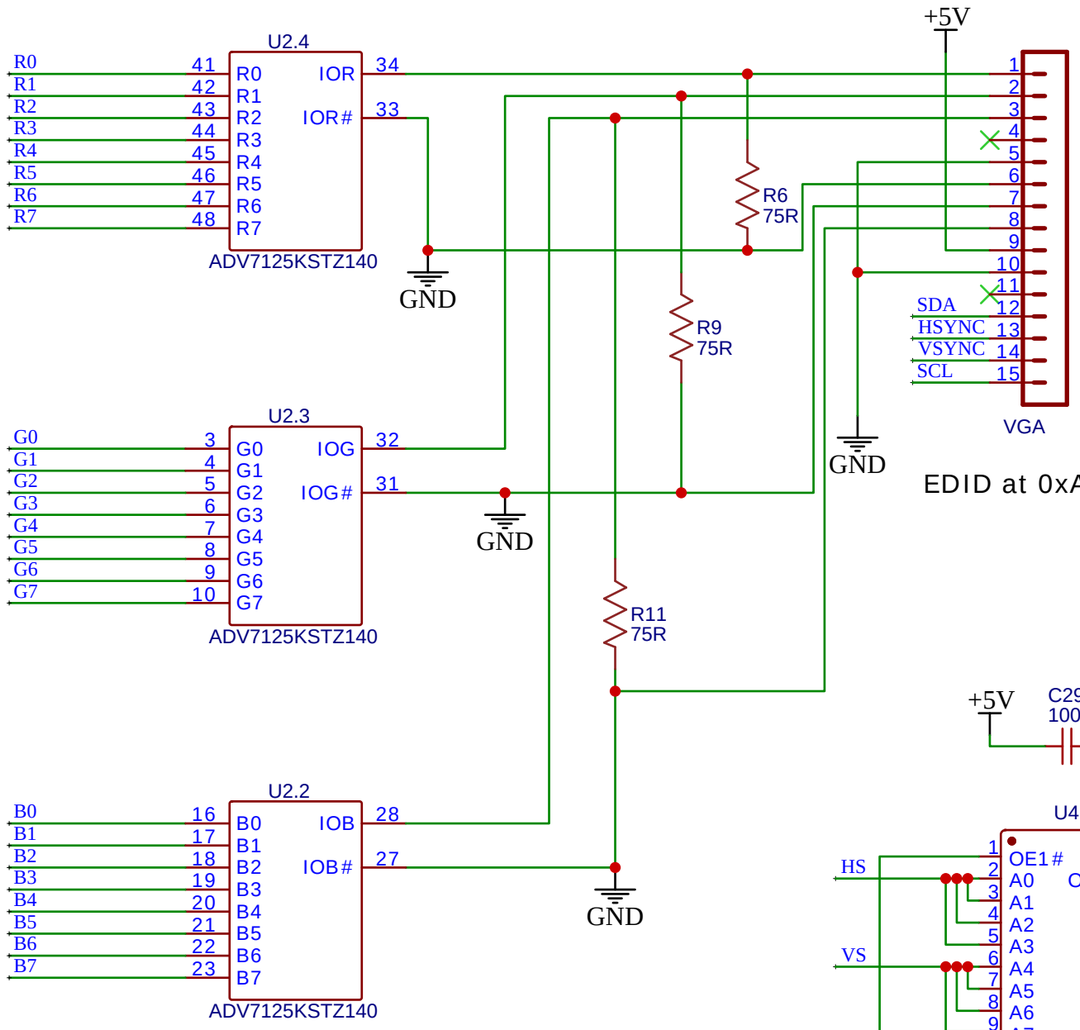


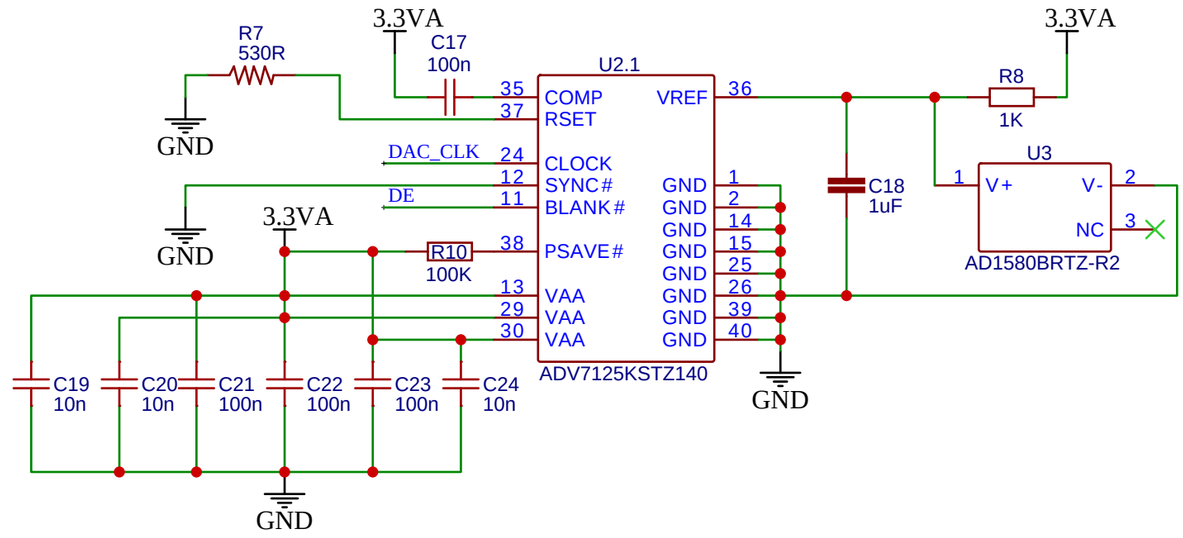


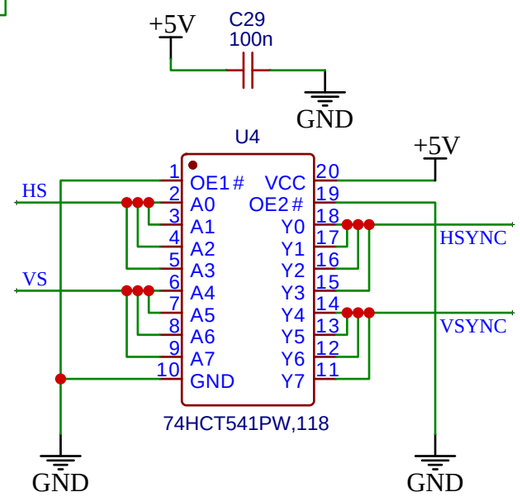


TITLE: Cyclone V GPU		REV: 1.0
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-09-22 Drawn By: nockieboy	

24-bit VGA VIDEO OUTPUT



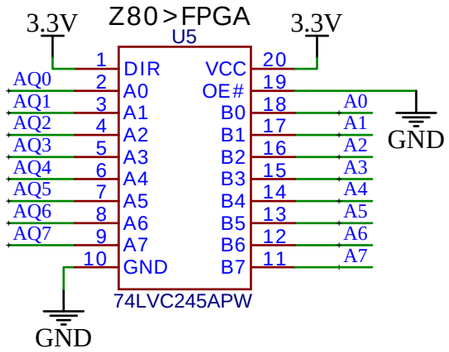


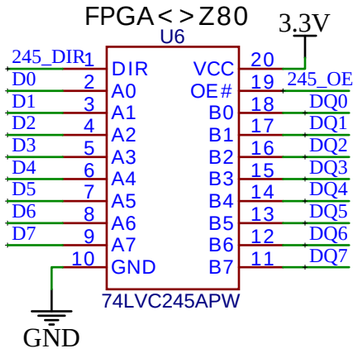


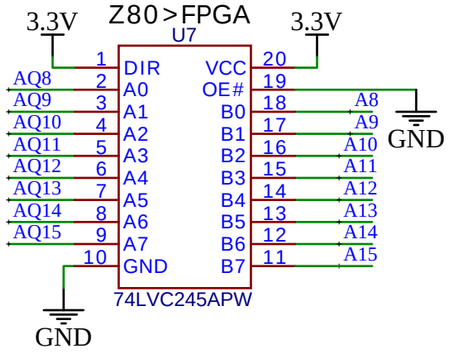
HSYNC/VSYNC BOOST

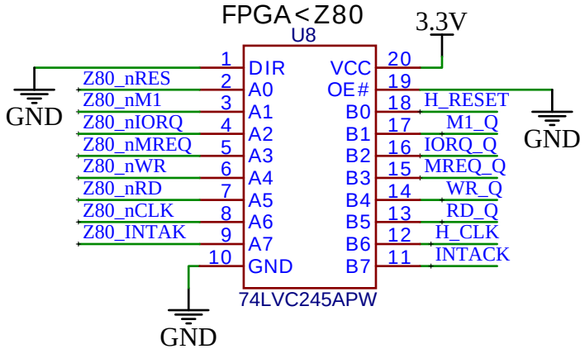
TITLE: Cyclone V GPU		REV: 1.0
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-08-23 Drawn By: nockieboy	

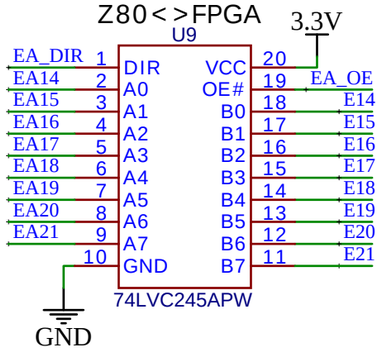
5V<->3.3V SYSTEM BUS CONVERTERS

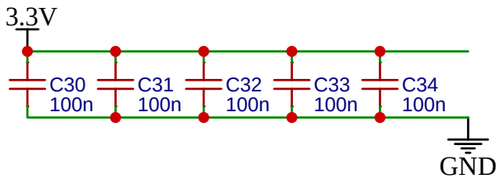


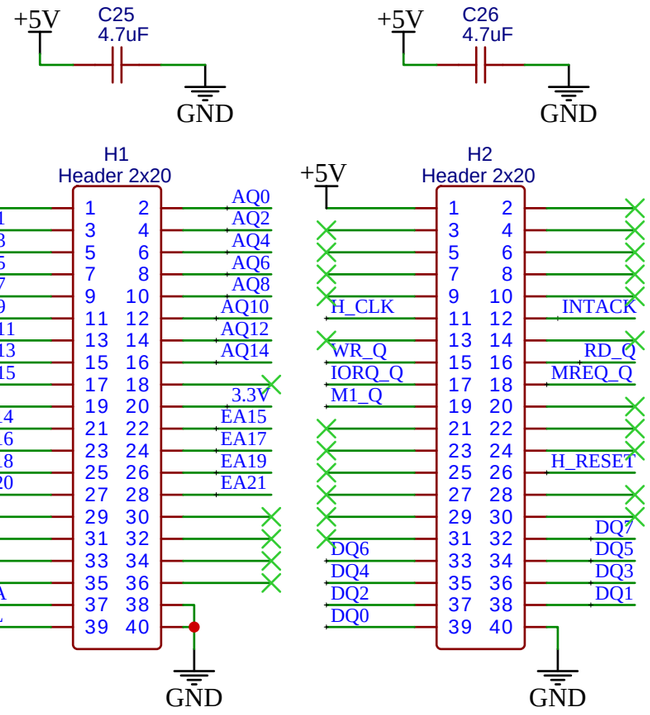












SYSTEM BUS HEADERS

TITLE: Cyclone V GPU		REV: 1.0
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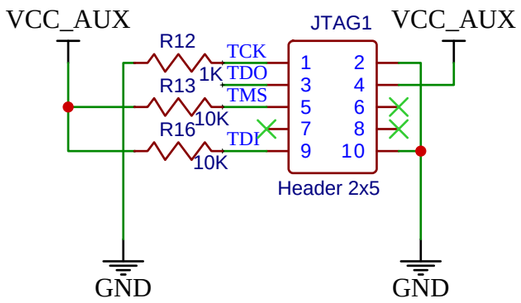
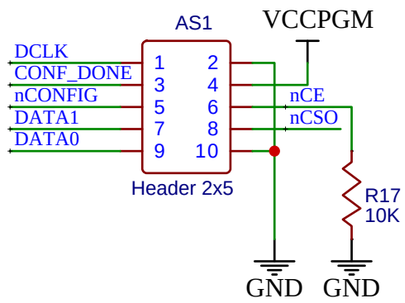
	Date: 2020-06-25 Drawn By: nockieboy	

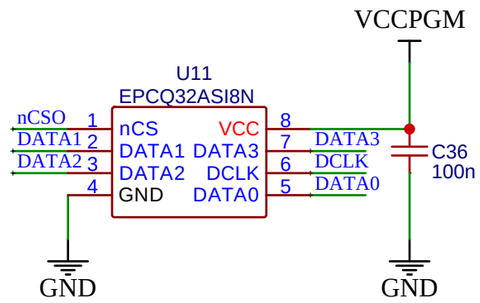
CLOCK & FPGA CONFIGURATION



JTAG HEADER

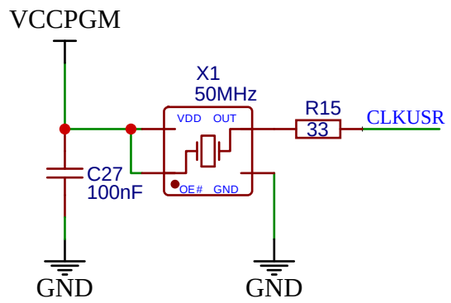


AS HEADER

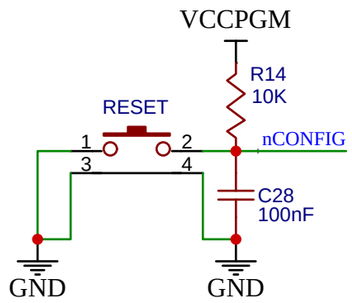


CONFIG EEPROM

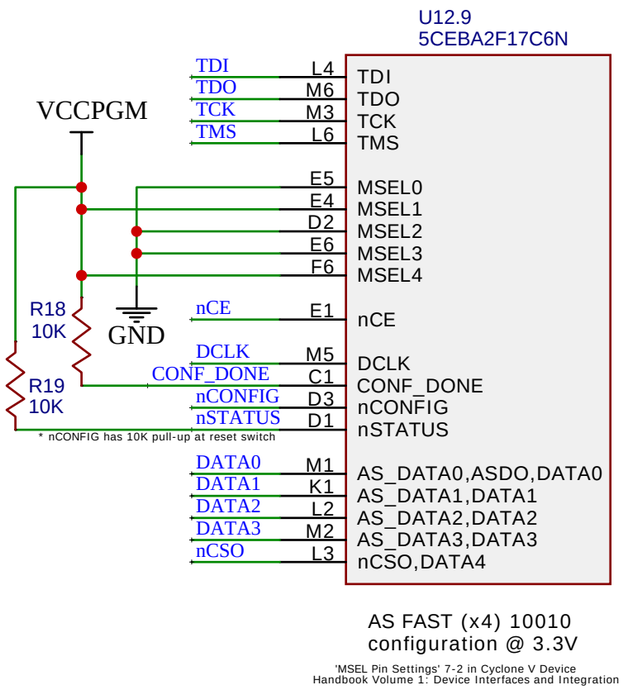
* Minimum 32Mbit EEPROM required for 21Mbit image



50 MHz CLOCK



FPGA RESET



AS FAST (x4) 10010 configuration @ 3.3V

'MSEL Pin Settings' 7-2 in Cyclone V Device Handbook Volume 1: Device Interfaces and Integration

TITLE: Cyclone V GPU		REV: 1.0
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	Date: 2020-06-25 Drawn By: nockieboy	

Cyclone V FPGA

NOTE: Cyclone V A2 and A4 versions are pin-compatible and interchangeable on this PCB design.

U12.1
5CEBA2F17C6N
BANK 2A

IO,(DIFFIO_TX_L9p,DIFFOUT_L9p,DQ1L)	F4
IO,(DIFFIO_TX_L9n,DIFFOUT_L9n)	F3
IO,(DIFFIO_RX_L10p,DIFFOUT_L10p,DQ1L)	H3
IO,(DIFFIO_RX_L10n,DIFFOUT_L10n,DQ1L)	G3
IO,(DIFFIO_RX_L11p,DIFFOUT_L11p,DQS1L)	H5
IO,(DIFFIO_RX_L11n,DIFFOUT_L11n,DQSn1L)	H4
IO,(DIFFIO_TX_L12p,DIFFOUT_L12p)	F2
IO,(DIFFIO_TX_L12n,DIFFOUT_L12n,DQ1L)	E2
IO,(DIFFIO_TX_L13p,DIFFOUT_L13p,DQ1L)	G2
IO,(DIFFIO_TX_L13n,DIFFOUT_L13n,DQ1L)	G1
IO,(DIFFIO_RX_L14p,DIFFOUT_L14p,DQ1L)	J3
IO,(DIFFIO_RX_L14n,DIFFOUT_L14n,DQ1L)	J2
IO,(DIFFIO_RX_L15p,DIFFOUT_L15p)	K5
IO,(DIFFIO_RX_L15n,DIFFOUT_L15n)	K4
IO,(DIFFIO_TX_L16p,DIFFOUT_L16p,DQ1L)	J1
IO,(DIFFIO_TX_L16n,DIFFOUT_L16n,DQ1L)	H1

U12.2
5CEBA2F17C6N
BANK 3A

IO,DATA8,(DIFFIO_RX_B1p,DIFFOUT_B1p,DQ1B)	P4 SD_CMD
IO,DATA6,(DIFFIO_RX_B1n,DIFFOUT_B1n,DQ1B)	N4 SD_D3
IO,DATA7,(DIFFIO_TX_B2p,DIFFOUT_B2p,DQ1B)	P1 SD_D1
IO,DATA5,(DIFFIO_TX_B2n,DIFFOUT_B2n)	N1 SD_D2
IO,DATA12,(DIFFIO_RX_B3p,DIFFOUT_B3p,DQS1B)	L7 IOR
IO,DATA10,(DIFFIO_RX_B3n,DIFFOUT_B3n,DQSn1B)	M7 SD_CLK
IO,DATA11,(DIFFIO_TX_B4p,DIFFOUT_B4p)	P2 A0
IO,DATA9,(DIFFIO_TX_B4n,DIFFOUT_B4n,DQ1B)	R1 SD_D0
IO,CLKUSR,(DIFFIO_RX_B5p,DIFFOUT_B5p,DQ1B)	N3 CLKUSR
IO,DATA14,(DIFFIO_RX_B5n,DIFFOUT_B5n,DQ1B)	P3 A3
IO,DATA15,(DIFFIO_TX_B6p,DIFFOUT_B6p,DQ1B)	R2 A1
IO,DATA13,(DIFFIO_TX_B6n,DIFFOUT_B6n,DQ1B)	T2 A2
IO,PR_ERROR,(DIFFIO_RX_B7p,DIFFOUT_B7p)	P7 A11
IO,PR_DONE,(DIFFIO_RX_B7n,DIFFOUT_B7n)	R6 A8
IO,(DIFFIO_TX_B8p,DIFFOUT_B8p,DQ1B)	R4 A5
IO,PR_READY,(DIFFIO_TX_B8n,DIFFOUT_B8n,DQ1B)	T3 A4

U12.3
5CEBA2F17C6N
BANK 3B

IO,(DIFFIO_TX_B17p,DIFFOUT_B17p,DQ2B)	T4 A6
IO,(DIFFIO_TX_B17n,DIFFOUT_B17n)	T5 A7
IO,(DIFFIO_RX_B18p,DIFFOUT_B18p,DQ2B)	P8 A13
IO,(DIFFIO_RX_B18n,DIFFOUT_B18n,DQ2B)	R7 A10
IO,(DIFFIO_RX_B19p,DIFFOUT_B19p,DQS2B)	L9 IOB
IO,(DIFFIO_RX_B19n,DIFFOUT_B19n,DQSn2B)	M8 IOC
IO,(DIFFIO_TX_B20p,DIFFOUT_B20p)	T8 A12
IO,(DIFFIO_TX_B20n,DIFFOUT_B20n,DQ2B)	T7 A9
IO,FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB,(DIFFIO_TX_B21p,DIFFOUT_B21p,DQ2B)	R12 E19
IO,FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn,(DIFFIO_TX_B21n,DIFFOUT_B21n,DQ2B)	R11 E14
IO,(DIFFIO_RX_B22p,DIFFOUT_B22p,DQ2B)	T13 E20
IO,(DIFFIO_RX_B22n,DIFFOUT_B22n,DQ2B)	T12 E18
IO,CLK1p,(DIFFIO_RX_B23p,DIFFOUT_B23p)	P9 A15
IO,CLK1n,(DIFFIO_RX_B23n,DIFFOUT_B23n)	R9 A14
IO,(DIFFIO_TX_B24p,DIFFOUT_B24p,DQ2B)	R10 EA_OE
IO,(DIFFIO_TX_B24n,DIFFOUT_B24n,DQ2B)	T10 EA_DIR

U12.4
5CEBA2F17C6N
BANK 4A

IO,(DIFFIO_TX_B25p,DIFFOUT_B25p,DQ3B)	P16 HS
IO,RZQ_0,(DIFFIO_TX_B25n,DIFFOUT_B25n)	R15 PS2_KCLK
IO,(DIFFIO_RX_B26p,DIFFOUT_B26p,DQ3B)	R16 DE
IO,(DIFFIO_RX_B26n,DIFFOUT_B26n,DQ3B)	T15 PS2_MDAT
IO,(DIFFIO_RX_B27p,DIFFOUT_B27p,DQS3B)	L10
IO,(DIFFIO_RX_B27n,DIFFOUT_B27n,DQSn3B)	M10
IO,(DIFFIO_TX_B28p,DIFFOUT_B28p)	N14
IO,(DIFFIO_TX_B28n,DIFFOUT_B28n,DQ3B)	M13
IO,(DIFFIO_TX_B29p,DIFFOUT_B29p,DQ3B)	P13 E21
IO,(DIFFIO_TX_B29n,DIFFOUT_B29n,DQ3B)	P14 VS
IO,(DIFFIO_RX_B30p,DIFFOUT_B30p,DQ3B)	M11 E17
IO,(DIFFIO_RX_B30n,DIFFOUT_B30n,DQ3B)	M12
IO,CLK2p,(DIFFIO_RX_B31p,DIFFOUT_B31p)	N11 E16
IO,CLK2n,(DIFFIO_RX_B31n,DIFFOUT_B31n)	P11 E15
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B)	R14 PS2_KDAT
IO,(DIFFIO_TX_B32n,DIFFOUT_B32n,DQ3B)	T14 PS2_MCLK

U12.5
5CEBA2F17C6N
BANK 5A

IO,RZQ_1,(DIFFIO_TX_R1p,DIFFOUT_R1p,DQ1R)	N15 B1
IO,PR_REQUEST,(DIFFIO_TX_R1n,DIFFOUT_R1n,DQ1R)	N16 B0
IO,INIT_DONE,(DIFFIO_RX_R2p,DIFFOUT_R2p)	L13 B4
IO,CRC_ERROR,(DIFFIO_RX_R2n,DIFFOUT_R2n)	K14 B6
IO,nCEO,(DIFFIO_TX_R3p,DIFFOUT_R3p,DQ1R)	H16 G3
IO,CvP_CONFDONE,(DIFFIO_TX_R3n,DIFFOUT_R3n,DQ1R)	J16 G0
IO,(DIFFIO_RX_R4p,DIFFOUT_R4p,DQ1R)	L14 B3
IO,(DIFFIO_RX_R4n,DIFFOUT_R4n,DQ1R)	L15 B2
IO,DEV_OE,(DIFFIO_TX_R5p,DIFFOUT_R5p)	G15 G7
IO,DEV_CLRn,(DIFFIO_TX_R5n,DIFFOUT_R5n,DQ1R)	G16 G6
IO,(DIFFIO_RX_R6p,DIFFOUT_R6p,DQS1R)	K12 B7
IO,(DIFFIO_RX_R6n,DIFFOUT_R6n,DQSn1R)	J12 G2
IO,(DIFFIO_TX_R7p,DIFFOUT_R7p,DQ1R)	J14 G1
IO,(DIFFIO_TX_R7n,DIFFOUT_R7n)	H15 G4
IO,(DIFFIO_RX_R8p,DIFFOUT_R8p,DQ1R)	K15 DAC_CLK
IO,(DIFFIO_RX_R8n,DIFFOUT_R8n,DQ1R)	K16 B5

U12.6
5CEBA2F17C6N
BANK 5B

IO,CLK6p,(DIFFIO_RX_R9p,DIFFOUT_R9p)	F12 D4
IO,CLK6n,(DIFFIO_RX_R9n,DIFFOUT_R9n)	G12 R0
IO,(DIFFIO_TX_R10p,DIFFOUT_R10p,DQ2R)	E16 R5
IO,(DIFFIO_TX_R10n,DIFFOUT_R10n,DQ2R)	D16 R7
IO,(DIFFIO_RX_R11p,DIFFOUT_R11p,DQ2R)	E12 D5
IO,(DIFFIO_RX_R11n,DIFFOUT_R11n,DQ2R)	D13 Z80_nRES
IO,FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB,(DIFFIO_TX_R12p,DIFFOUT_R12p,DQ2R)	B16 Z80_INTAK
IO,FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn,(DIFFIO_TX_R12n,DIFFOUT_R12n,DQ2R)	C16 Z80_nCLK
IO,(DIFFIO_RX_R13p,DIFFOUT_R13p,DQS2R)	H13 G5
IO,(DIFFIO_RX_R13n,DIFFOUT_R13n,DQSn2R)	G13 R1
IO,(DIFFIO_TX_R14p,DIFFOUT_R14p)	B15 Z80_nWR
IO,(DIFFIO_TX_R14n,DIFFOUT_R14n,DQ2R)	C15 Z80_nMREQ
IO,(DIFFIO_RX_R15p,DIFFOUT_R15p,DQ2R)	F14 R2
IO,(DIFFIO_RX_R15n,DIFFOUT_R15n,DQ2R)	F15 R3
IO,(DIFFIO_TX_R16p,DIFFOUT_R16p,DQ2R)	D14 R6
IO,(DIFFIO_TX_R16n,DIFFOUT_R16n)	E15 R4

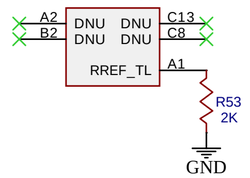
U12.7
5CEBA2F17C6N
BANK 7A

IO,CLK10p,(DIFFIO_RX_T17p,DIFFOUT_T17p)	F11 D0
IO,CLK10n,(DIFFIO_RX_T17n,DIFFOUT_T17n)	F10 DAC_D0
IO,(DIFFIO_TX_T18p,DIFFOUT_T18p,DQ1T)	A15 Z80_nRD
IO,(DIFFIO_TX_T18n,DIFFOUT_T18n,DQ1T)	A14 Z80_nIORQ
IO,(DIFFIO_RX_T19p,DIFFOUT_T19p,DQ1T)	D11 D1
IO,(DIFFIO_RX_T19n,DIFFOUT_T19n,DQ1T)	C11 D2
IO,(DIFFIO_TX_T20p,DIFFOUT_T20p,DQ1T)	A13 Z80_nM1
IO,(DIFFIO_TX_T20n,DIFFOUT_T20n,DQ1T)	A12 D7
IO,(DIFFIO_RX_T21p,DIFFOUT_T21p,DQS1T)	E10 DAC_A1
IO,(DIFFIO_RX_T21n,DIFFOUT_T21n,DQSn1T)	E9 DAC_D3
IO,(DIFFIO_TX_T22p,DIFFOUT_T22p)	B12 D6
IO,(DIFFIO_TX_T22n,DIFFOUT_T22n,DQ1T)	B11 D3
IO,(DIFFIO_RX_T23p,DIFFOUT_T23p,DQ1T)	C10
IO,(DIFFIO_RX_T23n,DIFFOUT_T23n,DQ1T)	C9 DAC_D1
IO,(DIFFIO_TX_T24p,DIFFOUT_T24p,DQ1T)	B10 245_OE
IO,RZQ_2,(DIFFIO_TX_T24n,DIFFOUT_T24n)	A10 245_DIR

U12.8
5CEBA2F17C6N
BANK 8A

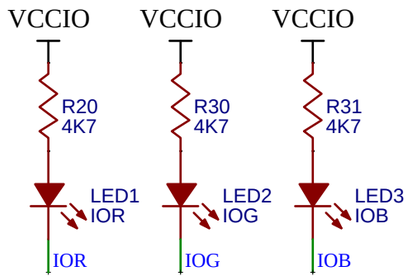
IO,CLK9p,(DIFFIO_RX_T25p,DIFFOUT_T25p)	F8 DAC_D6
IO,CLK9n,(DIFFIO_RX_T25n,DIFFOUT_T25n)	F7
IO,(DIFFIO_TX_T26p,DIFFOUT_T26p,DQ2T)	A8 DAC_D2
IO,(DIFFIO_TX_T26n,DIFFOUT_T26n,DQ2T)	A9 DAC_A0
IO,(DIFFIO_RX_T27p,DIFFOUT_T27p,DQ2T)	B8 DAC_D4
IO,(DIFFIO_RX_T27n,DIFFOUT_T27n,DQ2T)	A7 DAC_D7
IO,FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB,(DIFFIO_TX_T28p,DIFFOUT_T28p,DQ2T)	A5
IO,FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn,(DIFFIO_TX_T28n,DIFFOUT_T28n,DQ2T)	A4
IO,(DIFFIO_RX_T29p,DIFFOUT_T29p,DQS2T)	D8 DAC_D5
IO,(DIFFIO_RX_T29n,DIFFOUT_T29n,DQSn2T)	D7
IO,(DIFFIO_TX_T30p,DIFFOUT_T30p)	B3 UART_TX
IO,(DIFFIO_TX_T30n,DIFFOUT_T30n,DQ2T)	A3 UART_RX
IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T)	B7 DAC_nWR
IO,(DIFFIO_RX_T31n,DIFFOUT_T31n,DQ2T)	B6
IO,(DIFFIO_TX_T32p,DIFFOUT_T32p,DQ2T)	C3
IO,(DIFFIO_TX_T32n,DIFFOUT_T32n)	C4

U12.12
5CEBA2F17C6N

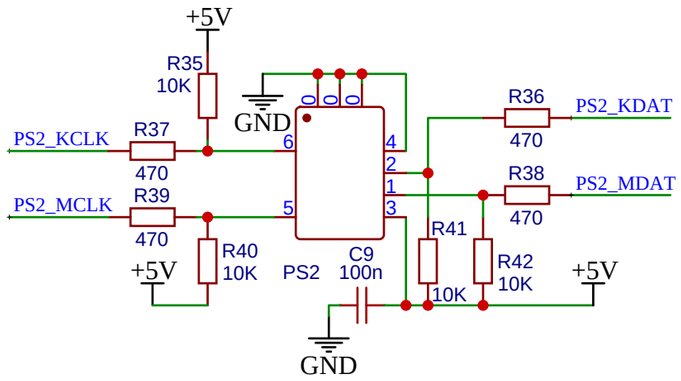


TITLE: Cyclone V GPU			REV: 1.0
EasyEDA	Company: 10103		Sheet: 1/1
	Date: 2020-06-19	Drawn By: nockieboy	

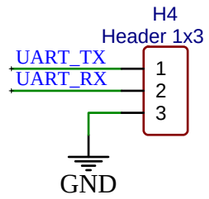
PERIPHERALS



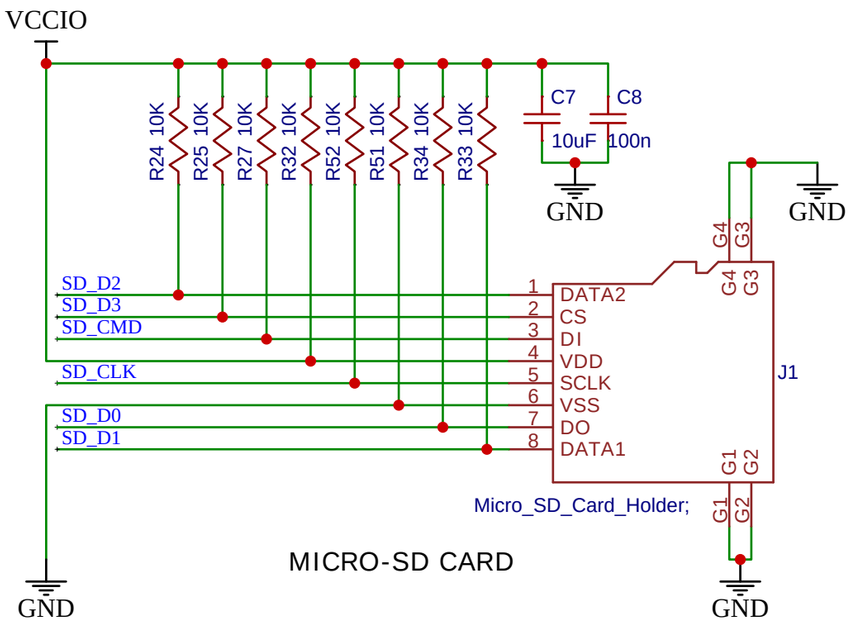
GPIO LEDS



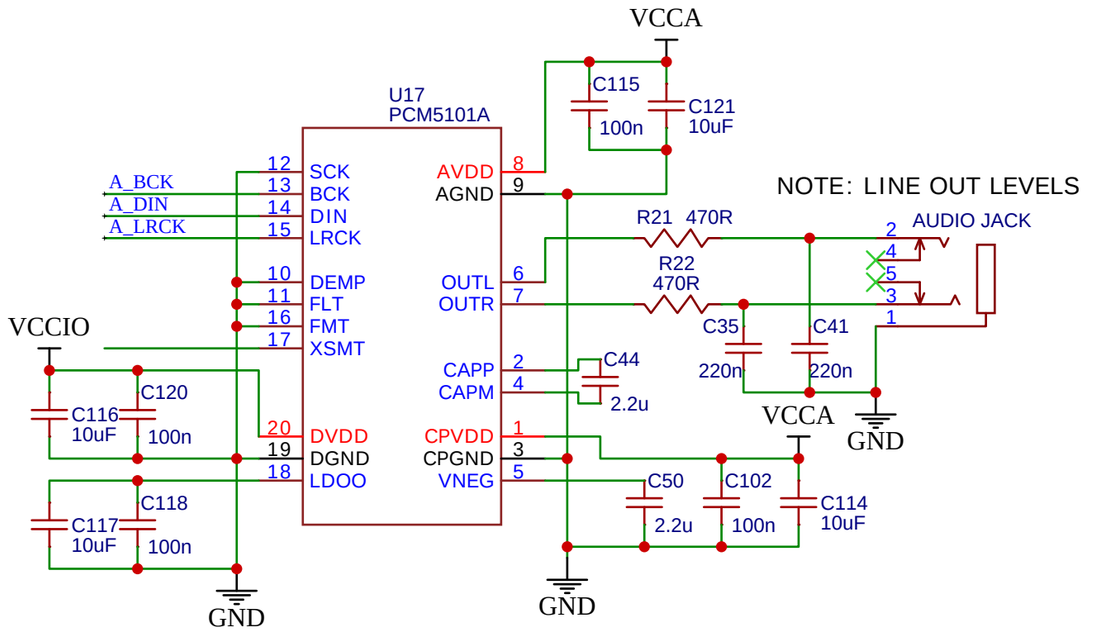
PS2 KEYBOARD/MOUSE



3.3V SERIAL DEBUG PORT



MICRO-SD CARD



24-bit AUDIO DAC

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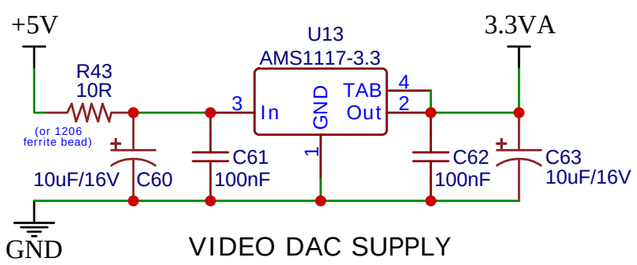
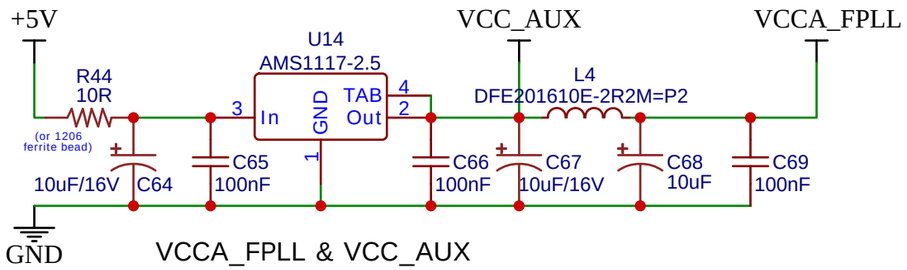
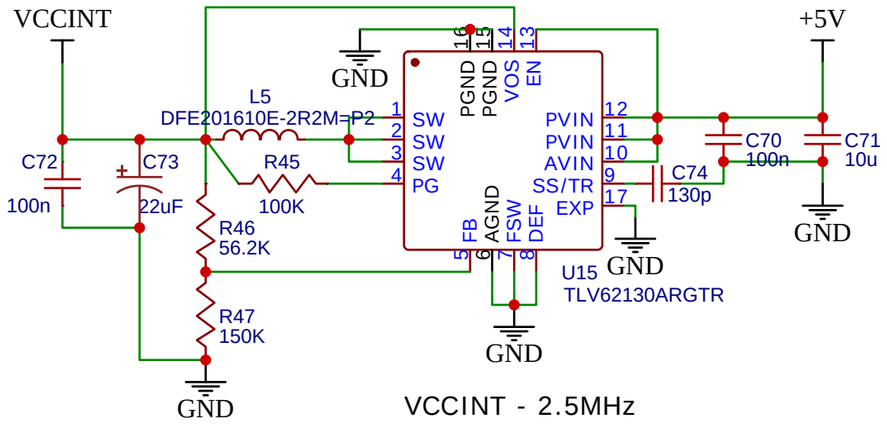
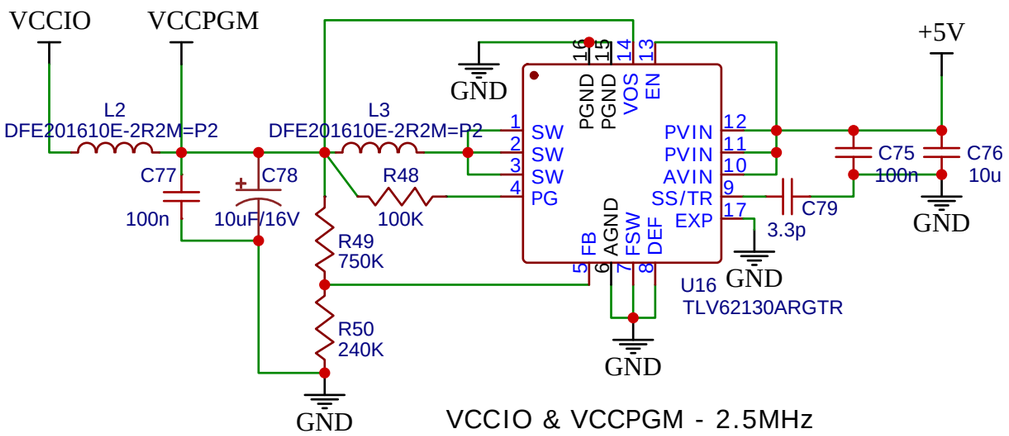
POWER SUPPLIES

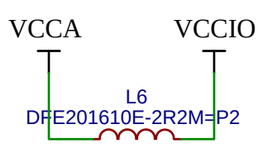


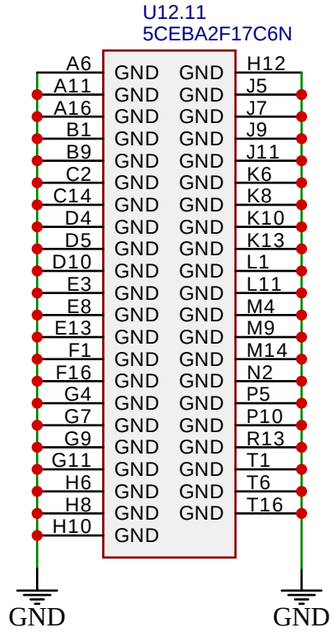


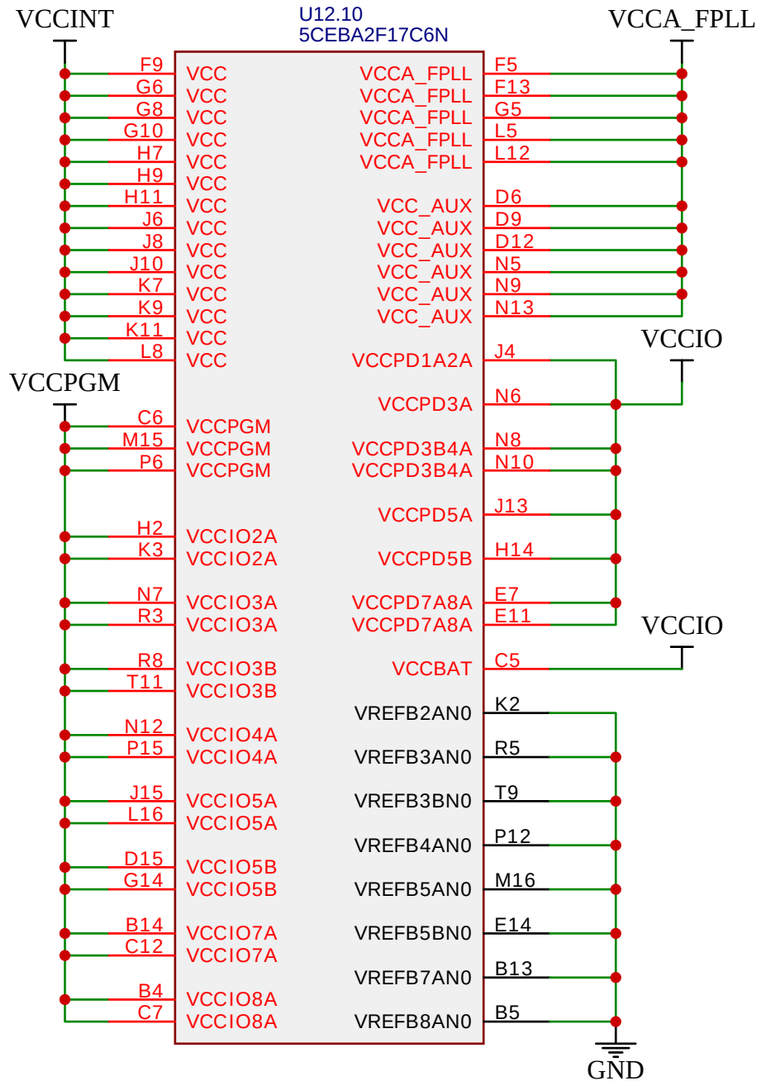
DESIGN NOTE: All 10uF/22uF components are SMD 3216 tantalum caps.











Supplies: U13 - 3.3V supply (3.3VA)
U14 - 2.5V supply (VCCA_FPLL, VCC_AUX)
U15 - 1.1V supply (VCCINT)
U16 - 3.3V supply (VCCIO, VCCPGM, VCCA)

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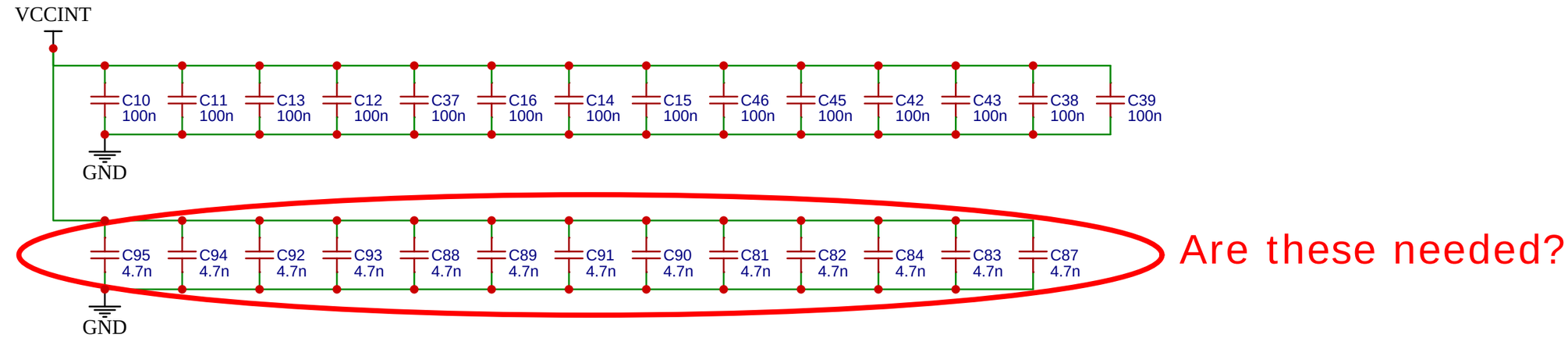
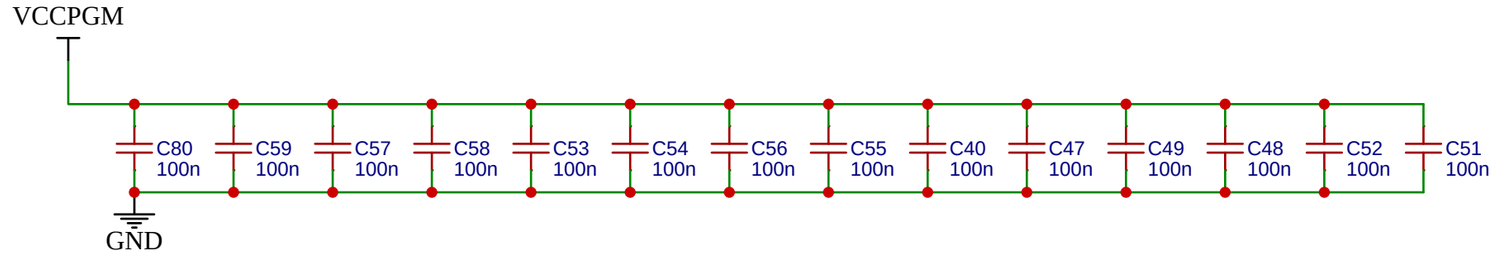
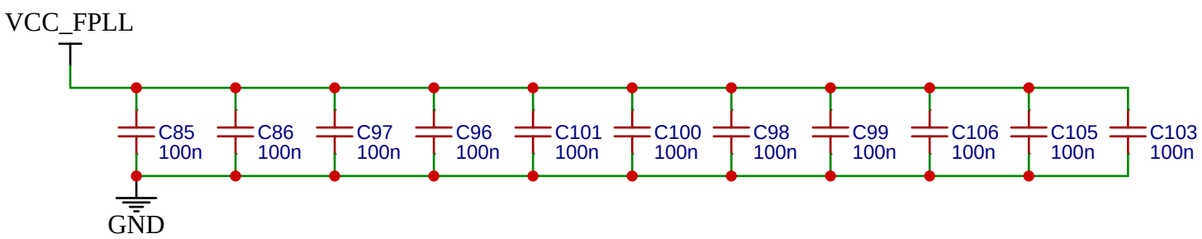
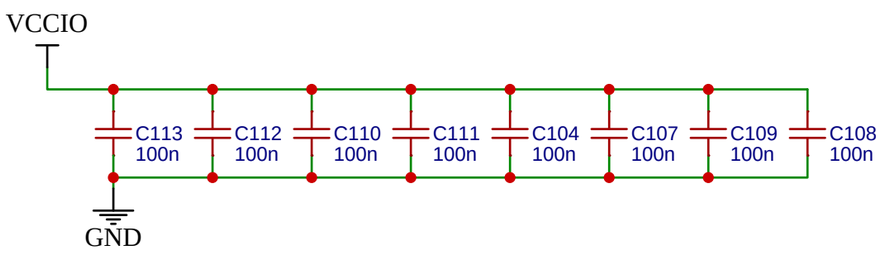
FPGA DECOUPLING

Note: Place capacitors near FPGA pins









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