Project Description

In this project you are asked to implement a single-cycle processor. Your processor should handle the following subset of the MIPS instruction set:

- arithmetic: add, addi, addu, sub, subu
- logical: and, or, sll
- data transfer: lw, sw
- conditional branch: beq, bne, slt, sltu

As part of the implementation, you should design, implement, and test a 32-entry register file, an ALU (you can use your ALU from the individual project), and a control mechanism. A VHDL library is included on this assignment. You cannot use any other components.

Test Files

The format of the input files is

address / data_at_address;

Thus, the input file has one address-data pair per line in hex. Comment lines are allowed, and must begin with a #. There are three test files attached to the assignment, so you don't need to write your own test files. Here are the test programs:

- a sort program – sort_corrected_branch.dat
- a summation program – unsigned_sum.dat
- a simple transaction simulator – bills_branch.dat

The test files are extracted from a MIPS simulator called SPIM. The simulator assumes that code begins at address 0x00400020, so make sure that the program counter is loaded with this initial value.

THINGS TO TURN IN:

You should turn in a report describing and justifying your design decisions and describing the problems you have encountered and how you solved them. In addition to this report, please submit:

1. All your VHDL codes (datapath, register file, ALU, etc.)
2. A table summarizing the control signals.
3. Traces of running the above programs, demonstrating that the correct result was obtained (i.e., you have to figure out what the program did, and show the memory location(s) where the results are stored).

Please note that you will do a demo of your processor.

Please, submit your report electronically through blackboard before the deadline or bring a hard copy to your demo.

Deadlines:

You have to form your project groups by **Friday, October 31st, at 2pm**. At this time, I will make group assignments of the remaining students randomly.

If you have already formed a group and told me about it, you should see your group members on Canvas. If you see nothing there, it means you haven't formed a group yet, or you haven't contacted me about it. Again, I will randomly assign to groups any student who has not contacted me by the above deadline. Group assignments are final, so it is in your best interest to choose your teammates yourselves, rather than rely on my random choices.

The demos will be held on **Monday, November 24th** throughout the day. There will be a signup sheet for determining the exact time of your demo. Your project reports are due the end of day, November 24th.