

# ES\_LPC11Cxx

## Errata sheet LPC11C12/14/22/24

Rev. 3 — 1 March 2011

Errata sheet

### Document information

Info	Content
<b>Keywords</b>	LPC11C12, LPC11C22, LPC11C14, LPC11C24 errata
<b>Abstract</b>	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table.</p>



## Revision history

Rev	Date	Description
3	20110301	<ul style="list-style-type: none"><li>• Combined errata for LPC11C12, LPC11C14, LPC11C22, and LPC11C24 into one document.</li><li>• Added VDD.1.</li><li>• <a href="#">Section 3.1</a>: Removed text “For PCLK_ADC = 100 MHz....”</li></ul>
2	20101115	<ul style="list-style-type: none"><li>• Added ADC.1.</li></ul>
1	20100510	<ul style="list-style-type: none"><li>• Initial version</li></ul>

## Contact information

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## 1. Product identification

The LPC11Cxx devices typically have the following top-side marking:

LPC11Cxxx  
/xxx  
xxxxxxx  
xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC11Cxx:

**Table 1. Device revision table**

Revision identifier (R)	Revision description
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

## 2. Errata overview

**Table 2. Functional problems table**

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	External sync inputs not operational	'A'	<a href="#">Section 3.1 on page 4</a>
VDD.1	The minimum voltage of the power supply ramp must be 200 mV or below	'A'	<a href="#">Section 3.2 on page 5</a>

**Table 3. AC/DC deviations table**

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

**Table 4. Errata notes**

Note	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

### 3. Functional problems detail

#### 3.1 ADC.1: External sync inputs not operational

##### Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START	When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
0x0		No start (this value should be used when clearing PDN to 0).	
0x1		Start conversion now.	
0x2		Start conversion when the edge selected by bit 27 occurs on PIO0_2/SSEL/CT16B0_CAP0.	
0x3		Start conversion when the edge selected by bit 27 occurs on PIO1_5/DIR/CT32B0_CAP0.	
0x4		Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT0.	
0x5		Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT1.	
0x6		Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT0.	
0x7		Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT1.	

##### Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on PIO0\_2 or PIO1\_5 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK\_ADC = 50 MHz, probability error = 6 %
- For PCLK\_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

##### Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

### 3.2 VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below

#### Introduction:

The datasheet specifies that the power supply (on the VDD pin) must ramp-up from a minimum voltage of 400 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the VDD pin) needs to be below 400 mV or below before ramping up is 12 us.

#### Problem:

The device might not always start-up if the power supply (on the VDD pin) does not reach 200 mV. The minimum voltage of the power supply ramp (on the VDD pin) must be 200 mV or below with ramp-up time of 500 ms or faster.

#### Work-around:

None.

## 4. AC/DC deviations detail

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No known errata.

## 5. Errata notes

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No known errata.

## 6. Legal information

### 6.1 Definitions

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