ADEN ESEAS BRIANO

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Education

Rice University – Houston, TX **Expected May 2026**

BS in Electrical and Computer Engineering **GPA:** 3.5 / 4.0

Relevant Coursework: Digital Logic Design, Microcontroller Programming, Analog Circuits Laboratory, Digital IC Design, Fundamentals of Machine Learning, VLSI, Engineering Design, Advanced VLSI, High Performance Computer Architecture

Affiliations: Society of Hispanic Professional Engineers (SHPE), Questbridge, Colorstack, Rice Robotics, INROADS

Skills

Software: FPGA Programming, Vivado, Verilog, Python, C, C++, MATLAB, Java, JavaScript, HTML/CSS, LaTeX, Matplotlib

Hardware: Spartan-7, Soldering, PCB Design, 3D Printing, Laser Cutting, Iterative Prototyping

Developer Tools: LTspice, EAGLE, KiCad, Magic, Irsim, Cadence Virtuoso, PocketBeagle, Arduino, ESP32, MSPM0, CCS

Experience

Rover Electrical Team Lead, Rice University Robotics Club – Houston, TX **Sep 2024 – Present**

- Organize and lead 2 weekly meetings for the Electrical Sub Team, utilizing Slack for team coordination
- Document project progress and communicate with **10+** other officers and leads regarding changes to project timeline
- Guide **10+** new members in the current progress of the project in the Electrical subdivision and assign them responsibilities for each meeting

MidWeek Math Trainer, Rice University Math Department – Houston, TX **Aug 2024 – May 2025**

- Collaborate with the Rice University Math Department in a team of 4 to deliver focused support through tailored review sessions twice a week for **50+** students currently enrolled in Calculus I and Calculus II
- Lead engaging exam review sessions for **200+** students currently enrolled in Calculus I and Calculus II
- Create exam keys to be sent out to attending students, and write mock exam problems for future review sessions

Rice Emerging Scholars Program Fellow, Rice University – Houston, TX **Jul 2024 – Aug 2024**

- Worked closely in a team of 9 for 8 weeks to facilitate academic and social support for **50** FGLI (First Gen Limited Income) incoming freshmen pursuing STEM degrees
- Mentored 3 engineering design teams, guiding project development and fostering collaborative problem-solving
- Led **72** hours of focused group work sessions, teaching scholars effective collaboration in a group academic setting
- Hosted **15+** Office Hours and 6 exam review sessions throughout the duration of the program for Calculus/Physics

Projects

16-Bit Processor | Verilog, FPGA Programming, Vivado **Sep 2024 – Dec 2024**

- Designed **Verilog** logic for emulation of a 16-bit processor, implemented using **Vivado** onto a **Real Digital Boolean Board** with button and switch inputs
- Developed a 16-bit one-cycle processor capable of executing simple assembly instructions for arithmetic operations

Snake Game ASIC | Verilog, Magic, Questa Sim, Innovus P&R, Design Compiler **Jan 2025 – May 2025**

https://github.com/BrianoAden/SnakeASIC

- Designed an FSM Controller/Datapath architecture in **Verilog** to emulate the classic Snake game in **static CMOS** Logic
- Used **Questa Sim** to simulate and analyze the behavior of the **Verilog** logic and verify the functionality of the game
- Used **Design Compiler** to optimize the **Verilog** logic, and **Innovus** to place and route our design for **Magic** injection

Adder Design Competition | Cadence Virtuoso **April 2025 - May 2025**

- Implemented a **Full Adder** and **Multiplexer** in various logic families to determine the design that yielded the smallest propagation delay for each device
- Developed various Carry-Select **32-bit Adder** architectures using the fastest **Full Adder** and **Multiplexer** designs
- Calculated **logical effort**, **transistor sizings**, **EDP,** and **critical paths** for all **32-bit Adder** architectures