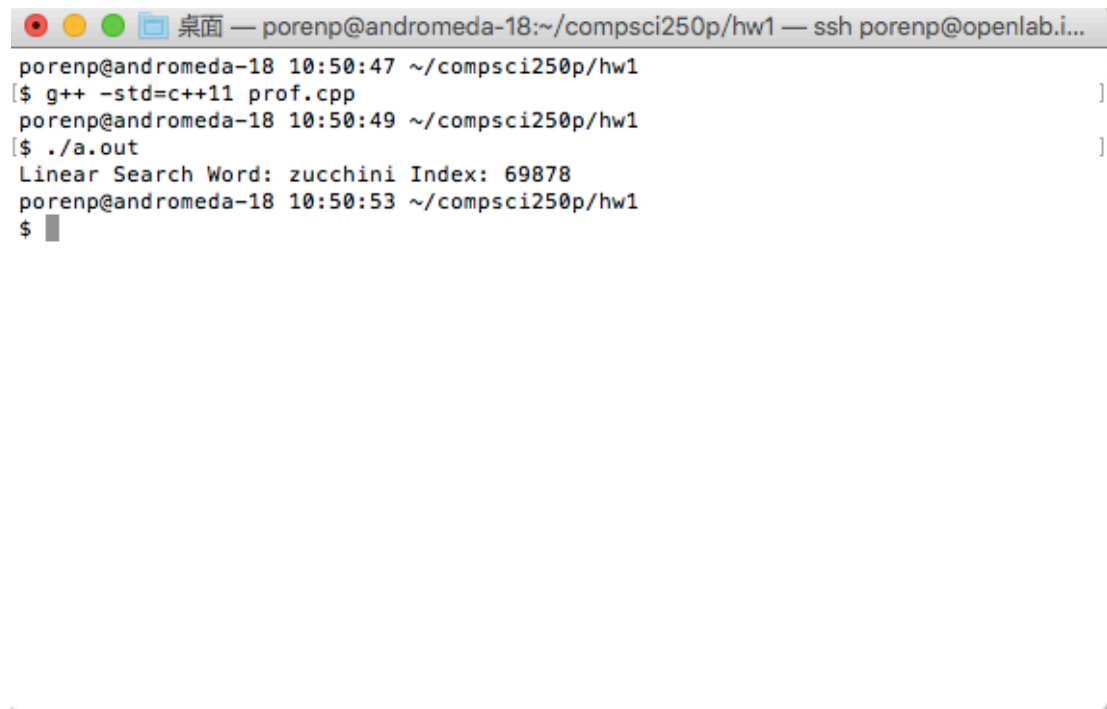


Homework 1 Report 1

Notice : Because writing two searches in the same program, so it should comment one and run the other to get the answer.

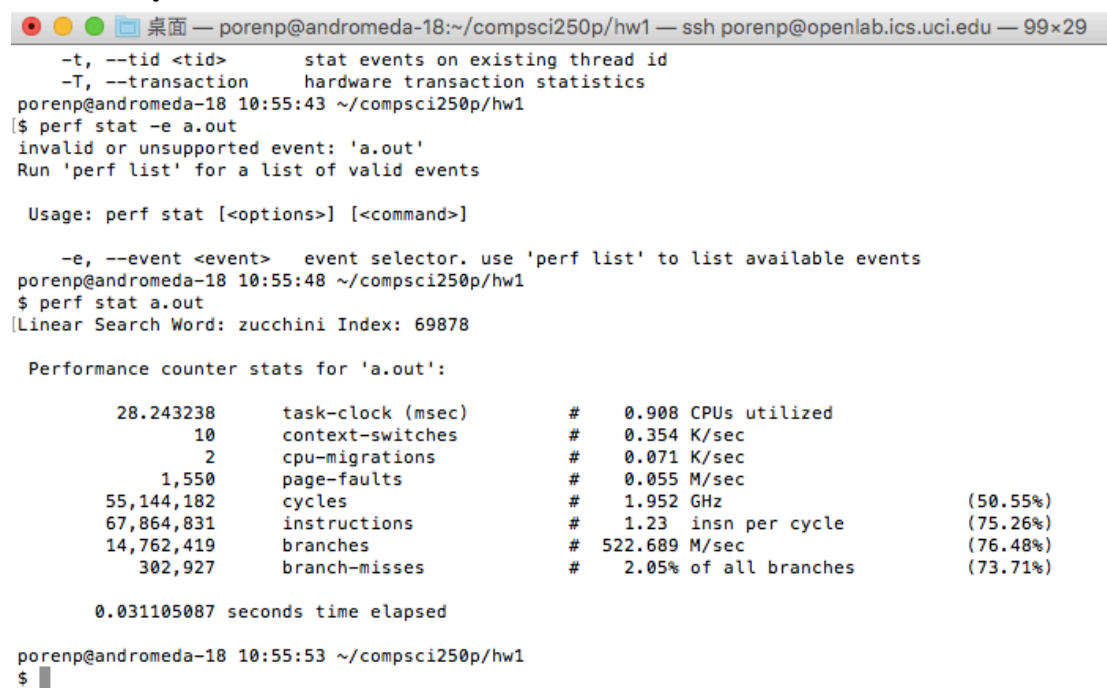
Linear Search



```
poren@andromeda-18 10:50:47 ~/compsci250p/hw1
[$ g++ -std=c++11 prof.cpp
poren@andromeda-18 10:50:49 ~/compsci250p/hw1
[$ ./a.out
Linear Search Word: zucchini Index: 69878
poren@andromeda-18 10:50:53 ~/compsci250p/hw1
$
```

Figure 1: The compile and execution of the linear search

Perf analysis



```
poren@andromeda-18 10:55:43 ~/compsci250p/hw1
[$ perf stat -e a.out
invalid or unsupported event: 'a.out'
Run 'perf list' for a list of valid events

Usage: perf stat [<options>] [<command>]

-e, --event <event>  event selector. use 'perf list' to list available events
poren@andromeda-18 10:55:48 ~/compsci250p/hw1
$ perf stat a.out
Linear Search Word: zucchini Index: 69878

Performance counter stats for 'a.out':

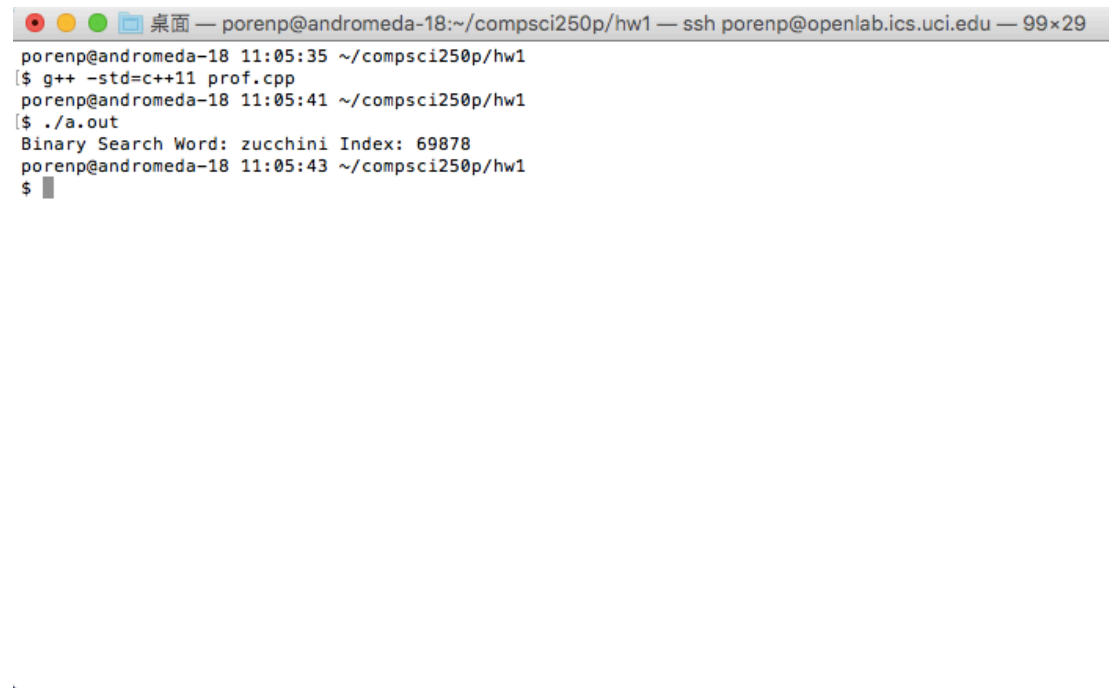
      28.243238 task-clock (msec)          #    0.908 CPUs utilized
           10 context-switches            #    0.354 K/sec
             2 cpu-migrations             #    0.071 K/sec
        1,550 page-faults                 #    0.055 M/sec
  55,144,182 cycles                        #    1.952 GHz                    (50.55%)
  67,864,831 instructions                 #    1.23 insns per cycle         (75.26%)
  14,762,419 branches                    # 522.689 M/sec                   (76.48%)
    302,927 branch-misses                 #    2.05% of all branches       (73.71%)

0.031105087 seconds time elapsed

poren@andromeda-18 10:55:53 ~/compsci250p/hw1
$
```

Figure 2: The result of perf for linear search

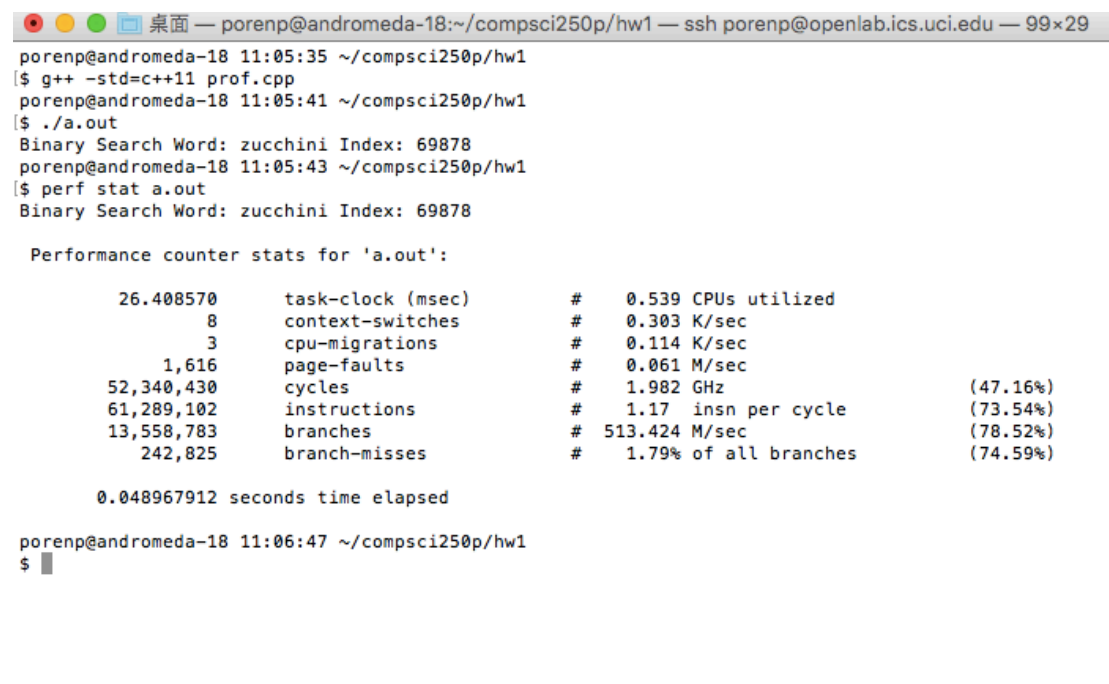
Binary Search



```
poren@andromeda-18:~/compsci250p/hw1 — ssh poren@openlab.ics.uci.edu — 99x29
poren@andromeda-18 11:05:35 ~/compsci250p/hw1
$ g++ -std=c++11 prof.cpp
poren@andromeda-18 11:05:41 ~/compsci250p/hw1
$ ./a.out
Binary Search Word: zucchini Index: 69878
poren@andromeda-18 11:05:43 ~/compsci250p/hw1
$
```

Figure 3: The compile and execution of the binary search

Perf analysis



```
poren@andromeda-18:~/compsci250p/hw1 — ssh poren@openlab.ics.uci.edu — 99x29
poren@andromeda-18 11:05:35 ~/compsci250p/hw1
$ g++ -std=c++11 prof.cpp
poren@andromeda-18 11:05:41 ~/compsci250p/hw1
$ ./a.out
Binary Search Word: zucchini Index: 69878
poren@andromeda-18 11:05:43 ~/compsci250p/hw1
$ perf stat a.out
Binary Search Word: zucchini Index: 69878

Performance counter stats for 'a.out':

    26.408570 task-clock (msec)    #    0.539 CPUs utilized
           8 context-switches     #    0.303 K/sec
           3 cpu-migrations        #    0.114 K/sec
        1,616 page-faults         #    0.061 M/sec
   52,340,430 cycles                #    1.982 GHz                    (47.16%)
   61,289,102 instructions          #    1.17 insn per cycle          (73.54%)
   13,558,783 branches              # 513.424 M/sec                   (78.52%)
    242,825 branch-misses          #    1.79% of all branches        (74.59%)

0.048967912 seconds time elapsed

poren@andromeda-18 11:06:47 ~/compsci250p/hw1
$
```

Figure 4: The result of perf for binary search

Term explanation

Use *Figure 4* as an example

- **Context-Switches :** In figure 4, there is 8 context switches and 0.303K/sec in binary search.
The term called context switches means the switches of the CPU from one process or thread to another. The context switches performs the following steps:
 1. Suspend progression of current process/thread, store the state for that process/thread to the memory
 2. Retrieve the context of next process/thread from the memory and store them to the register.
 3. Return the location and resume the state of the next process/thread.
- **Page Faults:** In figure 4, it shows 1,616 page faults and 0.061M/sec in binary search.
The term called page faults means that when a program doesn't find its' data or instruction in virtual memory. Then, it should go to physical memory to fetch them.
- **IPC(Instructions Per Cycle):** The IPC for binary search is 1.17 which can be derived from instructions/cycles. The IPC highly relates the speed of execution. That's because CPU has its' own clock speed. We can take 4GHz CPU as an example. It runs 4×10^9 cycles per second. In other words, when IPC value raises, CPU can run more instructions in a second. Hence, the efficiency would be better than before.
- **Branch Misses:** The binary search has 242,825 branch misses. That is about 1.79% of all branches. Branch Misses will happen when CPU mispredict the next instruction to execute. The reason why CPU would predict the next instruction to execute is to make pipeline efficiently and speed up the execution.