Computer System Architecture HW 2

1) (20 pts) Integer pipeline (Fig. 2.3). Assume that registers are written in the 1st half of the clock cycle, read in the 2nd half. Show cycle by cycle execution of the following code segment. Identify every possible type of hazard, mark the hazards by arrows. The processor does not use forwarding, resolve all hazards by stalling. Shows stalls as letter "S" in an appropriate cycle. Execute all instructions shown after the branch is resolved. The branch is not taken (after it is resolved).

Instr/Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Xor R4, R5, R9	IF	ID	EX	M	WB												
Add R1, R1, #4		IF	ID	EX	M	WB											
Sub R6, R5, R4 <- Data Hazzard			IF	ID	S	EX	M	WB									
BNE R1, R7, L_ <- Data,Control Hazzard				IF	S	ID	EX	M	WB								
Ld R5, 52(R6)					S	IF	S	IF	ID	EX	M	WB					
St R6, 8(R4)							S		IF	ID	EX	M	WB				
Sub R7, R5, R4 <- Data Hazzard										IF	ID	S	EX	M	WB		
Add R2, R5, R7 <- Data Hazzard											IF	S	ID	S	S	EX	WB
...																	
L_:																	

2) (40 pts) Same as 1) but now the processor supports forwarding on data hazards. Show the cycle by cycle execution.

Instr/Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Xor R4, R5, R9	IF	ID	EX	M	WB										
Add R1, R1, #4		IF	ID	EX	M	WB									
Sub R6, R5, R4			IF	ID	EX	M	WB								
BNE R1, R7, L_ <- Control Hazzard				IF	ID	EX	M	WB							
Ld R5, 52(R6)					S	S	IF	ID	EX	M	WB				
St R6, 8(R4)						S		IF	ID	EX	M	WB			
Sub R7, R5, R4									IF	ID	EX	M	WB		
Add R2, R5, R7										IF	ID	EX	M	WB	
...															
L_:															

3) (40 pts) Same as 2) but now assume a branch delay slot. Reorder instructions to reduce stalls on control hazards. Show the new code and its cycle by cycle execution.

Instr/Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13
Add R1, R1, #4	IF	ID	EX	M	WB								
BNE R1, R7, L_		IF	ID	EX	M	WB							
Xor R4, R5, R9			IF	ID	EX	M	WB						
Sub R6, R5, R4				IF	ID	EX	M	WB					
Ld R5, 52(R6)					IF	ID	EX	M	WB				
St R6, 8(R4)						IF	ID	EX	M	WB			
Sub R7, R5, R4							IF	ID	EX	M	WB		
Add R2, R5, R7								IF	ID	EX	M	WB	
...													
L_: