**Computer Systems Architecture**

**Homework 3**

**(Note TAs are still making a key, so they may make slight changes to this document.)**

**Memory Hierarchy**  
  
For all problems assume the address is 32bits.  
  
**Problem 1**a) What are the sizes of tag, index, and offset fields (in bits) for a cache of size 1MB,  
  a block size of 32 bytes, and 2-way associativity?  
Index size: 1MB = 2\*32\*S

S = 2^14

lg(S) = 14 bits

Offset: lg(32) = 5 bits

Tag: 32 – 5-14 = 13 bits

**Tag sizes**: 13bits

**Index sizes**: 14bits

**Offset sizes**: 5bits  
b) A 32KB cache has 16 byte blocks.  What is the associativity of this cache if the cache tag size is 19 bits?  
Offset: lg(16) = 4 bits  
Index: 32 –4-19=9bits

32KB=n\*2^9\*16

2^5\*2^10=2^9\*2^4\*n

n=2^2

n=4

**4 way associative**  
**Problem 2**  
What is the L2 hit time at which adding an L2 cache to the hierarchy is not profitable,   
given that an average L2 miss rate is 10%?

L1 miss penalty: m1  
L2 hit time: h2

L2 miss penalty: m2

L2 miss rate is 10%

To show that add an L2 cache to the hierarchy is not profitable means:

L1 miss penalty <= L2 hit time + (L2 miss penalty)\*(L2 miss rate)  
**m1 <= h2 + m2\*0.1**

**h2 >= m1 – m2\*0.1**

**Problem 3**  
Draw a detailed block diagram of a 24KB, 3-way set-associative cache with 32B blocks.  Show the size and widths of all the fields in the SRAM.

Index sizes :

24KB = 3\*32\*S

S = 2^8

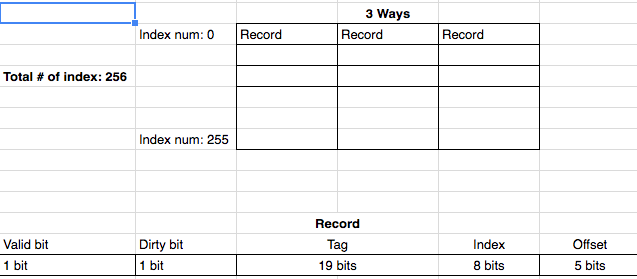
lg(2^8) = 8 bits

Offset sizes:

lg(32) = 5 bits

Tag sizes:

32 -5-8 = 19 bits

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***Figure 1 : Representation of 24KB, 3-way set-associative cache with 32B blocks***

**Problem 4**  
a) X% of the lines in a write-back, write-allocate L1 cache are modified.  What is the average memory latency (AMLAT) in this case assuming a one level of cache? A write-back has to be completed before a miss service can start. The average miss MR rate is over both reads and writes in this case.  
Assume

L1 hit time: h1

L1 Miss penalty: m1

Average memory latency means:

**With write back situation:**

**(L1 hit time) + 2\*(L1 Miss penalty)\*( L1 Miss ratio)**

When write back failed to find in cache, it should write the data back to the memory and load the data from memory to L1 cache.

**Without write back situation:**

**(L1 hit time) +** **L1 Miss penalty)\*( L1 Miss ratio)**

That is, the AMLAT is **(h1 + 2\*m1\*MR)\*X% + (h1 + m1\*MR)\*(1-X%)**

**h1 + m1\*MR + m1\*MR\*X%**

b) What is the effect of this cache on the CPI?

The CPI increase the amount of the miss in cache.

Assume Miss penalty cycles is m1

**Without X% write back:**

h1 + m1\*MR

h1 + m1\*MR + m1\*MR\*X% - h1 + m1\*MR = m1\*MR\*X%

**The amount of increase in CPI is m1\*MR\*X%**