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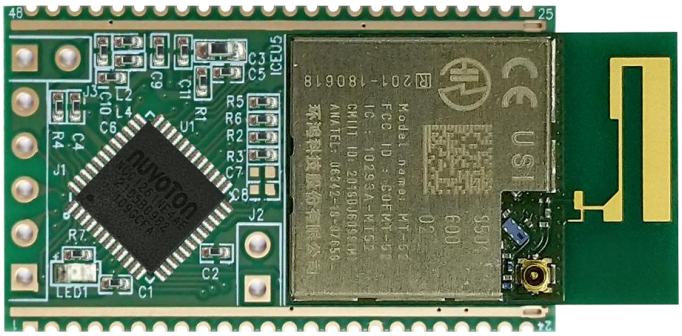
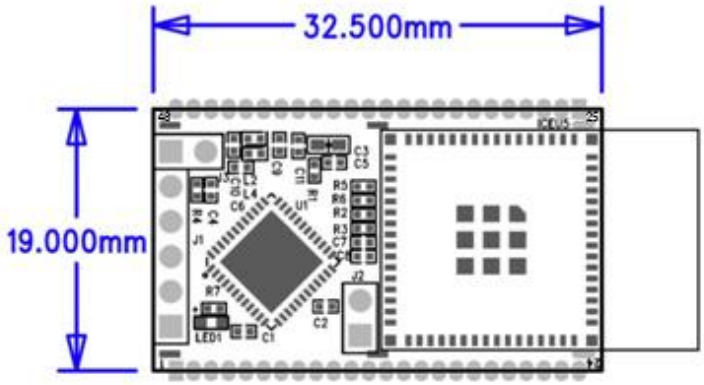
ITM-1261-ACK





802.11b/g/n + BT4.2 Alexa Connect Kit+ Nuvoton 72 MHz. Cortex®-M0 core

General Description

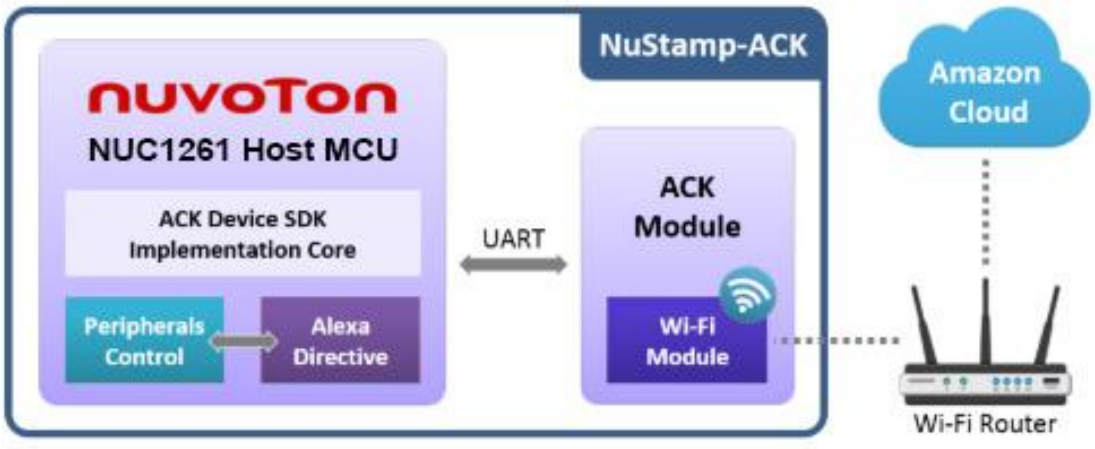
ITM-1261-ACK module is a highly integrated and low power consumption and compact size module supporting on-board Antenna Wireless LAN (WLAN 802.11 b/g/n) and Bluetooth Low Energy (BLE 4.2). With the preloaded firmware, it provides the ability to connect
with Alexa service.

ITM-1261-ACK consists of two key parts:

1. USI 802.11b/g/n + BT4.2 Alexa Connect Kit
2. Nuvoton 72 MHz. Cortex®-M0 core

The Alexa Connect Kit (ACK) is a way for device makers to connect devices to Alexa without worrying about managing cloud services, writing an Alexa skill, or developing complex networking and security firmware.
ACK enables device makers to make any device an Alexa-connected smart device. With ACK, you pay for the hardware module and a low, upfront fee that covers your ongoing use of the ACK cloud service. ACK enables you to turn the ongoing and variable cost of
managing your own cloud service into a fixed, one-time cost. ACK will also offer cloud extensibility options in addition to ACK cloud services for you to connect your
device to your own mobile applications, your own cloud service, and third-party cloud services such as IFTTT.
While you build and manage devices more quickly and economically, your customers enjoy Alexa control, Wi-Fi simple setup, and (optionally) the Dash Replenishment
Service.

The architecture of ITM-1261-ACK is shown as below.



Features

- Core
  - Arm® Cortex®-M0 core running up to 72 MHzFPU/DSP
  - One 24-bit system timer
  - Supports low power sleep
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports programmable mask-able interrupts
  - Serial Wire Debug supports with 2 watch-points / 4 breakpoints
  - Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
  - Supports 256/128 Kbytes application ROM (APROM)
  - Supports 4 Kbytes Flash for loader (LDROM)
  - Supports 2 Kbytes Security Protection Rom (SPROM)
  - Supports 12 bytes User Configuration block to control system initiation
  - Supports Data Flash with configurable memory size
  - Supports 2 Kbytes page erase for all embedded Flash
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded Flash memory
  - Supports CRC-32 checksum calculation function
  - Supports Flash all one verification function
  - Hardware external read protection of whole Flash memory by Security Lock Bit
  - Supports 2-wired ICP update through SWD/ICE interface
  - 20 Kbytes embedded SRAM
  - Supports byte-, half-word- and word-access

- Wi-Fi
  - Featuring integrated IEEE 802.11 b/g/n + BT4.2
  - Low power consumption and excellent power management performance which extends battery life
  - Small size suitable for low volume system integration
  - Three options for RF – LGA/IPEX SW23(w/o antenna) and onboard antenna(w antenna)
  - Lead Free design which supporting Green design requirement, RoHS Compliance Support 11n MCS7 HT20/HT40 Support antenna diversity Low power architecture and Tx/Rx for short range application @1.8V Low power beacon listen mode Low power Rx mode Very low power suspend mode (DLPS)

PDMA (Peripheral DMA)

– Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
– Supports single and burst transfer type
– Supports Normal and Scatter-Gather Transfer modes
– Supports two types of priorities modes: Fixed-priority and Round-robin modes
– Supports byte-, half-word- and word-access
– Supports incrementing mode for the source and destination address for each channel
– Supports time-out function for channel 0 and channel 1
– Supports software and SPI/I2S, UART, USCI, USB, ADC, PWM and TIMER request

Clock Control

– Built-in 22.1184 MHz high speed RC oscillator for system operation (Frequency variation < 2% at -40°C ~ +105°C)
– Built-in 48 MHz internal high speed RC oscillator for USB device operation
– Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
– Built-in 4~20 MHz high speed crystal oscillator for precise timing operation
– Built-in 32.768 kHz low speed crystal oscillator for Real Time Clock
– Supports PLL up to 144 MHz for high resolution PWM operation
– Supports dynamically calibrating the HIRC48 to 48 MHz ±0.25% by external 32.768 kHz crystal oscillator (LXT)
– Supports dynamically calibrating the HIRC to 22.1184 MHz by external 32.768 kHz crystal oscillator (LXT)
– Supports clock on-the-fly switch
– Supports clock failure detection for system clock
– Supports auto clock switch once clock failure detected
– Supports exception (NMI) generated once a clock failure detected
– Supports divided clock output

GPIO

– Four I/O modes
– TTL/Schmitt trigger input selectable
– I/O pin configured as interrupt source with edge/level trigger setting
– Supports high driver and high sink current I/O (up to 20 mA at 5 V)
– Supports software selectable slew rate control
– Supports up to 49/35 GPIOs for LQFP64/48 respectively
– Supports 5V-tolerance function for following pins

PA.0~PA.15, PB.12, PC.0~PC.7, PC.9~PC.14, PD.4~PD.7, PD.10~PD.15, PE.0~PE.1, PE.3~PE.13, PF.2, PF.7

Watchdog Timer

– Supports multiple clock sources from LIRC(default selection), HCLK/2048 and LXT
8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)

– Able to wake up from Power-down or Idle mode
– Interrupt or reset selectable on watchdog time-out

Window Watchdog Timer
– Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
Window set by 6-bit counter with 11-bit prescale
– Interrupt or reset selectable on time-out

RTC
– Supports separate battery power pin VBAT
– Supports software compensation by setting frequency compensate register (FCR)
– Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
– Supports Alarm registers (second, minute, hour, day, month, year)
– Supports Alarm mask registers
– Selectable 12-hour or 24-hour mode
– Automatic leap year recognition
– Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
– Supports wake-up function

PWM
– Supports maximum clock frequency up to144 MHz
– Supports up to two PWM modules, each module provides 6 output channels.
– Supports independent mode for PWM output/Capture input channel
– Supports complementary mode for 2 complementary paired PWM output channel

Dead-time insertion with 12-bit resolution

Two compared values during one period
– Supports 12-bit pre-scalar from 1 to 4096
– Supports 16-bit resolution PWM counter

Up, down and up/down counter operation type
– Supports mask function and tri-state enable for each PWM pin
– Supports brake function

Brake source from pin and system safety events: clock failed, Brown-out detection and CPU lockup.

Noise filter for brake source from pin

Edge detect brake source to control brake state until brake interrupt cleared

Level detect brake source to auto recover function after brake condition removed

– Supports interrupt on the following events:

PWM counter match zero, period value or compared value

Brake condition happened

– Supports trigger ADC on the following events:

PWM counter match zero, period value or compared value

– Supports up to 12 capture input channels with 16-bit resolution

– Supports rising or falling capture condition

– Supports input rising/falling capture interrupt

– Supports rising/falling capture with counter reload option

UART

– Supports up to 3 sets of UART

– Full-duplex asynchronous communications

– Separates receive and transmit 16/16 bytes entry FIFO for data payloads

– Supports hardware auto-flow control (RX, TX, CTS and RTS)

– Programmable receiver buffer trigger level

– Supports programmable baud rate generator for each channel individually

– Supports 8-bit receiver buffer time-out detection function

– Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])

– Supports Auto-Baud Rate measurement and baud rate compensation function

– Supports break error, frame error, parity error and receive/transmit buffer overflow detection function

– Fully programmable serial-interface characteristics

Programmable number of data bit, 5-, 6-, 7-, 8- bit character

Programmable parity bit, even, odd, no parity or stick parity bit generation and detection

Programmable stop bit, 1, 1.5, or 2 stop bit generation

– Supports IrDA SIR function mode

Supports for 3/16 bit duration for normal mode

– Supports LIN function mode

Supports LIN master/slave mode

Supports programmable break generation function for transmitter

Supports break detection function for receiver

– Supports RS-485 mode

Supports RS-485 9-bit mode

Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction

– Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function

– Supports PDMA transfer

I2C

– Supports up to two sets of I2C device
– Supports Master/Slave mode
– Supports bidirectional data transfer between masters and slaves
– Supports multi-master bus (no central master)
– Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
– Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
– Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
– Supports 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
– Programmable clocks allow versatile rate control
– Supports multiple address recognition, four slave address with mask option
– Supports two-level buffer function
– Supports setup/hold time programmable
– Supports wake-up function

USB 2.0 FS Device Controller

– Crystal-less USB 2.0 FS Device
– Compliant to USB specification version 2.0
– On-chip USB Transceiver
– Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
– Auto suspend function when no bus signaling for 3 ms
– Supports USB 2.0 Link Power Management (LPM)
– Provides 8 programmable endpoints
– Supports 512 Bytes internal SRAM as USB buffer
– Provides remote wake-up capability
– On-chip 5V to 3.3V LDO for USB PHY

ADC

– Supports 12-bit SAR ADC
– 12-bit resolution and 10-bit accuracy is guaranteed
– Analog input voltage range: 0~ AVDD
– Supports external VREF pin
– Up to 15 single-end analog input channels
– Maximum ADC peripheral clock frequency is 16 MHz
– Conversion rate up to 800 ksps at 5 V
– Configurable ADC internal sampling time

– Supports single-scan, single-cycle-scan, and continuous scan and scan on enabled channels
– Supports individual conversion result register with valid and overrun indicators for each channel
– Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting
– An A/D conversion can be triggered by:
    Software enable
    External pin (STADC)
    Timer 0~3 overflow pulse trigger
    PWM triggers with optional start delay period
– Supports 4 internal channels for
    Operational amplifier output
    Band-gap VBG input
    Temperature sensor input
    VBAT voltage measure
– Supports internal reference voltage: 2.048 V, 2.560 V, 3.072 V and 4.096 V
– Supports PDMA transfer

Analog Comparator
– Supports up to 2 rail-to-rail analog comparators
– Supports 4 multiplexed I/O pins at positive node.
– Supports I/O pin and internal voltages at negative node
– Support selectable internal voltage reference from:
    Band-gap VBG
    Voltage divider source from AVDD and internal reference voltage.
– Supports programmable hysteresis
– Supports programmable speed and power consumption
– Interrupts generated when compare results change, interrupt event condition is programmable.
– Supports power-down wake-up
– Supports triggers for break events and cycle-by-cycle control for PWM

Cyclic Redundancy Calculation Unit
– Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
– Programmable initial value
– Supports programmable order reverse setting for input data and CRC checksum
– Supports programmable 1’s complement setting for input data and CRC checksum.
– Supports 8/16/32-bit of data width
– Interrupt generated once checksum error occurs

User Configurable VDDIO=1.8 ~ 5.5 V I/O Interface
– Supports UART, SPI and I2C at PE.8~PE.13

Supports 96-bit Unique ID (UID)

Supports 128-bit Unique Customer ID (UCID)

One built-in temperature sensor with 1°C resolution

Brown-out detector

– With 4 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V

– Supports Brown-out Interrupt and Reset option

Low Voltage Reset

– Threshold voltage levels: 2.0 V

Power consumption

– Chip power down current < 10 uA with RAM data retention.

– VBAT power domain operating current <1.5 uA

Operating Temperature: -40°C~105°C

Packages

– All Green package (RoHS)

– LQFP 64-pin (7x7mm)

– LQFP 48-pin (7x7mm)

– QFN 48-pin (7x7mm)

Interface Definition

Flash (Kbytes)	SRAM (Kbytes)	Data Flash (Kbytes)	SPROM (Kbytes)	ISP ROM (Kbytes)	I/O	Timer/PWM	PWM	USBD	Connectivity				ADC(12-Bit)	ACMP	PDMA	V_{BAT} (RTC)	V_{DDIO}	EBI	ICP/IAP/ISP
									USCI*	UART	SPI/I2S	I2C							
128	20	Conf*	2	4	35	4	10	1	3	3	2	2	9-ch	2	5	V	V	V	V

NO	Name	Type	Description
1	PB.5	I/O	Multi-function I/O pin (see Appendix for more detail)
2	PB.6	I/O	Multi-function I/O pin (see Appendix for more detail)
3	PB.7	I/O	Multi-function I/O pin (see Appendix for more detail)
4	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
5	PD.0	I/O	Multi-function I/O pin (see Appendix for more detail)
6	AGND	P/G	Ground pin for analog circuit
7	PD.1	I/O	Multi-function I/O pin (see Appendix for more detail)
8	PD.2	I/O	Multi-function I/O pin (see Appendix for more detail)
9	PD.3	I/O	Multi-function I/O pin (see Appendix for more detail)
10	VDD	P	3.3V Power supply
11	PF.0	I/O	Multi-function I/O pin (see Appendix for more detail)
12	PF.1	I/O	Multi-function I/O pin (see Appendix for more detail)
13	PF.2	I/O	Multi-function I/O pin (see Appendix for more detail)
14	PD.7	I/O	Multi-function I/O pin (see Appendix for more detail)
15	PF.3	I/O	Multi-function I/O pin (see Appendix for more detail)
16	PF.4	I/O	Multi-function I/O pin (see Appendix for more detail)
17	GND	G	Ground pin for digital circuit
18	LDO_CAP	—	Not connected (LDO Output Pin)
19	PC.0	I/O	Multi-function I/O (see Appendix for more detail)
20	HOST_INT_B	I/O	For module internal usage; Not connected

21	UART_NT_WR	I/O	For module internal usage; Not connected
22	UART_NR_WT	I/O	For module internal usage; Not connected
23	PC.4	I/O	Multi-function I/O pin (see Appendix for more detail)
24	RESET_B	I/O	For module internal usage; Not connected
25	ICE_CLK	I/O	Serial wired debugger clock pin.
26	ICE_DAT	I/O	Serial wired debugger data pin.
27	PE.10	I/O	Multi-function I/O pin (see Appendix for more detail)
28	PE.11	I/O	Multi-function I/O pin (see Appendix for more detail)
29	I2C0_CLK	I/O	For module internal usage; Not connected
30	I2C0_SDA	I/O	For module internal usage; Not connected
31	VDD	P	3.3V power supply
32	USB_VBUS	P	USB power supply from host or hub
33	USB_D-	A	USB differential signal D-
34	USB_D+	A	USB differential signal D+
35	PWR_EN	I/O	For module internal usage; Not connected
36	USB_3V3_CAP	A	For module internal usage; Not connected
37	U0_RX	I/O	UART0 data receiver input pin
38	U0_TX	I/O	UART0 data transmitter output pin
39	PA.1	I/O	Multi-function I/O pin (see Appendix for more detail)
40	PA.0	I/O	Multi-function I/O pin (see Appendix for more detail)
41	VDD	P	3.3V power supply
42	AVDD	P	3.3V power supply for analog circuit
43	AVDD	P	3.3V power supply for analog circuit
44	PB.0	I/O	Multi-function I/O pin (see Appendix for more detail)
45	PB.1	I/O	Multi-function I/O pin (see Appendix for more detail)
46	PB.2	I/O	Multi-function I/O pin (see Appendix for more detail)
47	RESTORE_SET	I/O	For module internal usage; Not connected
48	PB.4	I/O	Multi-function I/O pin (see Appendix for more detail)

Appendix: Interface function detail

48	Pin Name	Type	MFP	Description
1	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
	SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
	SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
	ACMP0_P2	A	MFP5	Analog comparator 0 positive input 2 pin.
	EBI_AD6	I/O	MFP7	EBI address/data bus bit 6.
	UART2_RXD	I	MFP9	UART2 data receiver input pin.
2	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
	SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
	SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
	ACMP0_P1	A	MFP5	Analog comparator 0 positive input 1 pin.
	EBI_AD5	I/O	MFP7	EBI address/data bus bit 5.
3	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
	SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
	SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
	USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
	ACMP0_P0	A	MFP5	Analog comparator 0 positive input 0 pin.
	EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
4	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
5	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP1	SPI0 I_2S master clock output pin

48	Pin Name	Type	MFP	Description
6	AV_{SS}	P	MFP0	Ground pin for analog circuit.
7	PD.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH19	A	MFP1	ADC0 channel 19 analog input.
	PWM0_SYNC_IN	I	MFP2	PWM0 counter synchronous trigger input pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	USCI2_CLK	I/O	MFP4	USCI2 clock pin.
	ACMP1_P2	A	MFP5	Analog comparator 1 positive input 2 pin.
	TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
	EBI_nRD	O	MFP7	EBI read enable output pin.
8	PD.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_ST	I	MFP1	ADC0 external trigger input pin.
	TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
	USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
	ACMP1_P1	A	MFP5	Analog comparator 1 positive input 1 pin.
	PWM0_BRAKE0	I	MFP6	PWM0 Brake 0 input pin.
	EBI_nWR	O	MFP7	EBI write enable output pin.

48	Pin Name	Type	MFP	Description
	INT0	I	MFP8	External interrupt 0 input pin.
9	PD.3	I/O	MFP0	General purpose digital I/O pin.
	TM2	I/O	MFP1	Timer2 event counter input/toggle output pin.
	SPI0_I2SMCLK	I/O	MFP2	SPI0 I_2S master clock output pin
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
	USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
	ACMP1_P0	A	MFP5	Analog comparator 1 positive input 0 pin.
	PWM0_BRAKE1	I	MFP6	PWM0 Brake 1 input pin.
	EBI_MCLK	O	MFP7	EBI external clock output pin.
	INT1	I	MFP8	External interrupt 1 input pin.
10	V_{BAT}	P	MFP0	Power supply by batteries for RTC.
11	PF.0	I/O	MFP0	General purpose digital I/O pin.
	X32_OUT	O	MFP1	External 32.768 kHz crystal output pin.
	USCI2_CTL1	I/O	MFP5	USCI2 control 1 pin.
	INT5	I	MFP8	External interrupt 5 input pin.
12	PF.1	I/O	MFP0	General purpose digital I/O pin.
	X32_IN	I	MFP1	External 32.768 kHz crystal input pin.
	USCI2_CTL0	I/O	MFP5	USCI2 control 0 pin.
	PWM1_BRAKE0	I	MFP6	PWM1 Brake 0 input pin.
13	PF.2	I/O	MFP0	General purpose digital I/O pin.
	USCI2_CLK	I/O	MFP5	USCI2 clock pin.
	PWM1_BRAKE1	I	MFP6	PWM1 Brake 1 input pin.

48	Pin Name	Type	MFP	Description
14	PD.7	I/O	MFP0	General purpose digital I/O pin.
	USCI1_CTL1	I/O	MFP1	USCI1 control 1 pin.
	SPI0_I2SMCLK	I/O	MFP2	SPI0 I^2S master clock output pin
	PWM0_SYNC_IN	I	MFP3	PWM0 counter synchronous trigger input pin.
	TM1	I/O	MFP4	Timer1 event counter input/toggle output pin.
	ACMP0_O	O	MFP5	Analog comparator 0 output pin.
	PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
	EBI_nRD	O	MFP7	EBI read enable output pin.
15	PF.3	I/O	MFP0	General purpose digital I/O pin.
	XT1_OUT	O	MFP1	External 4~20 MHz (high speed) crystal output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
16	PF.4	I/O	MFP0	General purpose digital I/O pin.
	XT1_IN	I	MFP1	External 4~20 MHz (high speed) crystal input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
17	V_{SS}	P	MFP0	Ground pin for digital circuit.
	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital
18	LDO_CAP	A	MFP0	LDO output pin.
19	PC.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
	UART2_nCTS	I	MFP3	UART2 clear to Send input pin.
	USCI0_DAT0	I/O	MFP4	USCI0 data 0 pin.

48	Pin Name	Type	MFP	Description
20	PC.1	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	UART2_nRTS	O	MFP3	UART2 request to Send output pin.
	USCI0_DAT1	I/O	MFP4	USCI0 data 1 pin.
	ACMP1_WLAT	I	MFP5	Analog comparator 1 window latch input pin
	PWM0_CH1	I/O	MFP6	PWM0 channel 1 output/capture input.
	EBI_AD9	I/O	MFP7	EBI address/data bus bit 9.
21	PC.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP2	SPI0 slave select pin.
	UART2_TXD	O	MFP3	UART2 data transmitter output pin.
	USCI0_CTL1	I/O	MFP4	USCI0 control 1 pin.
	ACMP1_O	O	MFP5	Analog comparator 1 output pin.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	EBI_AD10	I/O	MFP7	EBI address/data bus bit 10.
22	PC.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
	UART2_RXD	I	MFP3	UART2 data receiver input pin.
	USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	EBI_AD11	I/O	MFP7	EBI address/data bus bit 11.
23	PC.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	USCI0_CLK	I/O	MFP5	USCI0 clock pin.
	PWM0_CH4	I/O	MFP6	PWM0 channel 4 output/capture input.
	EBI_AD12	I/O	MFP7	EBI address/data bus bit 12.
24	PE.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	TM2_EXT	I/O	MFP4	Timer2 external capture input/toggle output pin.

48	Pin Name	Type	MFP	Description
25	PE.6	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MFP1	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on
	I2C0_SCL	I/O	MFP2	I2C0 clock pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
26	PE.7	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	O	MFP1	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.

48	Pin Name	Type	MFP	Description
32	USB_VBUS	P	MFP0	Power supply from USB host or HUB.
33	USB_D-	A	MFP0	USB differential signal D-.
34	USB_D+	A	MFP0	USB differential signal D+.
35	PF.7	I/O	MFP0	General purpose digital I/O pin.
36	USB_V_{DD}33_CAP	A	MFP0	Internal power regulator output 3.3V decoupling pin.
	PB.12	I/O	MFP0	General purpose digital I/O pin.
	PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
37	PA.3	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	UART0_nRTS	O	MFP3	UART0 request to Send output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
	EBI_AD3	I/O	MFP7	EBI address/data bus bit 3.
	USCI1_CLK	I/O	MFP8	USCI1 clock pin.
38	PA.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.
	EBI_AD2	I/O	MFP7	EBI address/data bus bit 2.
	USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
39	PA.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_nRTS	O	MFP1	UART1 request to Send output pin.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	USCI1_CTL1	I/O	MFP4	USCI1 control 1 pin.
	PWM1_CH4	I/O	MFP6	PWM1 channel 4 output/capture input.
	EBI_AD1	I/O	MFP7	EBI address/data bus bit 1.
40	PA.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_nCTS	I	MFP1	UART1 clear to Send input pin.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
	PWM1_CH5	I/O	MFP6	PWM1 channel 5 output/capture input.
	EBI_AD0	I/O	MFP7	EBI address/data bus bit 0.
	INT0	I	MFP8	External interrupt 0 input pin.

48	Pin Name	Type	MFP	Description
	V_{SS}	P	MFP0	Ground pin for digital circuit.
41	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital
42	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
43	V_{REF}	A	MFP0	ADC reference voltage input.
44	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
	VDET_P0	A	MFP2	Voltage detector positive input 0 pin.
	UART2_RXD	I	MFP3	UART2 data receiver input pin.
	TM2	I/O	MFP4	Timer2 event counter input/toggle output pin.
	USCI1_DAT0	I/O	MFP6	USCI1 data 0 pin.
	EBI_nWRL	O	MFP7	EBI low byte write enable output pin.
	INT1	I	MFP8	External interrupt 1 input pin.
	TM1_EXT	I/O	MFP10	Timer1 external capture input/toggle output pin.
45	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
	VDET_P1	A	MFP2	Voltage detector positive input 1 pin.
	UART2_TXD	O	MFP3	UART2 data transmitter output pin.
	TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
	PWM0_SYNC_OUT	O	MFP6	PWM0 counter synchronous trigger output pin.
	EBI_nWRH	O	MFP7	EBI high byte write enable output pin
	USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
46	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
	SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
	SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
	UART1_RXD	I	MFP4	UART1 data receiver input pin.
	TM_BRAKE0	I	MFP6	TM_BRAKE0 I Timer Brake * input pin.
	EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
	USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
	TM2_EXT	I/O	MFP10	Timer2 external capture input/toggle output pin.
47	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
	SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.

48	Pin Name	Type	MFP	Description
	SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
	UART1_TXD	O	MFP4	UART1 data transmitter output pin.
	TM_BRAKE1	I	MFP6	TM_BRAKE1 I Timer Brake * input pin.
	EBI_ALE	O	MFP7	EBI address latch enable output pin.
	USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
	TM0_EXT	I/O	MFP10	Timer0 external capture input/toggle output pin.
48	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
	SPI0_SS	I/O	MFP2	SPI0 slave select pin.
	SPI1_SS	I/O	MFP3	SPI1 slave select pin.
	UART1_nCTS	I	MFP4	UART1 clear to Send input pin.
	ACMP0_N	A	MFP5	Analog comparator 0 negative input pin.
	EBI_AD7	I/O	MFP7	EBI address/data bus bit 7.
	USCI0_CTL1	I/O	MFP8	USCI0 control 1 pin.
	UART2_RXD	I	MFP9	UART2 data receiver input pin.
	TM1_EXT	I/O	MFP10	Timer1 external capture input/toggle output pin.