Labs 5 and 6: Latches, Flip-flops, and Synchronous Counters

ITI1100 A — Digital Systems I

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Lab 5: Latches and Flip-flops

Objectives

- Provide insight into the characteristics of several important latches and flip-flops.
- Build latches and flip-flops from basic gates.
- Explain concepts of latching and edge-triggering.
- Test latches and flip-flops to understand their operation.

Equipment and Components

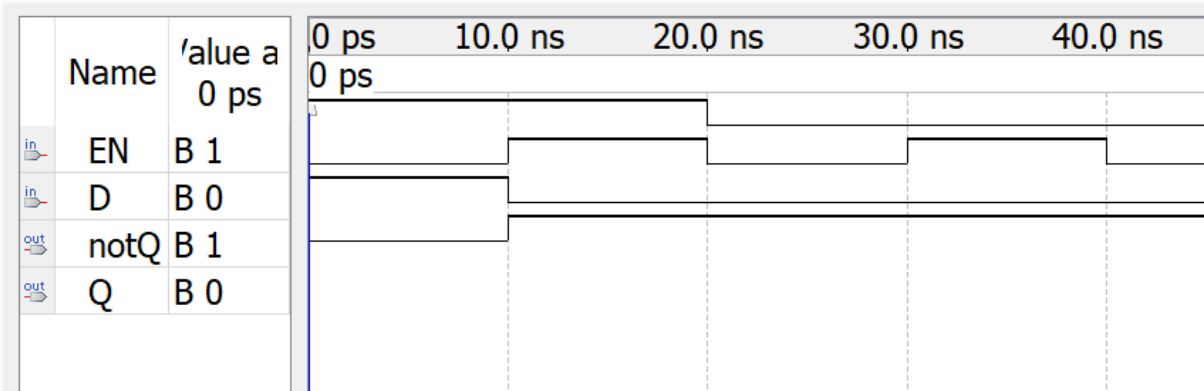- Quartus 11 13.0 Service Pack 1 (Local)
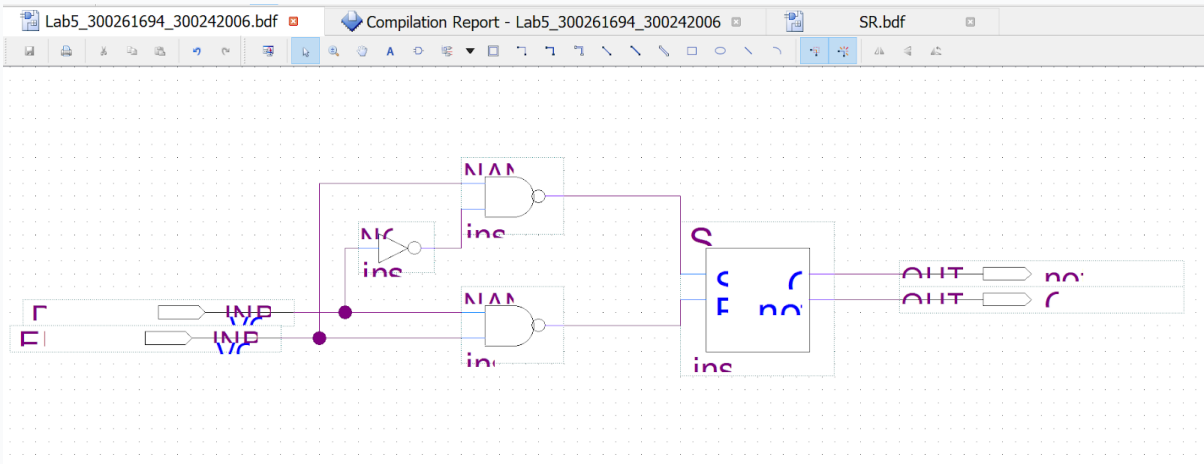
Part I — SR Latch
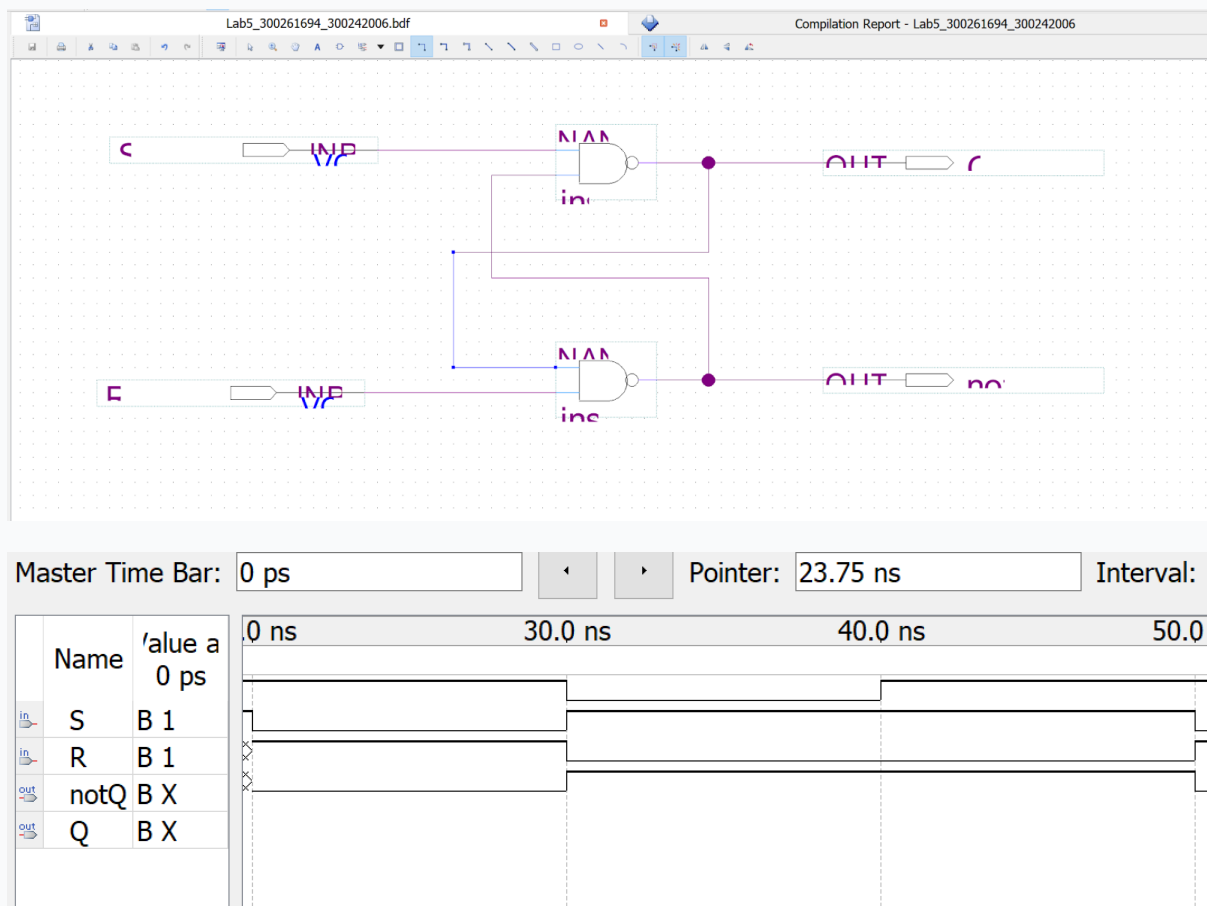
Experimental Function Table

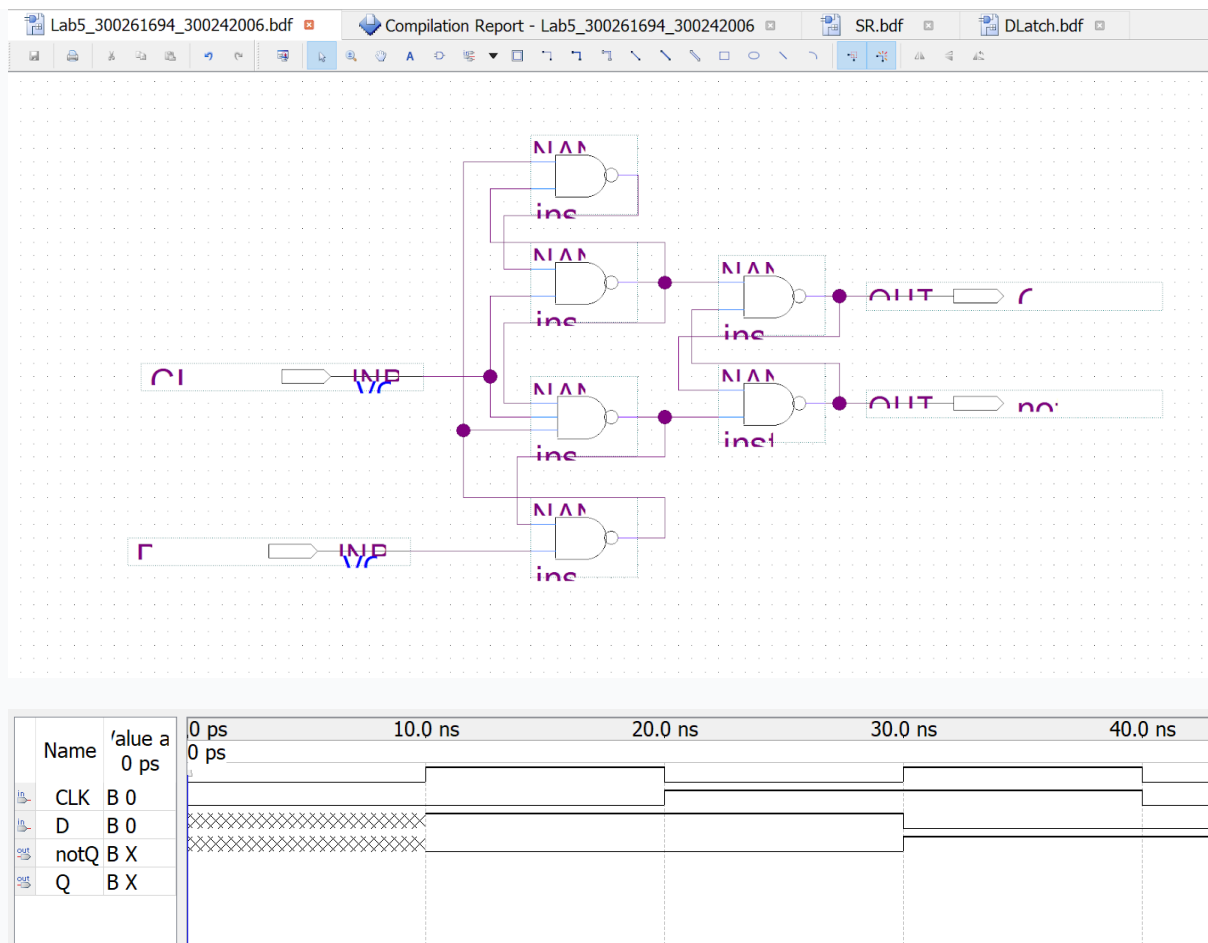| S	R	Q_t	Q_{t+1}
1	1	$\times$	Q_t
1	0	$\times$	0
0	1	$\times$	1
0	0	$\times$	$\times$

Comparison of Expected and Experimental Data

Experimental data is identical to expected data.

Part II — D Latch
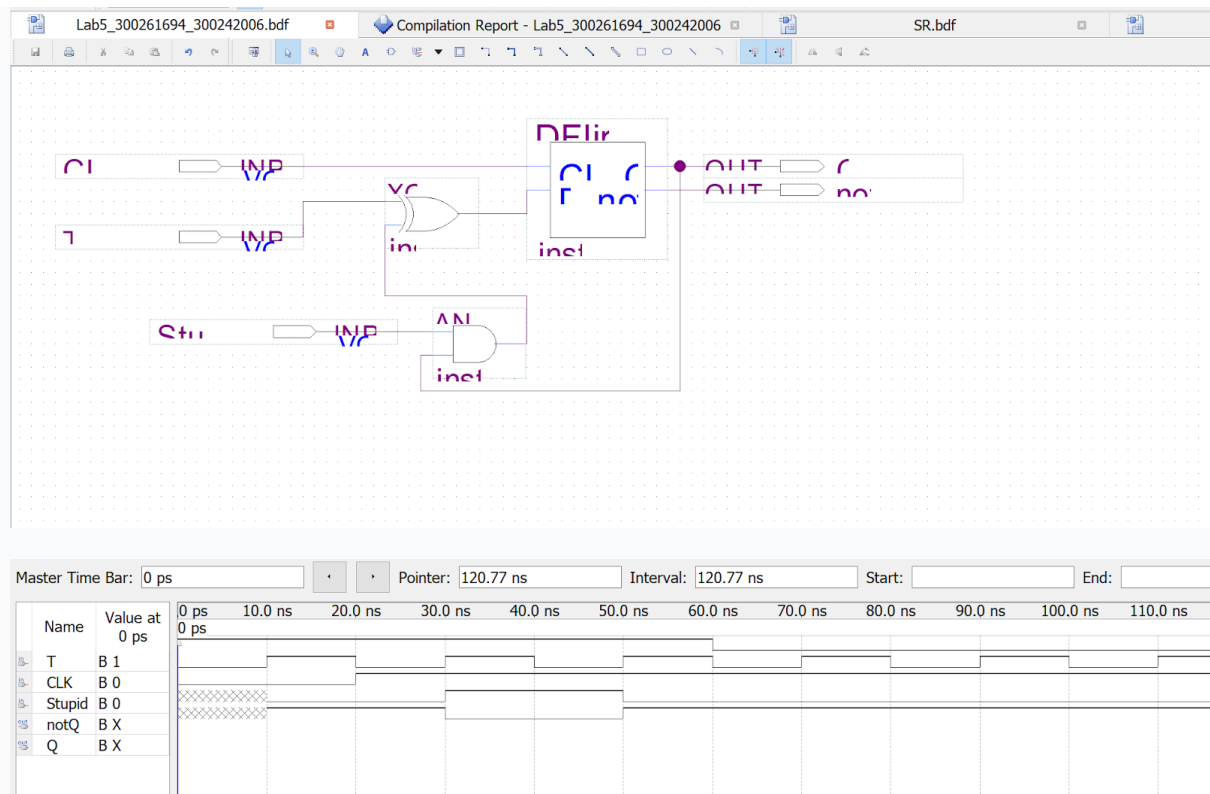

Part III — D Flip-Flop

Experimental Function Table

CLK	D	Q_{t+1}	$\overline{Q_{t+1}}$
↑	0	0	1
↑	1	1	0
0	×	Q_t	$\overline{Q_t}$
1	×	Q_t	$\overline{Q_t}$

Comparison of Expected and Experimental Data

Experimental data is identical to expected data.

Part IV — T Flip-Flop

Experimental Function Table

CLK	D	Q_{t+1}	$\overline{Q_{t+1}}$
$\uparrow$	0	Q_t	$\overline{Q_t}$
$\uparrow$	1	$\overline{Q_t}$	Q_t
0	$\times$	Q_t	$\overline{Q_t}$
1	$\times$	Q_t	$\overline{Q_t}$

Comparison of Expected and Experimental Data

Experimental data is identical to expected data.

Discussion and Conclusion

In this laboratory, we created several logic circuits using Quartus. We then analysed the circuits to predict their operation. Finally, we simulated the circuits to make sure our theoretical predictions were the same as the experimental results.

The experimental and expected data matched completely. We met the objectives of building latches and flip-flops from basic gates, and testing the latches and the flip-flops to understand their operation by creating and testing the following:

- SR Latch
- D Latch
- D Flip-Flop
- T Flip-Flop

Challenges

- We had to use an outdated version of Quartus for the labs, which often breaks for no apparent reason. The errors we received were unrelated to the actual issues in our circuits, making debugging very annoying.
- We had to use a manual reset signal for **Part III** as Quartus would set all outputs to `undefined` otherwise.
- It was unclear whether the gates used had to be active high or active low.
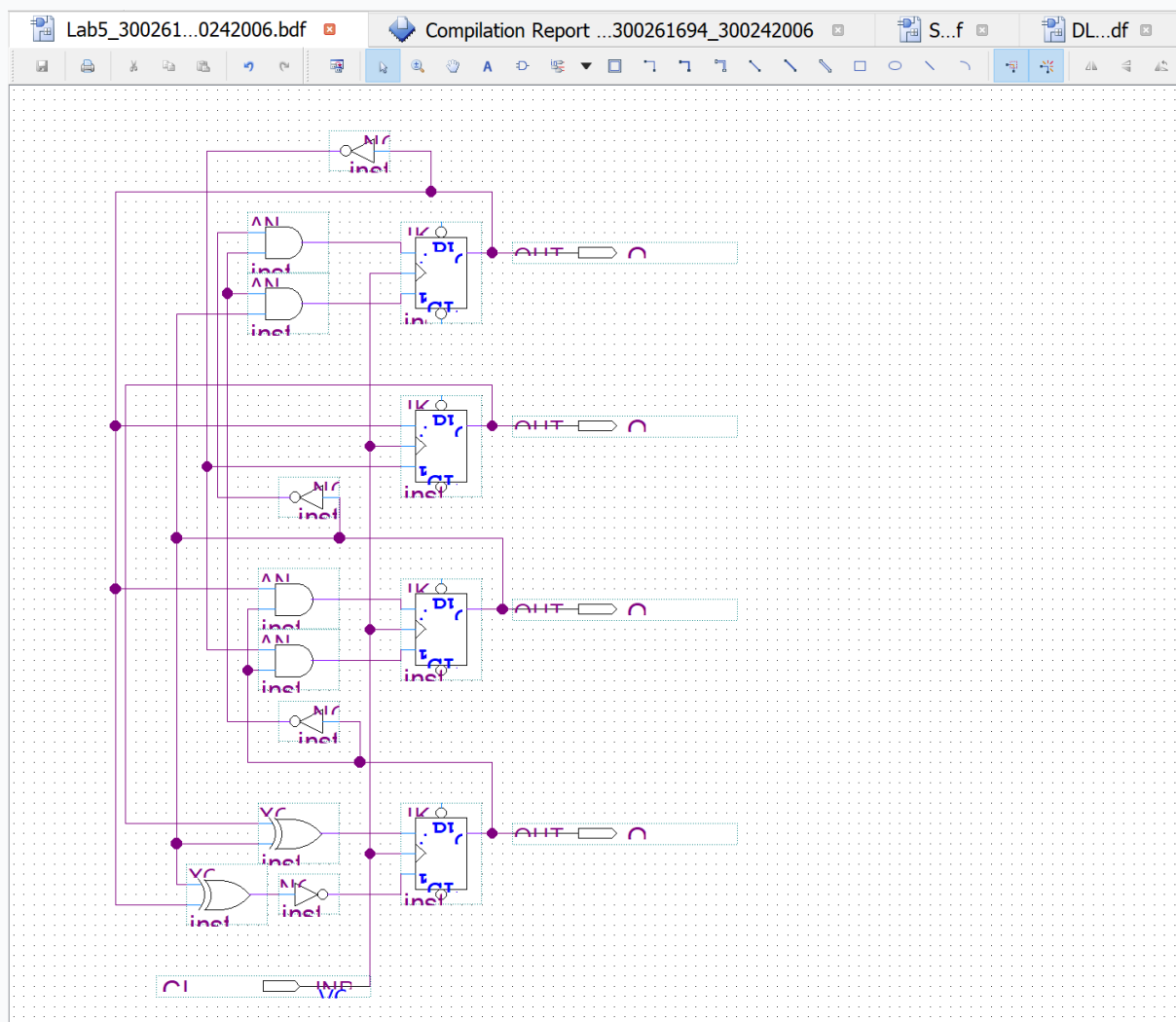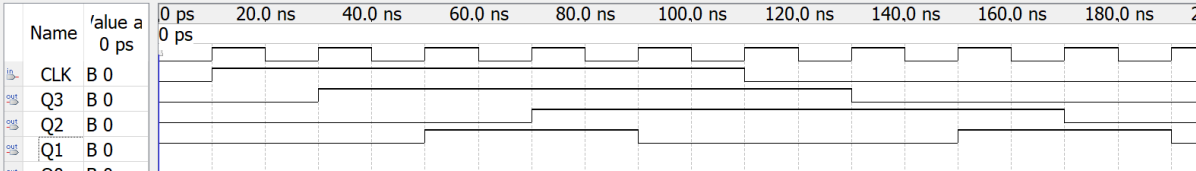
Lab 6: Synchronous Counters

Objectives

- Design synchronous counters
- Simulate the functions of the various counters in this laboratory exercise

Equipment and Components

- Quartus 11 13.0 Service Pack 1 (Local)

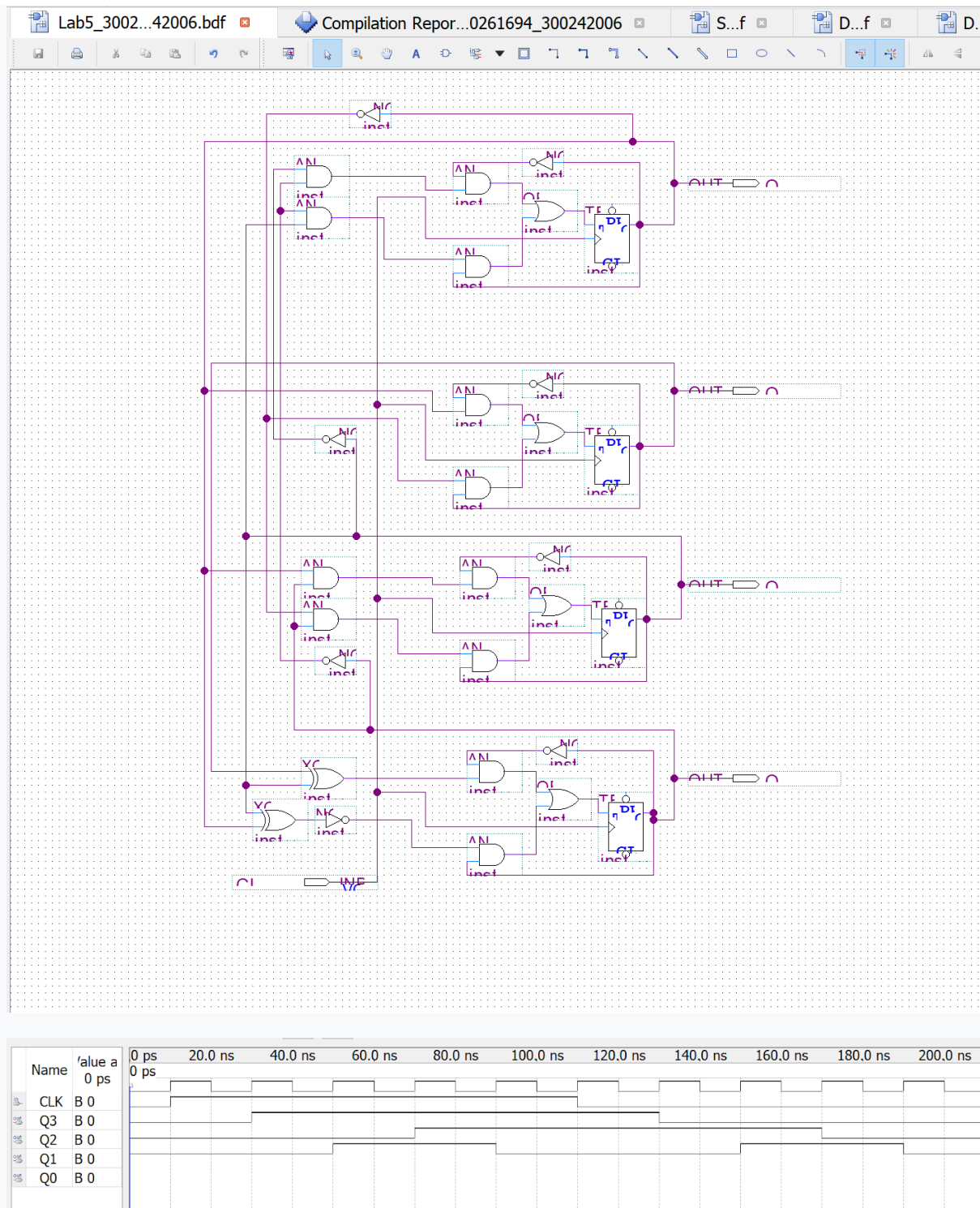## Part I

Experimental Function Table

CLK	Q_t	Q_{t+1}
↑	0	8
↑	8	12
↑	12	13
↑	13	15
↑	15	14
↑	14	6
↑	6	2
↑	2	3
↑	3	1
↑	1	0
0	×	Q_t
1	×	Q_t

Comparison of Expected and Experimental Data

Experimental data is identical to expected data.

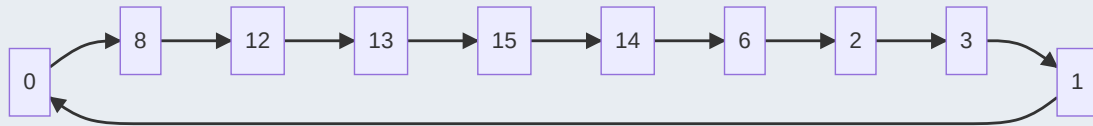# Part II

Comparison of Expected and Experimental Data

Experimental data is identical to expected data.

Discussion and Conclusion

In this laboratory, we created several logic circuits using Quartus. We then analysed the circuits to predict their operation. Finally, we simulated the circuits

to make sure our theoretical predictions were the same as the experimental results.

The experimental and expected data matched completely. We met the objectives of designing synchromous counters and simulating the functions of the various counters by designing counters iterating through the following numbers:

Challenges

- We had to use an outdated version of Quartus for the labs, which often breaks for no apparent reason. The errors we received were unrelated to the actual issues in our circuits, making debugging very annoying.