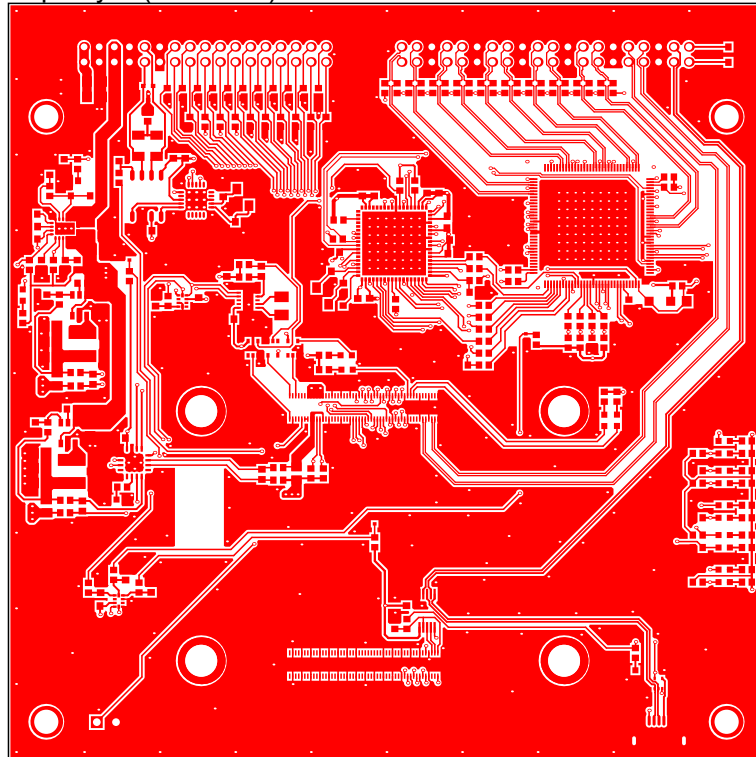


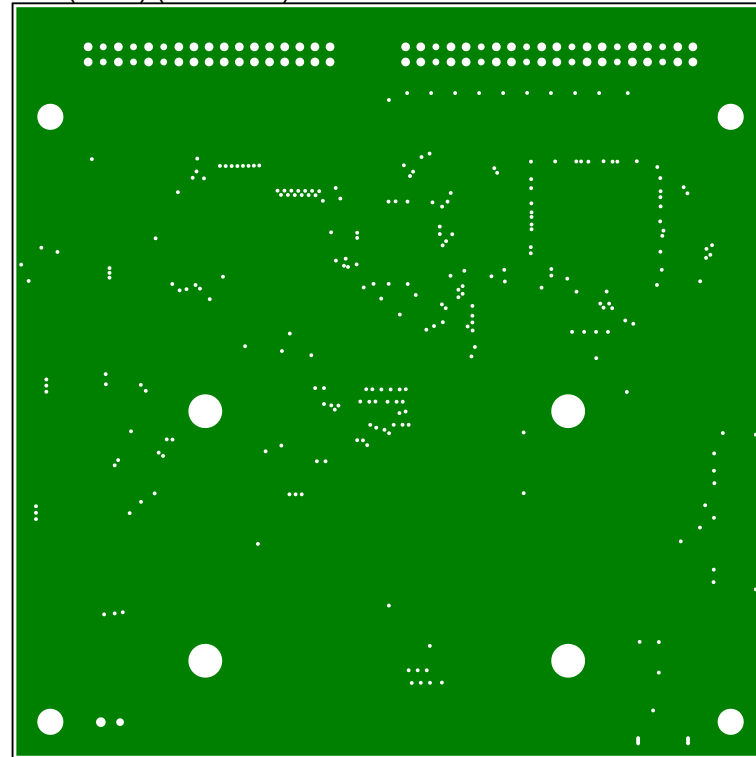
Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
☆	130	0.20mm	Plated	None
⊕	529	0.25mm	Plated	None
☆	9	0.30mm	Plated	None
◇	2	0.50mm	Plated	None
□	74	0.90mm	Plated	+/-0.05mm
○	2	1.02mm	Plated	None
⊗	4	3.20mm	Plated	None
◆	4	4.22mm	Plated	None
754 Total				

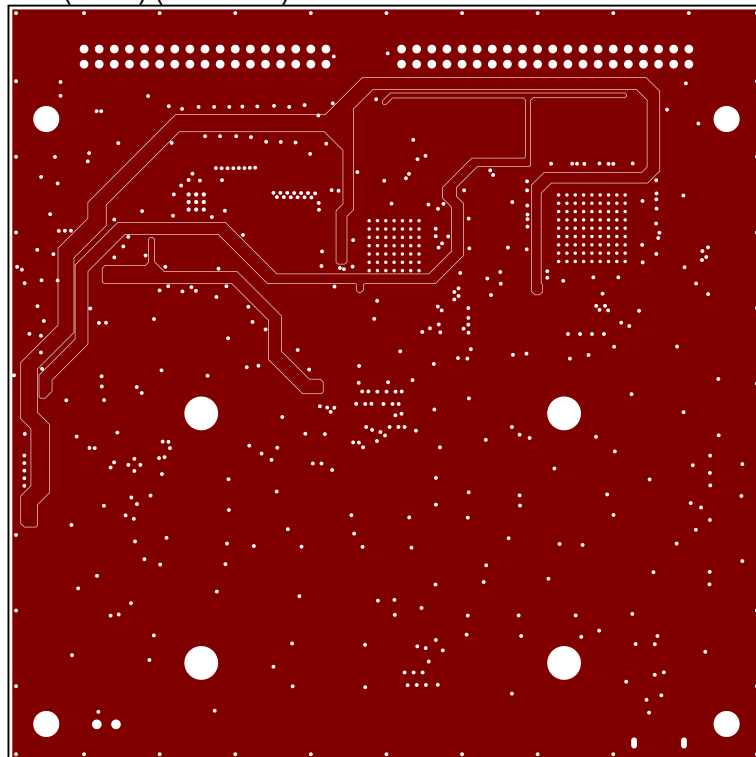
Top Layer (Scale 1:1)



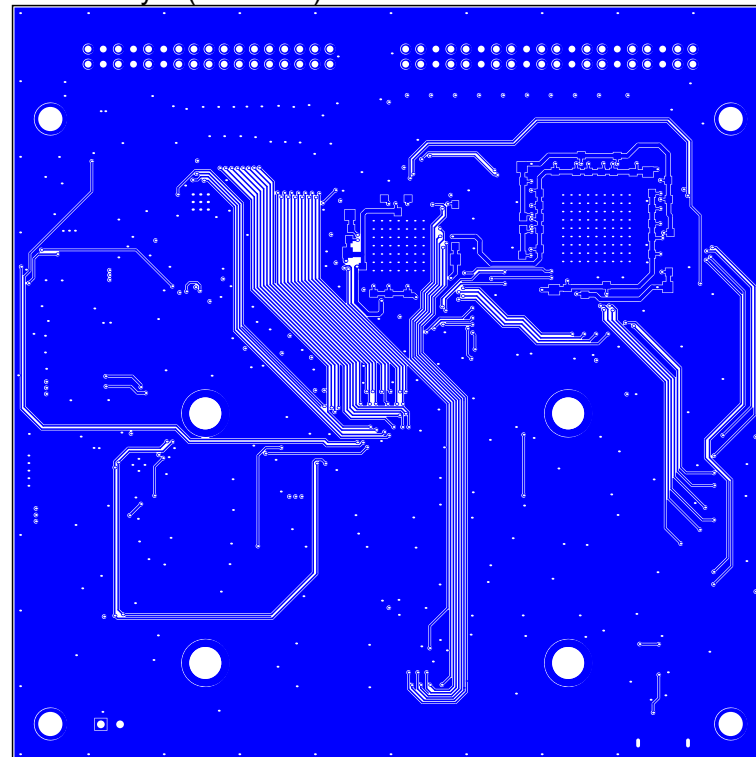
Int1 (GND) (Scale 1:1)



Int2 (PWR) (Scale 1:1)



Bottom Layer (Scale 1:1)



Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers	Substack
1	Edge-Coupled Coated Microstrip	100	100.03	Top Layer	0.17mm	0.17mm	0.13mm	Int1 (GND)	Board Layer Stack
2	Edge-Coupled Coated Microstrip	90	89.98	Top Layer	0.24mm	0.24mm	0.13mm	Int1 (GND)	Board Layer Stack
3	Edge-Coupled Coated Microstrip	100	100.03	Bottom Layer	0.17mm	0.17mm	0.13mm	Int2 (PWR)	Board Layer Stack
4	Edge-Coupled Coated Microstrip	90	89.98	Bottom Layer	0.24mm	0.24mm	0.13mm	Int2 (PWR)	Board Layer Stack

Layer Stack Legend

