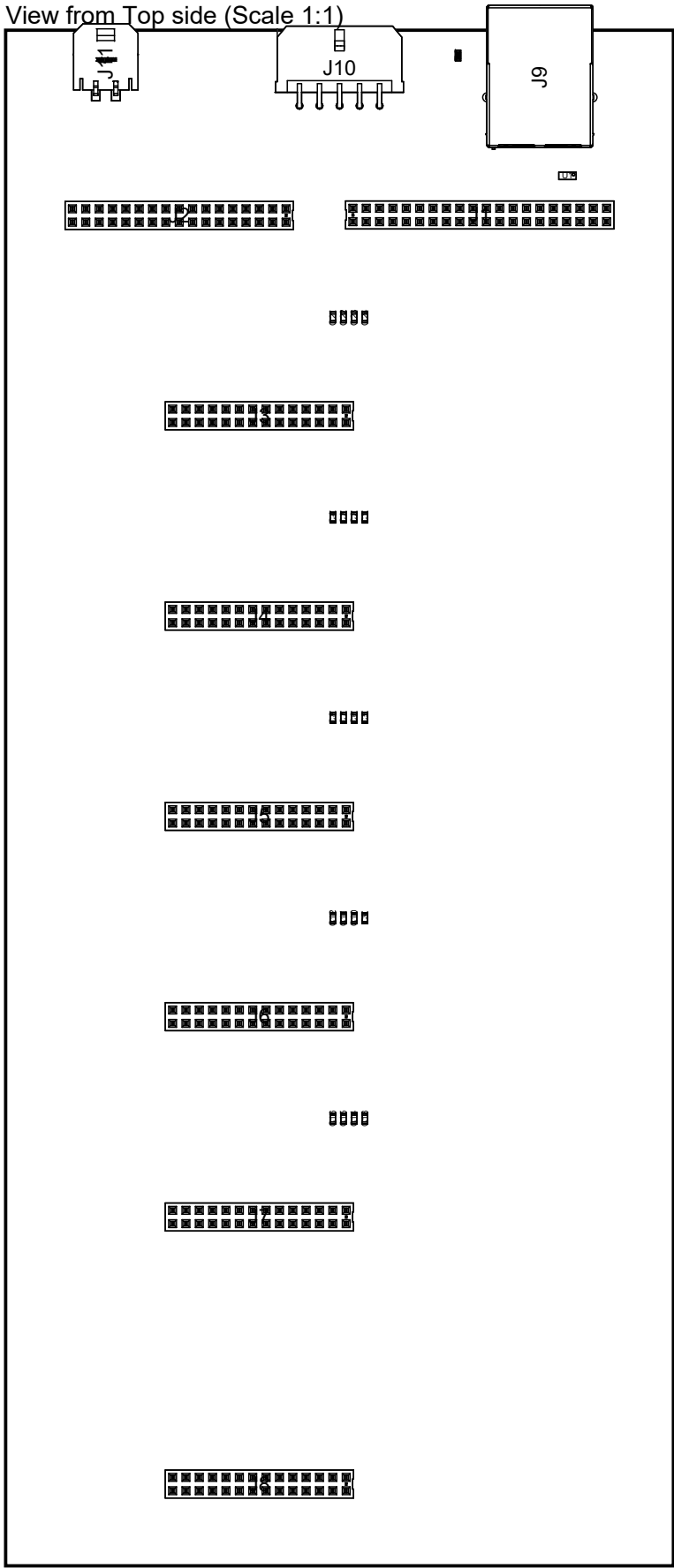
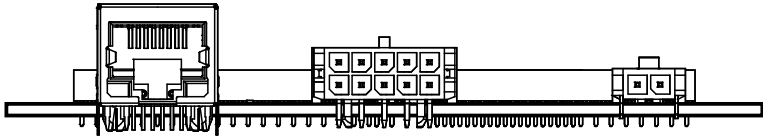


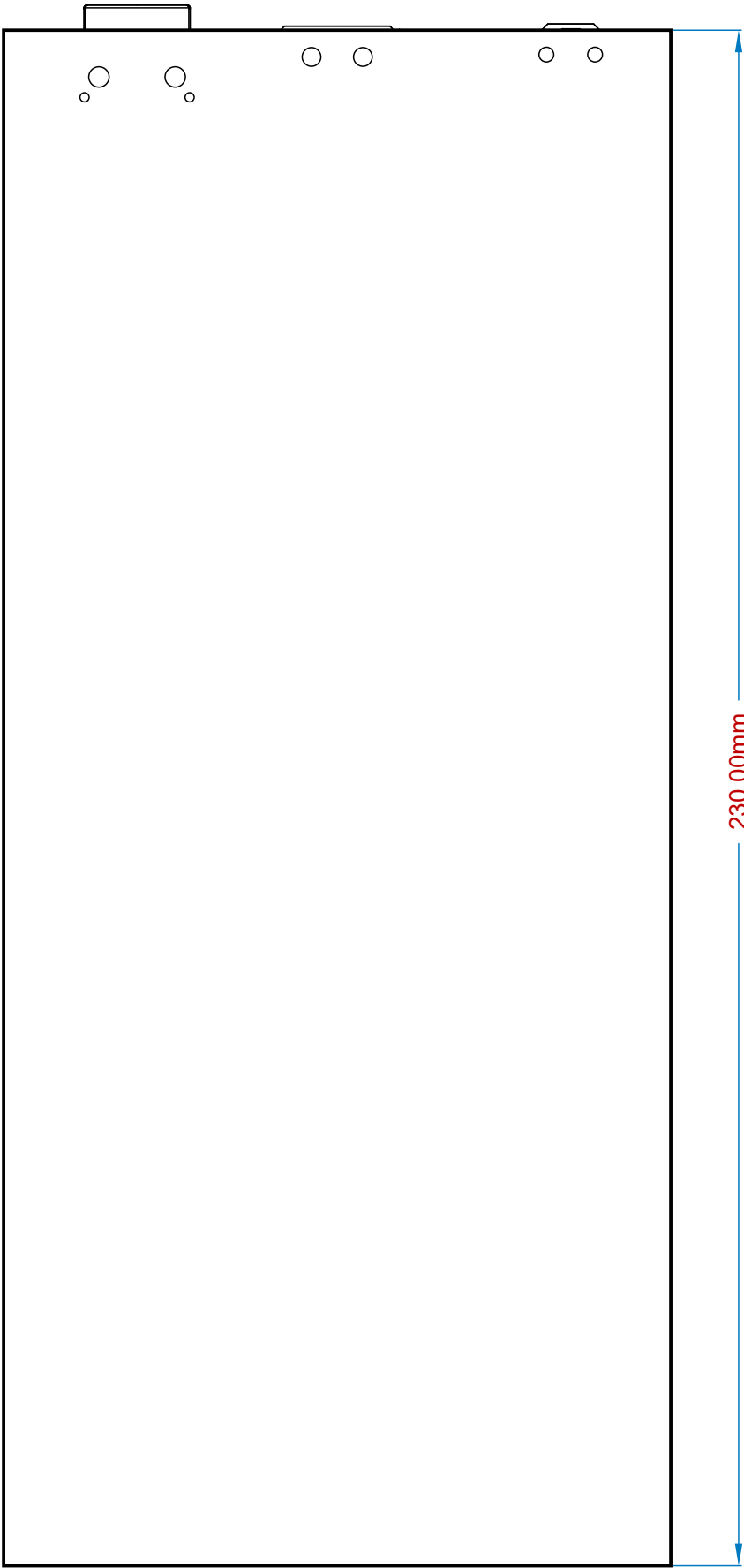
View from Top side (Scale 1:1)



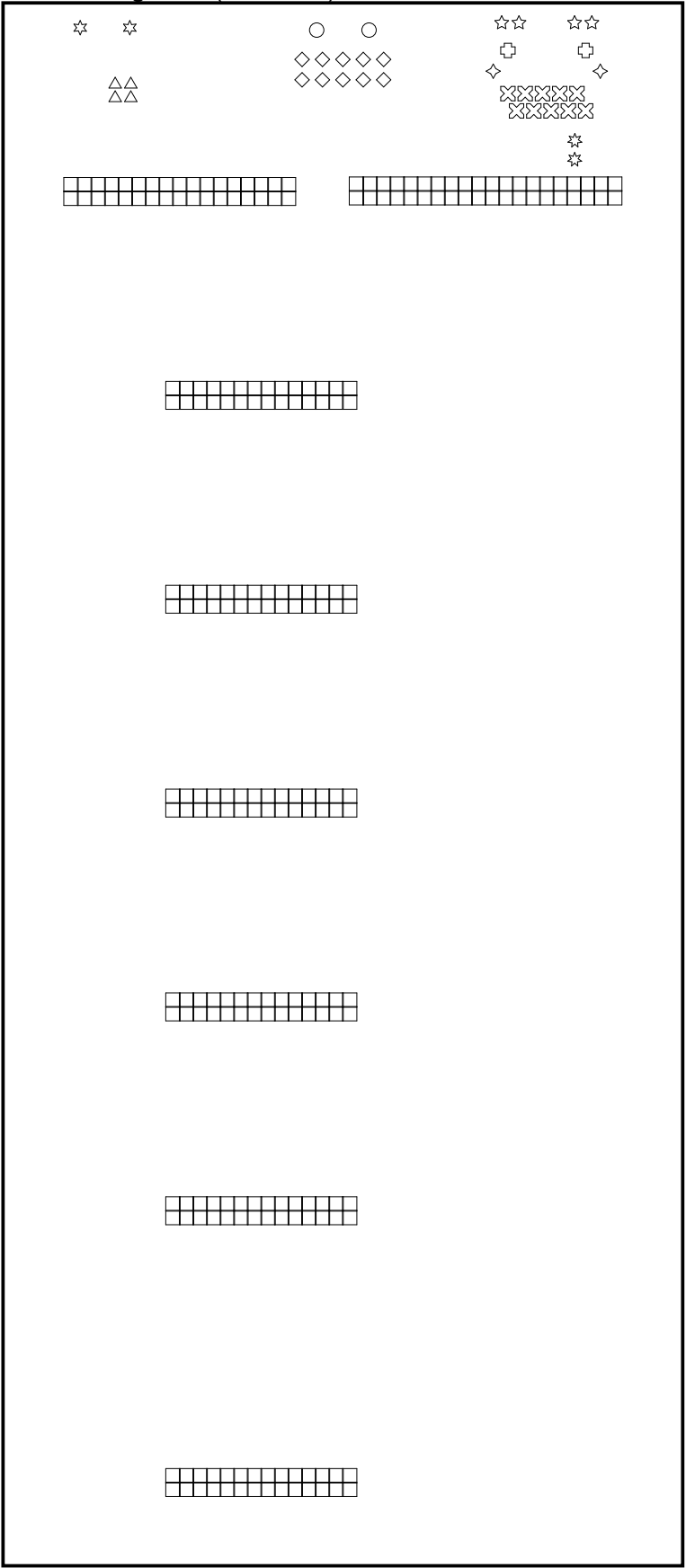
View from Back side (Scale 1:1)

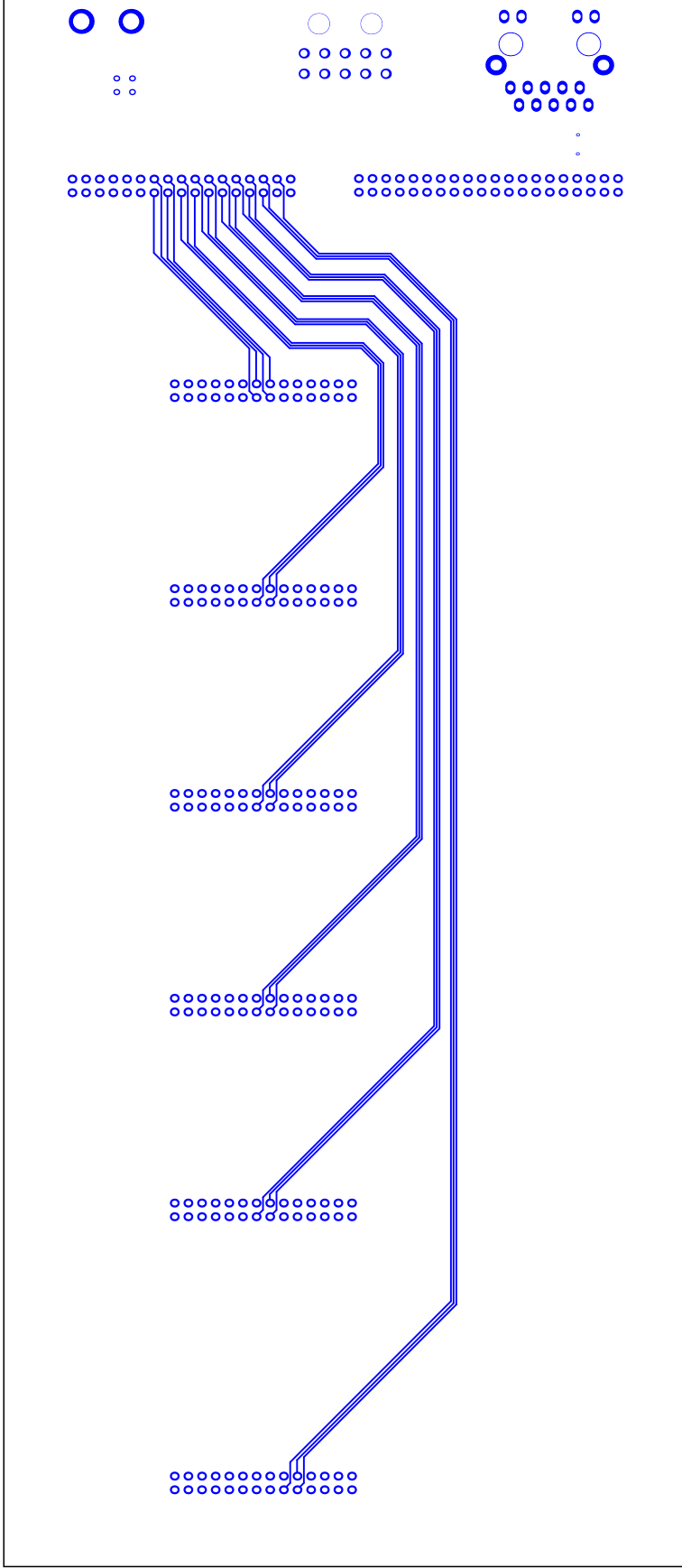
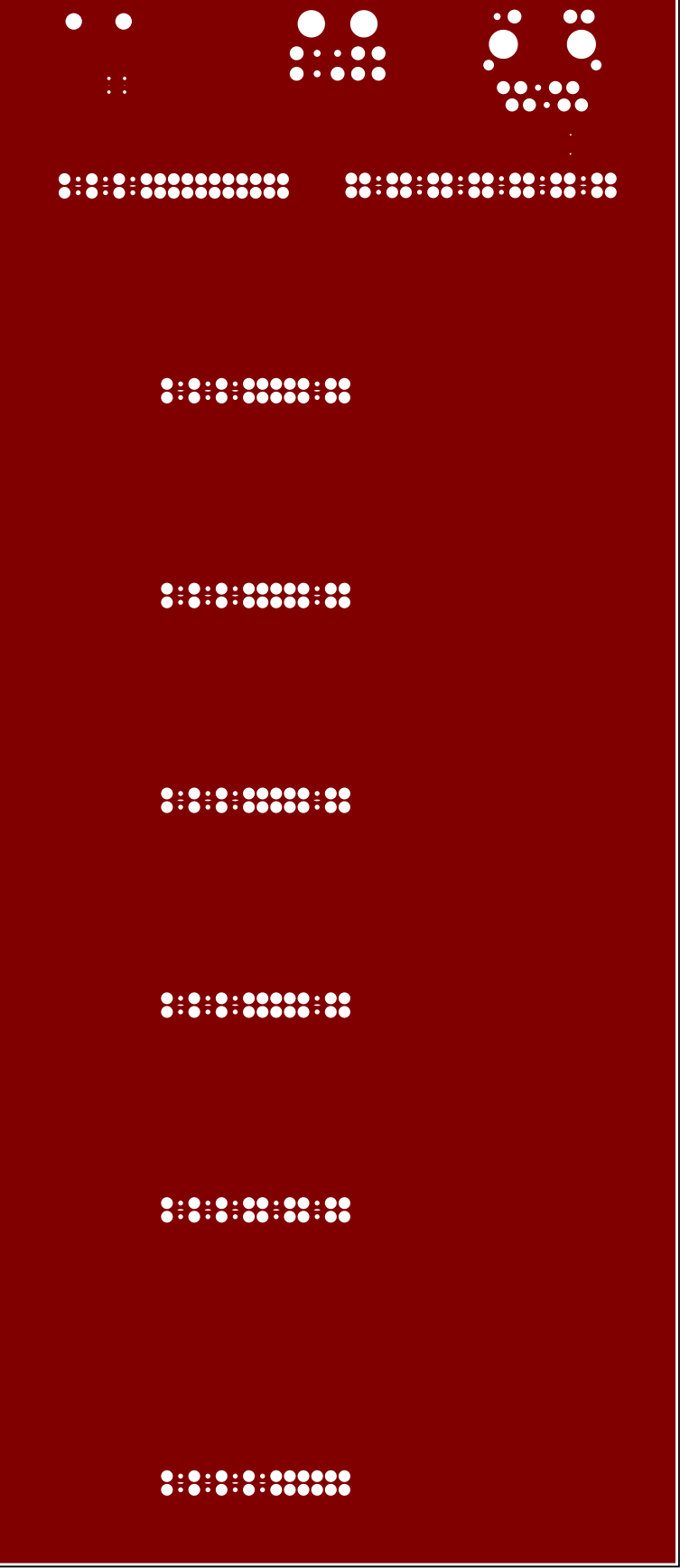
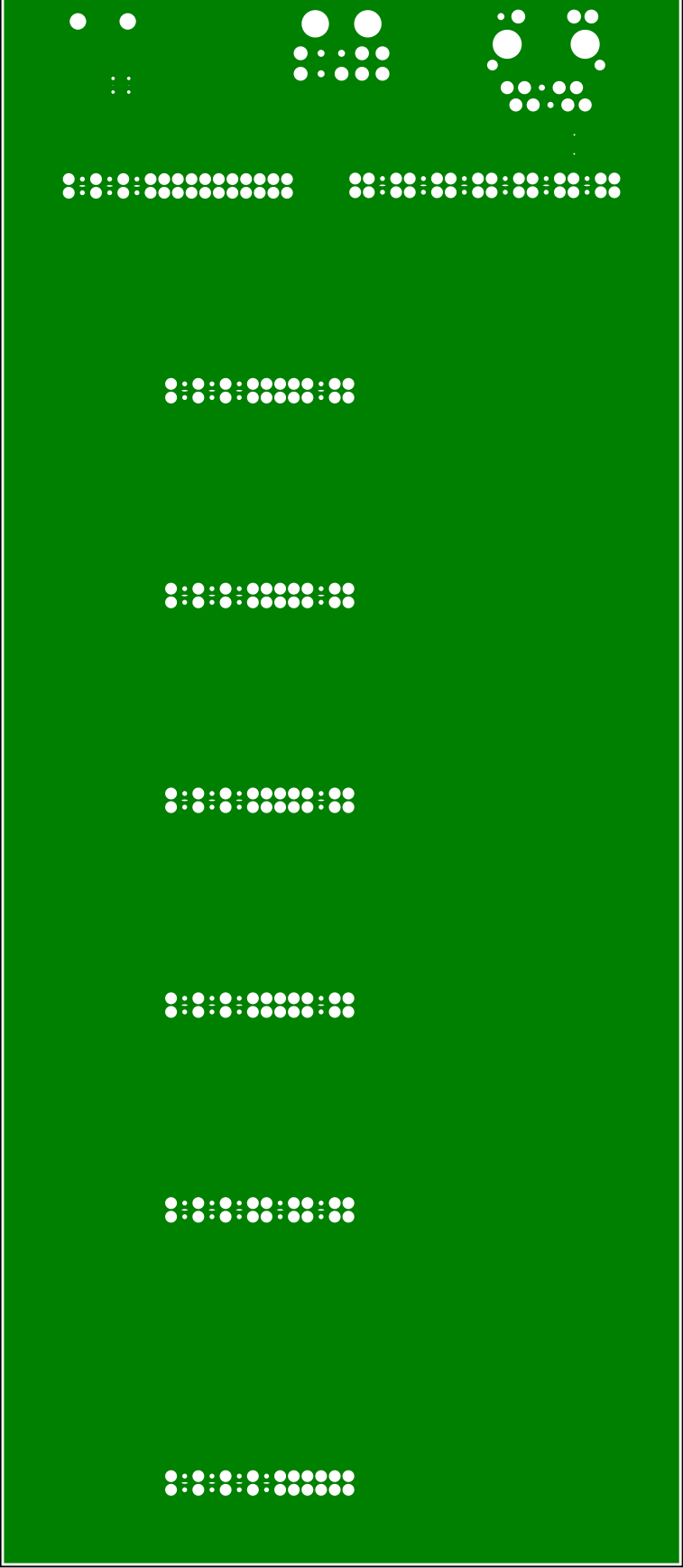
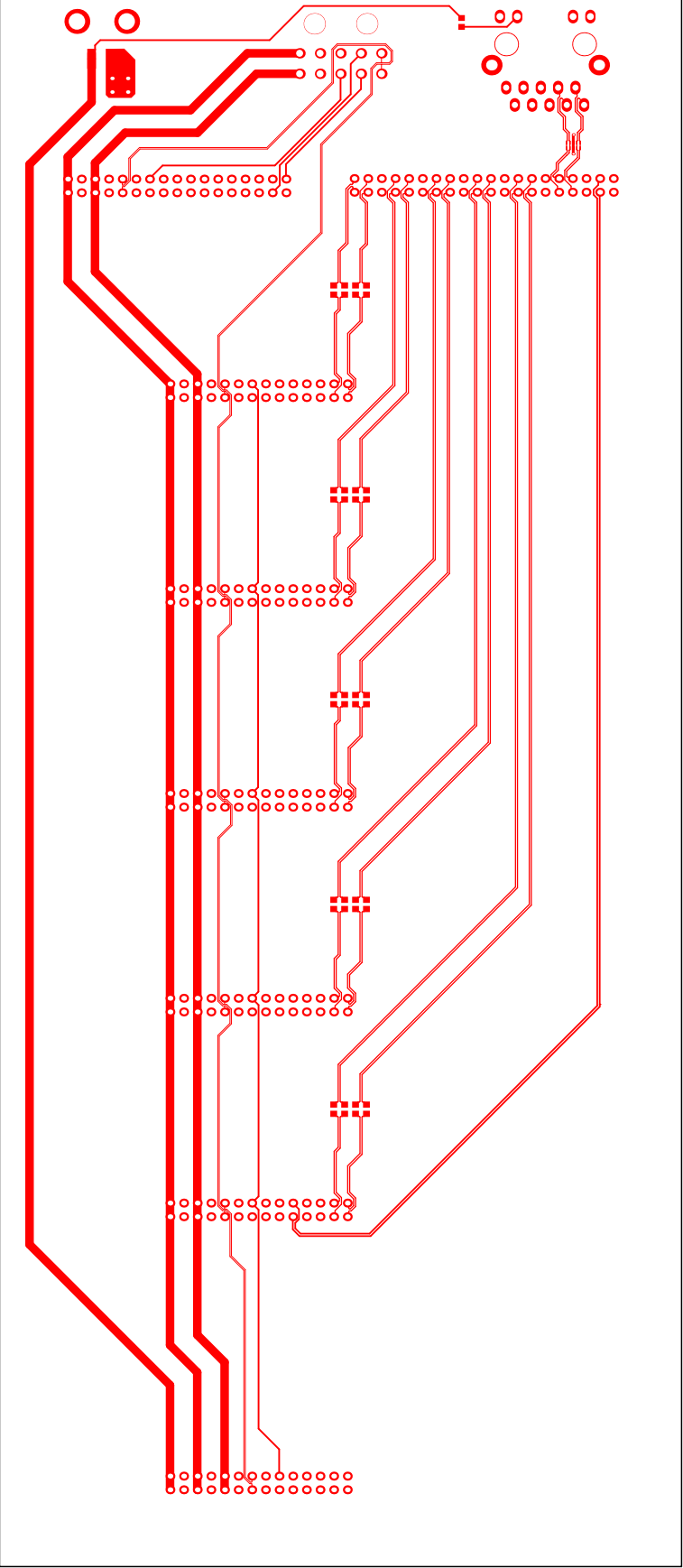


View from Bottom side (Scale 1:1)



Drill Drawing View (Scale 1:1)





Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers	Substack
1	Edge-Coupled Coated Microstrip	100	100.03	Top Layer	0.17mm	0.17mm	0.13mm	Int1 (GND)	Board Layer Stack
2	Edge-Coupled Coated Microstrip	90	89.98	Top Layer	0.24mm	0.24mm	0.13mm	Int1 (GND)	Board Layer Stack
3	Edge-Coupled Coated Microstrip	120	119.98	Top Layer	0.09mm	0.09mm	0.13mm	Int1 (GND)	Board Layer Stack
4	Edge-Coupled Coated Microstrip	100	100.03	Bottom Layer	0.17mm	0.17mm	0.13mm	Int2 (PWR)	Board Layer Stack
5	Edge-Coupled Coated Microstrip	90	89.98	Bottom Layer	0.24mm	0.24mm	0.13mm	Int2 (PWR)	Board Layer Stack
6	Edge-Coupled Coated Microstrip	120	119.98	Bottom Layer	0.09mm	0.09mm	0.13mm	Int2 (PWR)	Board Layer Stack

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⚙	2	0.25mm	Plated	None
△	4	0.51mm	Plated	None
□	242	0.71mm	Plated	+/-0.08mm
⊠	10	0.90mm	Plated	None
◇	10	1.02mm	Plated	+/-0.05mm
☆	4	1.02mm	Plated	None
◊	2	1.57mm	Plated	None
⚙	2	2.41mm	Plated	None
○	2	3.00mm	Plated	+/-0.05mm
⊞	2	3.25mm	Plated	None
	280 Total			

Layer Stack Legend

