Lowered-Complexity Decoding Algorithms of LDPC Codes for Agricultural-WSNs.

Dong-Hee Noh*, Sung-Hwan Jeong*, Ju-Hwan Choi*, Dong-Seong Kim†
*Software Convergence Cluster, Korea Electronics Technology Institute (KETI), Jeonju, South Korea
{dhee.noh, shjeong, netside}@keti.re.kr
†Department of IT Convergence Engineering, Kumoh National Institute of Technology, Gumi, South Korea
dskim@kumoh.ac.kr

***Abstract*—This paper proposes a pattern based Low-density parity-check (LDPC) codes scheme to reduce the decoding complexity using logical XOR. New approaches to this paper describe the pattern based encoder which using logical XOR operation. The proposed scheme can reduce iteration, complexity and packet errors while decoding procedures. It can obtain enhanced throughput performance and at receiver sides in several Signal to Noise Ratio (SNR) levels. Simulation results show that the proposed method can improve the throughput and transmission delay for wireless sensor networks.**

***Index Terms*—LDPC, Sum Product Algorithm Decoding, Decoding Complexity, Decoding Throughput, Wireless Sensor Network.**

I. Introduction

The main objective of recent communication technique such as 5G systems has required the high data throughput with reliable performance because its system demands the continuous communication with device of machine or sensor device. To transmit the high speed of quality data in a Noisy Channel Environment, a suitable coding technique of information is required for application system. Typically, the packet losses sometimes occur due to unreliable wireless links with specific industrial environments such as agricultural or smart factory system. In this reason, robustness and reliability become critical issues in the wireless sensor network. In wireless networks, its system collects a wide variety of environmental data and transmit the actuator controls which owing to maintaining these essential climate factors. In those cases, environments in greenhouse such as temperature and humidity can be affected by the packet transmission failures [1]. Therefore, its climate factors can be seriously affected by the variety of Signal to Noise Ratio (SNR) levels.

In this reason, Ultra Reliable with Low Latency communication (URLLC) has critical issue in 5G systems. The possible solutions can be tailored to different real-time system requirements; low computation complexity, low latency, low cost and higher flexibility. Nowadays, because wireless channels require Shannon limits and reliable BER ratio, to satisfy the URLLC performance for 5G, the several schemes have been proposed recently [2]–[4].

Low-density parity-check (LDPC) code is suitable to correct the data according to be a variety of the SNR levels in wireless standards such as IEEE 802.16, IEEE 802.11, etc. In [6], the LDPC error correction algorithm which trimming the data as using fake error addition was proposed. However, this scheme is limited, in their ability to perform the maximum allowable trimming part of the real-time data. It is seriously affected by complexity because of increasing iteration of decoding procedures.

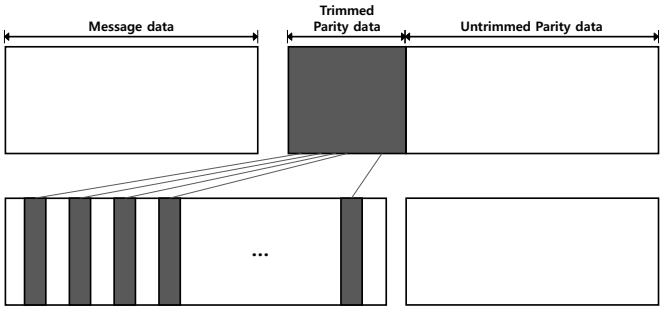


Fig. 1: Schematic of Allocated Parity on Message Data as Fake Error [6].

The main contribution of this paper lies on the possibilities to overcome the limited maximum allowable message data onto Industrial WSNs. Therefore, one of the advantages of the proposed scheme improves the throughput and the complexity of the decoding procedure to compensate the power consumption. Moreover, the proposed scheme can reduce the packet errors in several SNR levels. The proposed scheme includes pattern based different paradigm of real-time data transmission by using logical XOR and mapping group data.

II. Problem Formulation

LDPC itself is considered as an old theory presented by Robert G. Gallager in 1963 [5]. Based on previous researches, Matthew and David have shown that the LDPC code has the ability to meet the Shannon limit. Casado et al. Have shown the possibility of designing and implementing a multiple-rate LDPC code with a constant block length [13]. This idea has been exploited for encoding various messages in the LDPC standard. The code was different from conventional error correction codes; the encoder part of the general LDPC code is considered as harder to construct than the decoder part.

LDPC code can be further exploited in the quasi-cyclic mode where it can be easily decoded [7]–[9]. Several approaches to speed up decoding process also have been con-

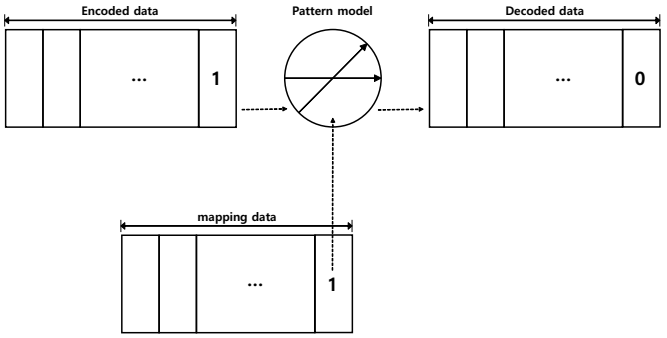


Fig. 2: Decoding Procedure of using Mapping Pattern Scheme: Scenario 1.

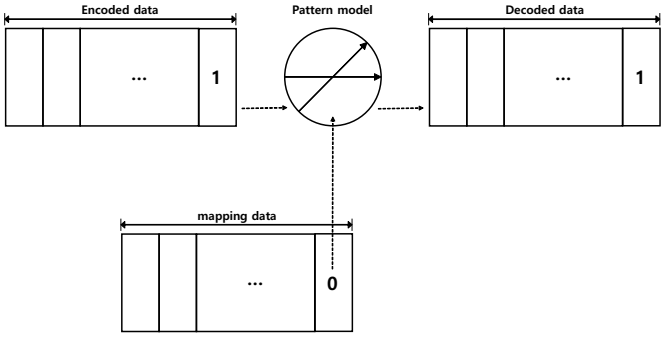


Fig. 3: Decoding Procedure of using Mapping Pattern Scheme: Scenario 2.

sidered at [10]–[12]. This approach was useful in predicting nondeterministic LDPC behavior.

LDPC codes usually can be decoded using the iterative decoding algorithm which is calculated by probability scheme such as Belief Propagation or Message Passing algorithm based on the supervised or unsupervised learning. In order to select the optimal LDPC decoding among these methods, it is necessary to obtain reliable BER performance at various SNR levels and computational complexity To achieve the requirement, a Sum-product algorithm (SPA) technique has been introduced which can reduce the number of decoding iterations.

The SPA algorithm which is one of the technique for reducing the computational complexity of the LDPC decoding scheme is represented by the relation between the bit node based on the Tanner graph and the check node. Although the existing SPA decoding scheme can guarantee BER performance, [7] demonstrate that decoding process in noisy channel environment can increase decoding complexity and iteration in decoding process.

The proposed LDPC code is classified under irregular accumulation (IRA) code, which is composed of message and parity data. Its data can be encoded with a certain rate γ where $1/2 \leq \gamma \leq 5/6$. After encoding process, transmission data will be compressed into n/γ bytes where the message code is n bytes and the parity code is $(1-\gamma)\, n/\gamma$ bytes. The transmitted encoded data over the variety of SNR levels can be affected by the packet transmission failures. To solve this problem, we propose an enhanced LDPC code using the parity allocation and logic XOR computation.

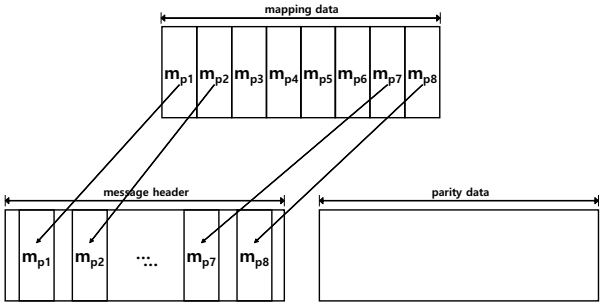
Following the model in [6], some sections of parity data are trimmed and distributed homogeneously over encoding process, the message data are replaced or erased by this trimmed parity data (Fig. 1). At the case, n bytes of message codes are replaced by ρ bytes of the trimmed parity code. Its encoded data consist of $(n/r) - \rho$ bytes of code. However in [6], it can not only increase the number of iterations in decoding, but also causes computational complexity problems.

The encoded data, $(n/r) - \rho$ bytes, can reconstructs to n/r byte according to replacing trimmed parity code, ρ bytes, in message data to original parity data. The transmitted data onto the SNR channel can increase computation complexity of the data reconstruction process by the decoding procedure. Moreover, the iteration count of the decoding will be increased based on the number of error data. To solve this problem, this paper proposes the modified sum decoding algorithm which applied to defined pattern using mapping code.

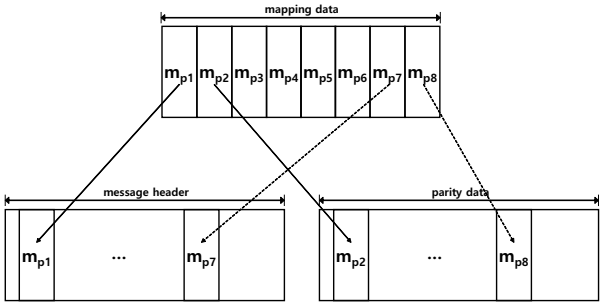
The key idea of the proposed scheme are to optimize the computational complexity of the LDPC decoding while using the trimming parity allocation method. Therefore, we acquire mapping group data by XOR computing between i th and $i+1$ th modified message code in encoding process. That is the main concept of proposed scheme. Finally, encoded data is transmitted over the SNR levels based on several data modulation methods such as FSK or ASK.

Algorithm 1 Proposed Decoding Algorithm

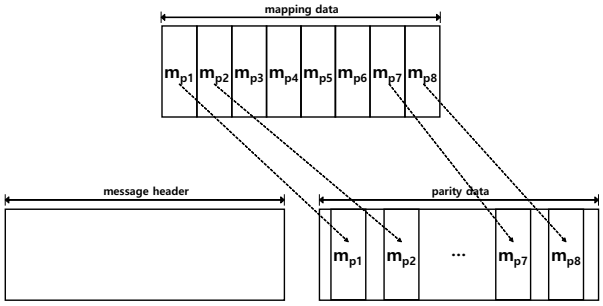
procedure STEP 1: INITIALIZATION
  check code for map pattern = $L\left(r_{i,j}\right)$
  bit code by XOR = $L\left(q_{i,j}\right)$
  $\alpha_{i'j} = sign\left(L^{(\gamma)} g_{ij}\right)$, $\beta_{i'j} = \left(L^{(\gamma)} g_{ij}\right)$
  $\phi = \phi\left(x\right) = log\left(\frac{e^x+1}{e^x-1}\right)$
  if $q_{i,j}\left(0\right) = P_{XY}\left(i_j = 0|y_i\right)$, $q_{n,m}\left(1\right) = P_{XY}\left(x_i = 1|y_i\right)$ **then**
    $L\left(x_n|y_n\right) = log\left(\frac{P_{XY}(x_n=1|y_n)}{P_{XY}(x_n=0|y_n)}\right)$
procedure STEP 2: RENEWING THE CHECK NODE
  for $V_i = 1 : m$ **do**
    if $\gamma \leq \gamma_{iteration}$ **then**
      $L^{\gamma}\left(r_{ji}\right) = \prod_{i' \in \frac{V_j}{i}} sign\left(L^{\gamma}\left(q_{ij}\right)\right) \phi\left(\sum_{i' \in \frac{V_j}{i}} \phi L^{\gamma}\left(g_{ij}\right)\right)$
    else return
  if $m_{p_i} = 1$ **then** $L^{\gamma}\left(r_{2(j)i}\right) = XOR(L^{\gamma}\left(r_{ji}\right))$
  else $L^{\gamma}\left(r_{2(j)i}\right) = L^{\gamma}\left(r_{ji}\right)$
procedure STEP 3: RENEWING THE BIT NODE
  for $C_j = 1 : n$ **do**
    if $\gamma \leq \gamma_{iteration}$ **then**
      $L^{\gamma}\left(g_{ij}\right) = L\left(g_{ij}\right) + \beta \sum_{j \subseteq \frac{C_i}{j}} \left(r_{j'i}\right)$
    else return
  if $L^{\gamma}\left(g_{ij}\right) > 0$ **then** $\hat{x} = 0$,
  else $\hat{x} = 1$,



(a) Example of Mapping Pattern: Scenario 1.



(b) Example of Mapping Pattern: Scenario 2.



(c) Example of Mapping Pattern: Scenario 3.

Fig. 4: Example of Mapping Pattern.

III. Proposed Scheme in LDPC Encoder

There are two primary aims at the proposed encoding scheme: 1. To compress data transmission using trimming way, 2. To make the mapping data which can help to reduce decoding complexity by the handling of iteration. Especially, this paper generates the mapping code by using logical XOR calculation between m_{2n-1} and m_{2n+1}. The following equation shows how the mapping code is calculated by comparing two message bits.

$$m_{1:\frac{n}{2}} = m_{2n-1} \otimes m_{2n+1} = \left\{ m_{p_1}, m_{p_2}, \cdots m_{p_{n/2}} \right\}, \quad (1)$$

The generated mapping code transmits to receiver sides with attached into ahead of message codes. Because of these reasons, the main role of mapping codes help not compress the data transmission but reduce the decoding complexity. The mapping code has two individual patterns, diagonal and direct pattern, it affects to a SPA decoding processing when renewing the bit nodes from check nodes. In this paper, the bit 1 of the mapping code is defined as a diagonal pattern (Fig. 2), and bit 0 is defined as a direct pattern (Fig. 3). When renewing the bit nodes, each pattern in mapping codes sequentially affects the SPA decoding process according to the placement order of mapping code.

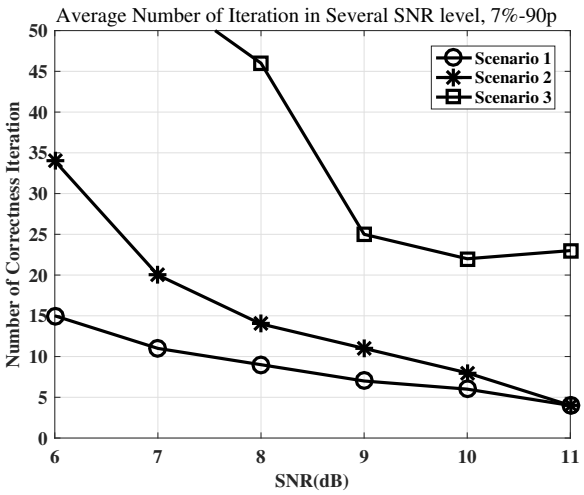


Fig. 5: Average Number of Iteration in several SNR levels, 7%-90p.

IV. Proposed Scheme in LDPC Decoder

In this section, the modified SPA which uses the mapping codes explains how it can reduce the decoding complexity efficiently. The processes of the proposed LDPC decoder are summarized in Algorithm 1.

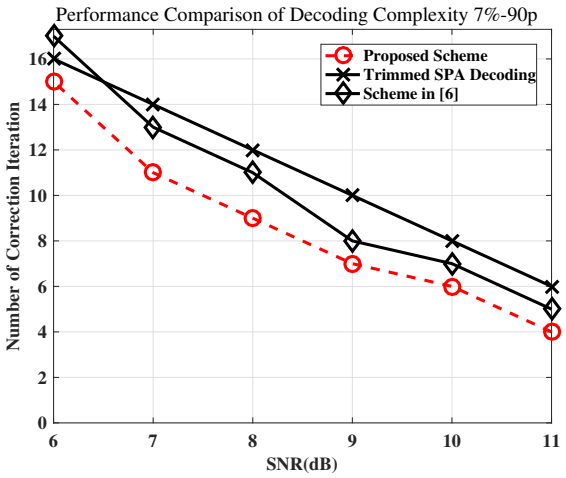
Initialization : Let $L\left(r_{ij}\right)$ denote the transmitted message from check nodes j to bit nodes i, $L\left(q_{ij}\right)$ denote the transmitted message from bit node i to check node j. At that time, we defines that $r_{ij} \in C$ denote the check node with index $i, j \in [1, n]$], $q_{ij} \in V$ denote the bit node with index $i, j \in [1, m]$. The symbol of $N\left(x\right)$ denote the set of neighbors of node x. A log-likelihood ratio (LLR) metric for all bit nodes V_i $(i = 1, 2, \cdots n)$ is given by

$$L\left(g_{ij}\right) = L\left(x_i | r_i\right) = log\left(\frac{P\left(x_i = 0 | r_i\right)}{P\left(x_i = 1 | r_i\right)}\right), \quad (2)$$

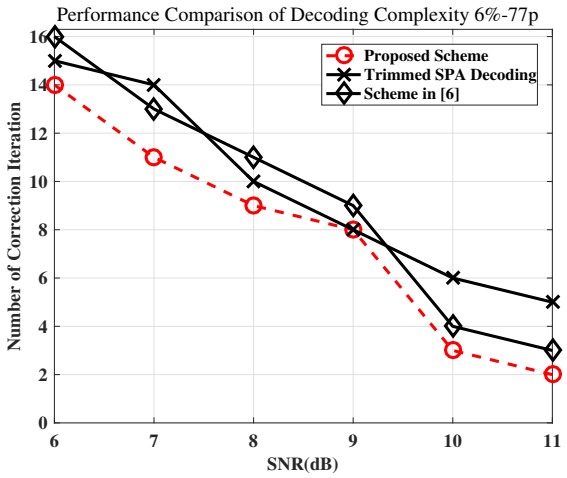
Renewal of Check Nodes : In γth iteration with the corresponding position when $H_{ij} = 1$, check nodes, $C_j (j = 1, 3, \cdots, 2m-1)$, is calculated to $L_{ji}\left(x_i\right)$, which is given by

$$L^{\gamma}\left(r_{ji}\right) = \prod_{i' \in \frac{V_j}{i}} sign\left(L^{\gamma}\left(q_{ij}\right)\right) \times \phi\left(\sum_{i' \in \frac{V_j}{i}} \phi L^{\gamma}\left(g_{ij}\right)\right), \quad (3)$$

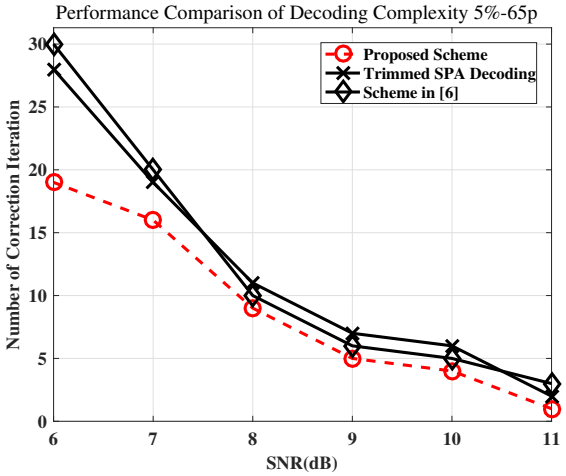
All even number of check nodes is simply determined by mapping pattern which is calculated by encoding process. If mapping codes, m_{pi}, are calculated to 0, ith even number of check nodes, $L_{ji}\left(x_i\right)$, refer to $L_{ji}\left(x_{2i-1}\right)$. However, if



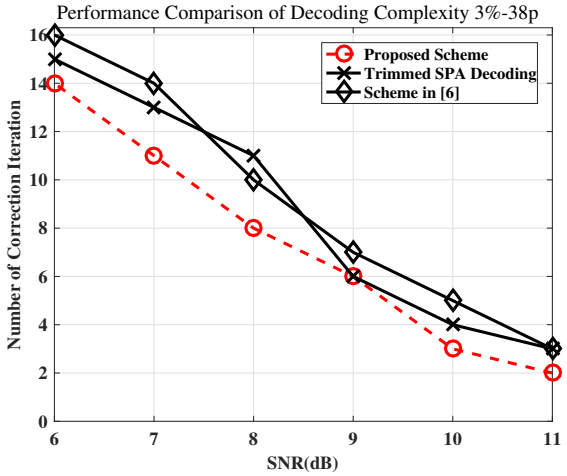
(a) Performance Comparison of Decoding Complexity, 7%-90p.



(b) Performance Comparison of Decoding Complexity, 6%-77p.



(c) Performance Comparison of Decoding Complexity, 5%-65p.



(d) Performance Comparison of Decoding Complexity, 3%-38p.

Fig. 6: Performance Comparison of Decoding Complexity.

mapping codes are calculated to 1, ith even number of check nodes is calculated by equation [1]. It can reduce the decoding complexity during calculation of check nodes.

Renewal of Bit Nodes : In γth iteration with the corresponding position when $H_{ij} = 1$, bit nodes, $V_j(j = 1, 3, \cdots, 2n-1)$, is calculated to $L^{\gamma}(g_{ij})$, which is given by

$$L^{\gamma}(g_{ij}) = L(g_{ij}) + \beta \sum_{j \subseteq \frac{C_i}{j}} (r_{j'i}), \tag{4}$$

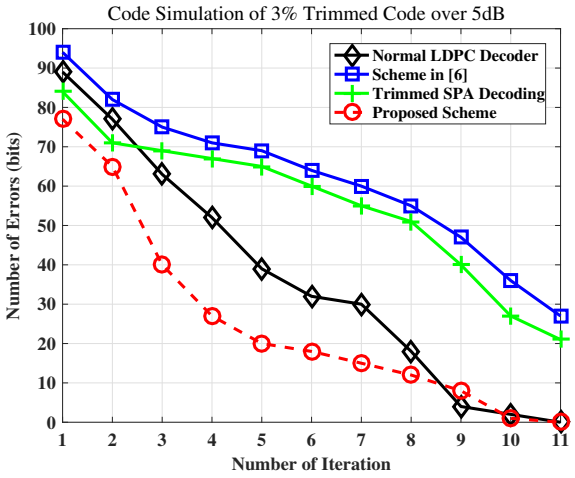
where β is called the trimming factor ($0 < \beta \leq 1$). β compensate the results of SPA decoding process after trimming the codes at encode process.

If $L^{\gamma}(g_{ij}) > 0$, $\hat{x} = 0$, otherwise, $\hat{x} = 1$. All even number of bit nodes is simply determined by mapping pattern, which is similar with procedure of renewal check nodes. If $\hat{x}_{2n-1} = 1$, $\hat{x}_n = 0$ likes diagonal pattern. Otherwise, $\hat{x}_n = 1$ likes direct pattern. Fig. 2 and Fig. 3 show how determine the $\hat{x}$ using proposed mapping pattern.

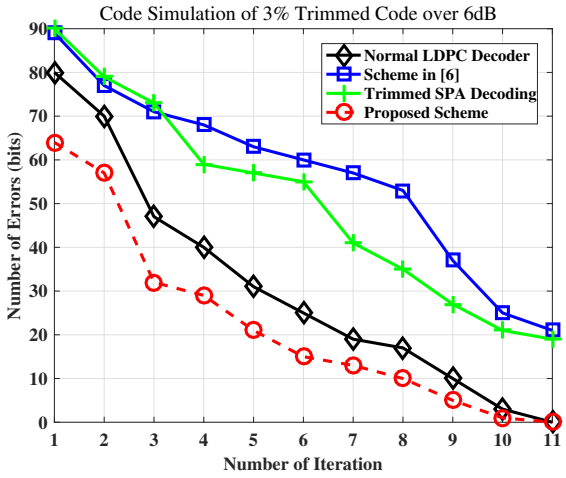
Consider the mapping pattern, the proposed pattern is divided into three methods; scenario 1, 2 and 3. These patterns have different priorities. The first pattern transmits into only message codes. The second pattern transmits the mapping codes between message and parity codes separately. The last pattern transmits only parity codes. It is necessary to analyze that which scenario can achieve accurate and low computational complexity decoding performance (Fig. 4).

V. Simulation Results

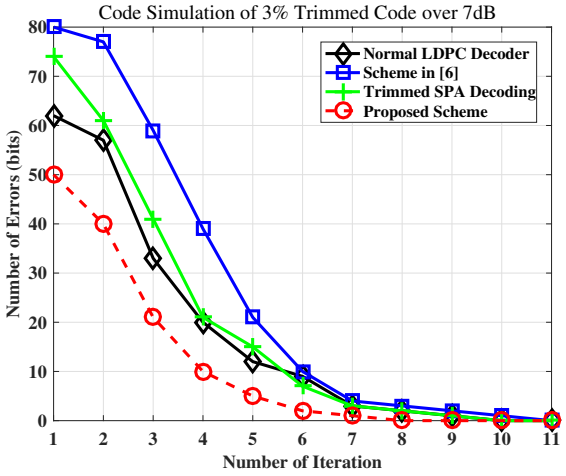
The proposed schemes are evaluated by C++ and MATLAB, where 1296-bit LDPC code with the code rate is randomly generated. The ability of the code in terms of error correction is observed over SNR levels. The simulated trimmed levels were divided into four different levels 3%, 5%, 6% and 7%. For example, when the code is subjected to 3% of the trimmed parity, then 38 parity bits are moved to replace 38 message



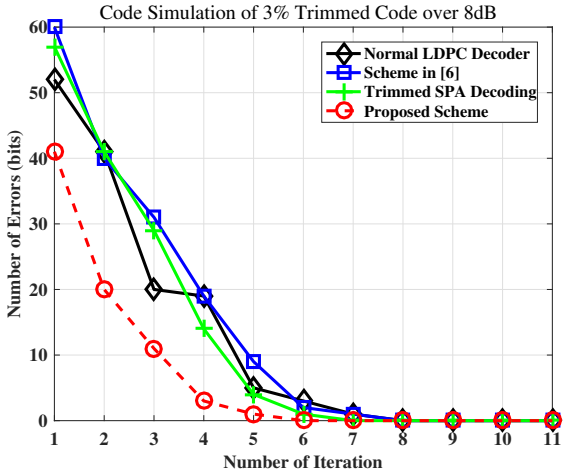
(a) Code Simulation 3% of Trimmed Code over 5dB.



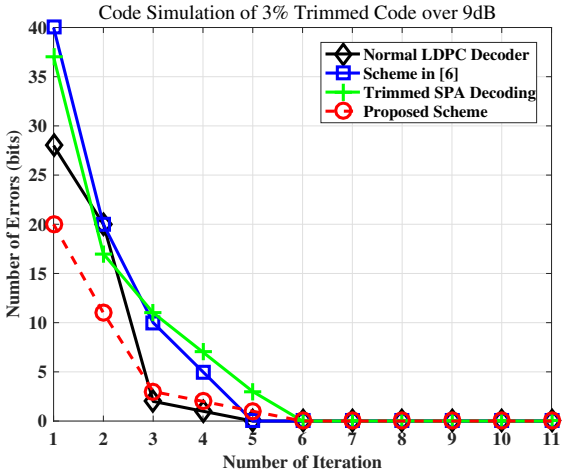
(b) Code Simulation 3% of Trimmed Code over 6dB.



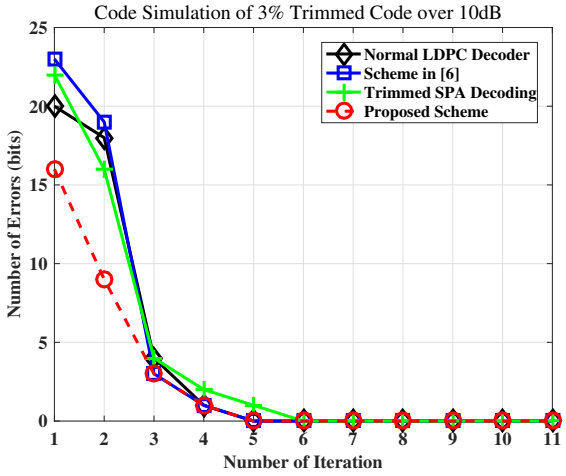
(c) Code Simulation 3% of Trimmed Code over 7dB.



(d) Code Simulation 3% of Trimmed Code over 8dB.



(e) Code Simulation 3% of Trimmed Code over 9dB.



(f) Code Simulation 3% of Trimmed Code over 10dB.

Fig. 7: Performance Comparison of Correction Iteration.

bits, with the result that the code length is 38 bits shorter than the normal LDPC code.

In the first simulation, we examine the efficient method of mapping pattern: scenario 1, 2 and 3 from 11 to 6 SNR levels (Fig. 5). In this simulation, we assume that 7% of the trimmed parity bit is applied to the LDPC code. Transmitting the mapping codes into only parity codes (scenario 3) has a bad decoding performance in less 8 SNR levels. Moreover, comparing between scenario 1 and 2, scenario 1 has a better decoding performance than scenario 2 in less 9 SNR levels. Based on these results, we can be verified that transmitting mapping code into only message code (scenario 1) has a more efficient method than different method (scenario 2 and 3).

Normally, the parity code is used to detect and to correct the errors on all the code (message and parity code). In this case, the parity code has a much higher impact than the message code while the decoding process of the LDPC code. It is effected that cannot detect an error and cannot correct the error during scenario 3 which is replaced with parity bit only. That is why scenario 3 has failed because the parity is not enough to detect an error and to correct errors. Therefore, this paper does not recommend the usage of scenario 3.

In the next simulation, we focused on reducing decoding complexity with apply the proposed mapping pattern in several trimmed parity codes variations on LDPC code (Fig. 6). In [6], they are already verified that trimming scheme can reduce the decoding complexity compared than other LDPC decoders. This paper, we examine that the proposed scheme can show a better decoding complexity performance than [6]. The simulation shows that proposed scheme. The simulation results show that the proposed scheme has a lower decoding iteration rate up to 54% than a normal method in from 11 to 8 SNR levels. Moreover, trimming the parity code to 3% has a minimum decoding complexity when using the proposed mapping pattern.

The last simulation, we examine the data recovery performance on each step of the decoding process for 3% trimming code case (Fig. 7). In this simulation, 3% of the trimmed parity bit is applied to the LDPC code based on Fig 6. The code is applied with various degrees of error, and in the figure, the error levels is denoted as SNR. A high SNR value indicates that the error in the code is less. In contrast, a low SNR value indicates the occurrence of more errors in the code. The x-axis of the figure shows the number of iterations required during the decoding process. The y-axis shows the remaining bit errors in the code after each iteration. It can be observed that for the code with high SNR, the total number of iterations needed to recover the data is small. However, for the code with low SNR, the total number of iterations needed to recover the data becomes large. Based on these results show that the proposed scheme can recover more bit errors than other schemes.

VI. Conclusion

This paper proposes an efficient LDPC code scheme which can reduce the decoding complexity using a logical XOR based mapping pattern. The mapping pattern is obtained by an XOR operation process between two adjacent message bits during the LDPC encoder process. In several simulation results, we could validate the proposed scheme have less decoding complexity and packet errors than the previous scheme.

As a future work, we are planning to improve and extend the proposed scheme to apply less than 6 SNR levels for developing robust systems.

VII. Acknowledgement

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References

[1] S. Maurya, V. K. Jain, "Energy-Efficient Network Protocol for Precision Agriculture: Using threshold sensitive sensors for optimal performance," IEEE Consumer Electronics Magazine, vol. 6, pp. 42–51, 2017.

[2] H. Gamage, N. Rajatheva and M. Latva-aho, "Channel coding for enhanced mobile broadband communication in 5G systems," in IEEE European Conf. on Networks and Communications (EuCNC), Oulu, Finland. pp. 1–6, 2017.

[3] M. Sybis, K. Wesolowski, K. Jayasinghe, V. Venkatasubramanian and V. Vukadinovic, "Channel coding for ultra-reliable low-latency communication in 5G systems," in IEEE Vehicular Technology Conf, Oulu, Finland. Conf. Canada, pp. 1–5, 2016.

[4] M. Shirvanimoghaddam, M. S. Mohamadi, R. Abbas, A. Minja, B. Matuz, G. Han, Z. Lin, Y. Li, S. Johnson and B. Vucetic, "Short block-length codes for ultra-reliable low-latency communications," Information Theory, pp. 1–7, 2018

[5] Robert GGallager, "Low-Density Parity-Check Codes", Cambridge, MIT, 1963.

[6] A. Prasetiadi, D. S. Kim and S. Y. Shin, "Decoding scheme of error correction using fake error addition to compress data transmission", 2013 IEEE International Conference on Consumer Electronics (ICCE), pp. 536–537, 2013.

[7] Chao Chen, Baoming Bai and Xinmei Wang, "Construction of quasi-cyclic LDPC codes based on a two dimensional MDS code", IEEE Communications Letters, vol. 14, pp. 447–449, 2010.

[8] Huang J., Liu L., Zhou W and Zhou S.L, "Large-Girth Nonbinary QC-LDPC Codes of Various Lengths", IEEE Transactions on Communications, vol. 58, pp. 3436–3447, 2010.

[9] Chen, X., Kang, J., Lin, S and Akella, "Memory System Optimization for FPGA-Based Implementation of Quasi-Cyclic LDPC Codes Decoders", Circuits and Systems I: Regular Papers, vol. 58, pp. 98–111, 2010.

[10] Joo-Yul Park and Ki-Seok Chung, Saunders. R and Marcoccia, R.M, "Overlapped message passing technique with resource sharing for high speed CMMB LDPC decoder", IEEE Transactions on Consumer Electronics, vol. 57, pp. 1564–1570, 2011.

[11] Tiwari, H.D., Huynh Ngoc Bao and Yong Beom Cho, "Flexible LDPC decoder using stream data processing for 802.11n and 802.16e", IEEE Transactions on Consumer Electronics, vol. 57, pp. 1505–1512, 2011.

[12] B. Lin, Q. Li, Y. Pei, L. Yin and J. Lu, "High speed LDPC decoder design based on general overlapped message-passing architecture," 2014 Sixth International Conference on Ubiquitous and Future Networks (ICUFN), Shanghai, pp. 454–459, 2014.

[13] Davey, M.C. and MacKay, D.J.C, "Low density parity check codes over GF(q)", Information Theory Workshop, pp. 70–71, 1998.