Implement of 100-Gbps optical transceiver firmware for optical communication systems

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***Abstract*—In this paper, an efficient firmware design scheme is proposed for a 100-Gbps CFP(C form-factor pluggable) optical transceiver. The proposed method uses an FPGA approach to integrate the CFP communication interface and register structure, and uses an MCU to implement the operation of the CFP optical transceiver. To ensure the implemented firmware satisfies the proposed design scheme, a real testbed was constructed and the performance of the firmware was evaluated.**

***Keywords*—CFP, Firmware, optical transceiver**

I. Introduction

In recent years, the demand for integrated telecommunication networks has increased because of the rapid increase in traffic due to the expansion of Information technology devices such as smart devices and intelligent Internet-of-Things devices[1]. Moreover, technology for transmitting 100-Gbps data in the optical transmission network has been studied and is a promising solution to this issue [2]-[3].

An optical transceiver is a module that converts electrical signals received through routers and switches into optical signals for optical fibers, transmits them, and then converts them back into electrical signals. Optical transceivers, which are commercially used in optical transmission networks, support 100-Gbps using 10 or 25-Gbps transmission rate channels, and optical transceivers capable of supporting up to 400 Gbps for the next generation optical communication are under development [4]. The C form-factor pluggable(CFP) optical transceivers one type of optical transceiver used for long distance data transmission over 100-Gbps. The CFP- Multi-Source Agreement(MSA) standard is the industry standard for physical/electrical specifications, control and management practices for quality assurance, and cost savings of CFP manufacturers [5]-[6].

The firmware designed by existing CFP manufacturers is based on industry standards, but manufacturers do not disclose their design techniques. Meanwhile, the Micro Controller Unit(MCU) IC maker has introduced an IC with a basic interface for designing the CFP firmware, but it only provides CFP and host interface functions, not a design method for the entire operation of the optical transceiver [7]. Therefore, new manufacturers must invest cost and development time to design firmware when developing optical transceivers. In this paper, we propose a CFP firmware design method based on the MSA standard. By implementing the CFP firmware using the proposed design method, quality can be assured and cost and development time can be reduced.

II. Related Work

The MSA standard consists of a CFP management interface, a CFP register, and CFP control and monitoring[5]. Fig.1 shows the CFP management interface architecture. The CFP management interface consists of three interfaces: the Mnagement Data Input Output(MDIO)[8] interface between the host and the CFP, the interface between the MDIO interface block and the CFP register, and the interface between the CFP register, nonvolatile memory (NVM) and digital diagnostic monitoring(DDM) . The nonvolatile register(NVR) of the CFP

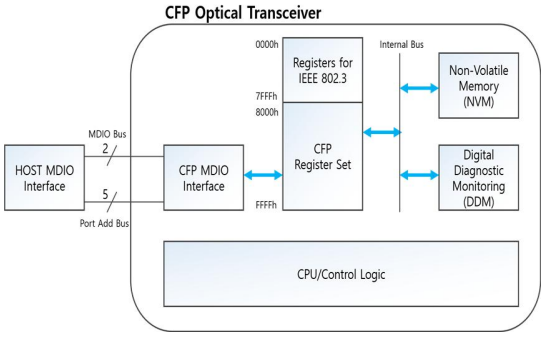

Fig. 1. CFP Management Interface Architecture

register is connected to the ROM, which is a nonvolatile memory, and stores the CFP fixed data. The CFP performs requests from the external host through the internal bus and updates the DDM data. The control logic device controls all operations.

The space of the CFP register has hexadecimal addressing ranging from 0x8000 to 0xFFFF, and is divided into eight sections for CFP register space allocation and access control. Eight tables are allocated to the NVR, and tables 1-4 store basic ID information, extended ID information, network channel specific information, and host channel specific information, respectively. Table 5-6 store information needed by the CFP manufacturer, and table 7-8 allow the user to store necessary

information. The remaining tables are assigned to the volatile register(VR) and configured to store CFP configuration, control, status, and DDM information.

For the operation and termination of the CFP, the MSA standard defines the signals related to the CFP state transition. There are 10 states for initial operation, general operation and termination. Of the 10 states, five states are transient states and five states are continuous states. Each state transitions to the next state when the corresponding signal is applied. Signals for state transitions are defined in detail in MSA standard.

III. CFP Firmware Design Schema

Fig.2 is a block diagram of the entire hardware architecture in which the firmware will be ported. The proposed firmware design technique uses FPGA for the MDIO interface of the CFP and a standard memory configuration. Using The FPGA, design space is minimized by implementing multiple subblocks on a single chip. We also used low-cost, reliable MCU for CFP operation and management functions. The optic

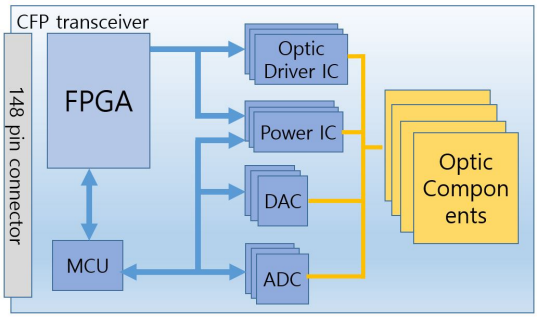

Fig. 2. CFP optical transceiver block diagram

driver IC is an IC needed for the photoelectric and electronic conversion of high-speed data in optical transceivers. The state signals monitored by the optical driver IC are designed to be processed at high speed through the FPGA without going through the CPU, because they need to be updated to the CFP standard memory quickly.

The functionality of FPGA in CFP firmware designed consists of an MDIO interface that communicates with the host, CFP standard memory configuration and access function, CFP hardware pin control function, and CFP power control function. The MDIO interface in the FPGA allows the CFP to communicate with the host. The registers of the FPGA consist of two main registers. The first register is the CFP register, which represents the CFP standard memory. It is implemented according to the CFP-MSA standard memory map, and the external host accesses the CFP register using the MDIO interface. The second register is an MCU interface register that communicates with the MCU to configure the additional memory map needed to control the CFP. In addition, MCU interface blocks exist within the FPGA block to handle requests from MCU.

For the MCU of the CFP, 8051 Silicon Labs chips were selected. The 8051 is widely availble in the industrial sector and provides a reliable library. The 8051 MCU has the SPI and SMbus built in for communication with external chips, and supports up to 256kB of flash memory.

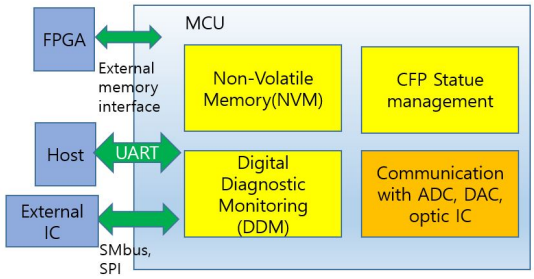

Fig. 3. MCU Function Block Diagram

Fig. 3 shows the internal functional block diagram and the external interface of proposed MCU. The CFP has non-volatile memory that consists of areas such as ”CFP NVR,” ”VENDOR NVR,” and ”USER NVR,”. A part of the flash memory of the MCU is allocated for the NVR memory and the value is stored. The DDM function monitors the state of the CFP optical component read from the external ADC chip and the hardware status read by the MCU internal sensor. CFP Status Management is a function to operate the module according to the CFP state transition described in MSA standard. The IC communication interface is a driver function for communication between the MCU and the external chip. The MCU controls the ADCs, DACs, FPGAs and optical component ICs.

Fig. 4 shows the MCU program flow chart. First, the MCU initialization process initializes the MCU system clock setting and MCU peripheral devices such as the SMbus, SPI, UART, and timer. The ADC / DAC initialization process

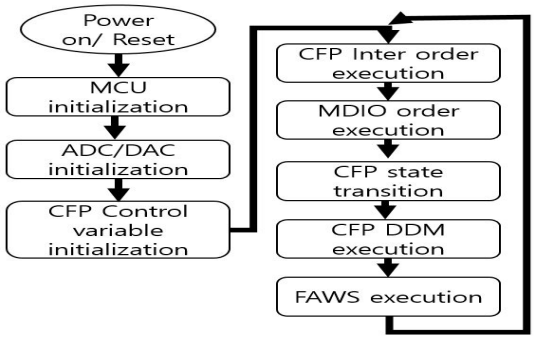

Fig. 4. MCU Program Flow Chart

initializes the external ADC / DAC chip. When initializing the CFP control variables, all the global variables required for the firmware are initialized and the firmware enters the polling loop. Within the polling loop, the CFP handles external requests coming into the UART. In the MDIO instruction process, the MCU accesses the internal status register of the FPGA and checks whether there is an MDIO request from

the current host. If there is a request, the MCU reads the corresponding address and value and processes it accordingly. In the CFP state process, the state transition is managed as in the MSA standard. The CFP DDM process monitors the value from the ADC and updates the DDM value in the CFP standard register. The FAWS process is used to indicate faults, alarms, and warning conditions according to the CFP status.

IV. Experimental Evaluation

We used a Xilinx Spartan-6 series as the FPGA, and the MCU ported firmware was implemented using the 8051 series. The ONT-606 is an optical network test equipment. Fig. 5 shows the test bed configuration. The CFP with implemented firmware is mounted on VIAVI's ONT-606, and a self-loopback was performed using a 40km optical cable. Through testing, we evluated whether the firmware could run the CFP hardware reliably and operate in compliance with the standard.

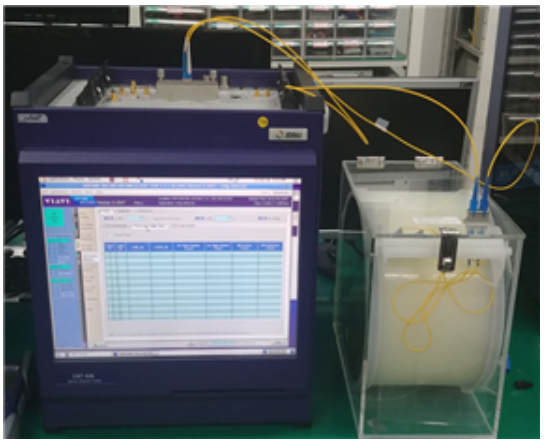

Fig. 5. Testbed Setup

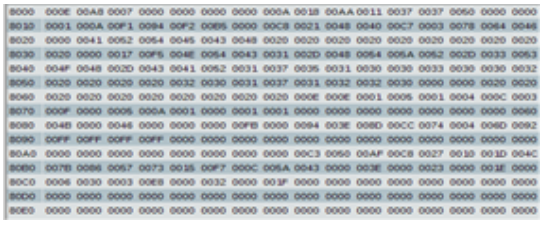

Fig. 6. Access of CFP Memory Map

Fig.6 shows the values read from the FPGA-based CFP memory map. The address starts from 0x8000. This result shows that the MDIO interface is working normally.

Fig.7 shows the result of blocking the optical input of the receiver to check whether the alarm is displayed according to the requirements of the standard.

V. Conclusion

In this paper, we proposed a 100-Gbps CFP firmware design based on the MSA standard and verified its utility

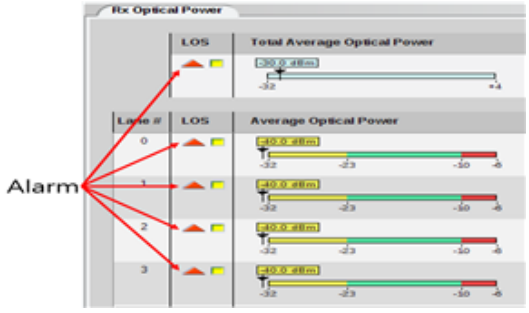

Fig. 7. Result of Alarm Function

by evaluating the actual implemented firmware in a testbed. The proposed method implements the communication interface using an external host and the internal operations of the CFP using FPGA and the MCU, and it was ported to actual CFP hardware. The validity of the proposed firmware design technique was verified through the correct operation of the CFP according to the MSA operation management standard. Moreover, the testbed results confirmed that the DDM accuracy is excellent by comparing the performance of the proposed firmware with that of a CFP of an existing product. The proposed firmware method satisfies the requirements of the standard but does not implement optional conditions such as firmware remote update. In addition, various data driver ICs are being released as the data transfer rate is increasing to 200G / 400 Gbps. We hance plan to design and implement the interface driver accordingly.

Acknowledgment

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