PHD THESIS SUBJECT PROPOSALS - FOR SEPT' 2019

ARCHITECTURE, DESIGN & EMBEDDED SOFTWARE DIVISION (DACLE)

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INTEGRATED VECTOR NETWORK ANALYZER FOR BIOMEDICAL SENSING APPLICATIONS

Thesis Reference: **SL-DRT-19-0290**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LAIR (**RF Architectures & ICs Design Laboratory**)** Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

This thesis addresses the topic of highly integrated vector network analyzer (VNA) in the context of biomedical sensing applications. The thesis study will cover the architecture, the design and the measurement of such a VNA. This PhD research will give the opportunity to work in cross-scientific disciplinary from the microelectronic design to the understanding of biological material characteristics. To achieve this objective several milestone will have to be successfully completed. The awaited innovation will encompass several aspect: high precision local oscillator, high sensitivity, low cost CMOS process.
The thesis will take place in the CEA Leti institute under the supervision of Dr Martineau and Dr Gonzalez (HDR). The publication in journals and international conferences will be encouraged and facilitated.

EDUCATION LEVEL:

Engineer / Master degree (with knowledges in radiofrequency electronics)

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SPINTRONIC WAKE-UP RADIO

Thesis Reference: **SL-DRT-19-0645**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LAIR (**RF Architectures & ICs Design Laboratory**)** Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

The increasing number of wireless connected objects and smart sensors requires defining components and operational schemes that drastically reduce the power consumption. Within such communicating networks the RxTx modules are the most power consuming elements. The solution actively searched for is to switch off the main RxTx module when no communication is requested and to use a low power, degraded wake-up radio receiver WuRx that will switch on the main module when receiving an according wake-up signal. The realization of robust and ultralow power WuRx is an active field of research. The thesis proposes to explore RF spintronic devices as such a compact and low power solution. Magnetic tunnel junctions, which are the main spintronics building blocks, are capable to passively convert an RF signal into a DC signal, with frequency selectivity and at relatively high output signal levels. LETI/DACLE and INAC/SPINTEC work together on the realization of such spintroncis based WuRx and the PhD project will be at the interface of the two laboratories. While SPINTEC will realize the devices and optimize their sensitivity to low input signal levels, the thesis will be carried out at LETI/DACLE to realize the corresponding antenna networks and rf electronics. In order to establish the performance parameters the student will first spend some time at SPINTEC to get trained on the characterization of spintronic based rf components. The student will also be involved in the testing of the developed rf circuits with the spintronics components to iteratively optimize the electronic circuits and adapt it to the spintronics device performances.

EDUCATION LEVEL:

Engineer / Master degree (Electronics, Signal processing)

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INTEGRATED AUTOMATIC CALIBRATION OF DISPERSIONS WITHIN A TRANSDUCERS ARRAY: APPLICATION TO A PMUT ARRAY

Thesis Reference:	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LGECA (**Power Efficiency, Sensors & Actuators ICs Laboratory**)** Location: **Grenoble** Start date of the thesis: 01/09/2019
SL-DRT-19-0293	

ABSTRACT:

The purpose of this thesis is to study and design an integrated electronic system dedicated to the automatic and continuous compensation of dispersions within a MEMS (Microelectromechanical Systems) array.
With the dissemination and the continual expansion of Internet of Things (IoT) and Cyber-Physical Systems (CPS), man-machine and machine-machine interfaces require increasingly efficient and sophisticated sensors. In addition to advantages in cost, reliability, size and power consumption, MEMS based transducers enable sensors to integrate more and more intelligence in their front-end electronics. They also allow innovative topological configurations giving access to measurement ranges that are not addressable by their discrete counterparts.
Arrays of MEMS based transducers enable the spatial discretization of the transduction surfaces and improve the measurements yields and accuracies (gas detector, mass spectrometry, pressure distribution, etc.). They also enable the resolution improvement of electromagnetic and acoustic beams (location, navigation, communication, etc.). Despite the considerable technological advancements that MEMS are continually enjoying, some application requirements are beyond the transducers intrinsic performances. It is then necessary to implement calibration systems to correct the transducers biases introduced during manufacture or evolving with the operating conditions. The evaluation and compensation of these errors requires costly calibration process in a dedicated test laboratory, that are not compatible with massive production.
The aim of this thesis is to achieve an integrated electronic diagnostic alternative, an electromechanical BIST (Built-In Self-Test) specific to transducers arrays, combined with an automatic correction system, which will operate in coexistence with the main functions of the sensor interface.
The proposed use-case is that of PMUT (Piezoelectric Micromachined Ultrasonic Transducer) arrays. These devices offer alternatives and complementary solutions to electromagnetic sensors for detection and localization, gesture recognition or wake-up signals detection. For most applications, these resonant transducers operate in transmit / receive modes (TX / RX) and need to be actuate at their resonance frequency to optimize the transmission power. The emitted and received beam is focused and steered by phase control. Errors and dispersion in the PMUT characteristics generates biases in their resonant frequency, gain and quality factor, leading to losses and distortions in the emitted and received beams. For example, a few percent of dispersions on the mechanical stiffness of the transducers can lead to several tens of percent loss on the acoustic power transmitted to a target.

EDUCATION LEVEL:

Engineer / Master degree (in Microelectronic design, with knowledges Signal processing and mechanical)

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DC-DC POWER CONVERTER AT MICRO-WATT AND MILLIMETER SCALES

Thesis Reference: **SL-DRT-19-0314**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LGECA (**Power Efficiency, Sensors & Actuators ICs Laboratory**)** Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

The PhD focus on the design of fully integrated on-chip DC-DC converter to efficiently deliver nW to µW to emerging ultra-low power devices from battery or an energy scavenger. The integration of power management in the same package as the electronic function is a key performance to achieve efficient, compact and robust autonomous system to widely spread them over environment. Unfortunately the existing power supplies answer partially the challenges in terms of surface, power delivery and efficiency. Based on Internet of Things constraints, the PhD student will study the literature and will propose, design and experimentally demonstrate a relevant topology of DC-DC converter to increase the power efficiency and the power density. The research program will study alternative topologies such as capacitive or piezo-based converter, free oscillating switching converter.

EDUCATION LEVEL:

Engineer / Master degree (Power electronics or Microelectronics)

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SPAD IMAGER FOR HDR TOF USING MULTIMODAL DATA FUSION

Thesis Reference: **SL-DRT-19-0301**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : L3i** (Smart IC's for Image Sensors & Display) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

Depth sensors are currently a very high trending topic. Indeed, in the fields of autonomous vehicles, portable electronic devices and the Internet of Things, new technology enablers now tend to provide handy 3D image data for future innovative end-user applications. There is a great diversity of 3D sensor types, either using passive imaging (depth from defocus, stereovision, phase pixels...) or using active imaging (ultrasounds, structured light, Time-of-Flight...). Each of these systems addresses specifications in terms of depth dynamic range (accuracy of the measurement versus maximum distance). In this thesis, we will study the specific case of Single Photon Avalanche Diodes (SPAD). Recent scientific results regarding this electro-photonic component demonstrate its relevance in the context of Time-of- Flight (ToF) imaging, especially in the case of integration in a 3D-stacked design flow exhibiting a pixel pitch of the order of ten micrometers. However, the nature of the data gathered by this type of component requires significant signal processing within the sensor to extract relevant information. This thesis will aim to revise traditional approaches related to histogram processing by directly extracting statistical features from raw data. Depending on the background and skills of the PhD candidate, two research axes would be investigated. First, on the hardware side, possible modifications of SPAD based sensor architecture in order to provide "augmented" multi-modal information. Second, on the theoretical and algorithmic side, data fusion methods to improve the final reconstruction rendering of depth maps from sensed data.

EDUCATION LEVEL:

Engineer / Master degree

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ADAPTIVE CMOS IMAGE SENSOR FOR SMART VISION SYSTEMS

Thesis Reference: **SL-DRT-19-0335**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : L3i** (Smart IC's for Image Sensors & Display) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

The aim of this thesis is to explore new kind of smart vision sensor architectures using for enhance the sensor reactivity and for simplify the image processing. The studied vision system will use new 3D microelectronic technologies from CEA-leti. These technologies are capable to stack several integrated circuits. The main advantage is to propose a high density of interconnections between them, allowing connection at the pixel level. This characteristic allows us to think about a totally new architecture of the image processing chain of a basic imager (readout, amplification, compensation, colorization, tone mapping) in order to improve the agility, a better image quality, a better energy efficiency, with a low silicon footprint.
The PhD student will benefit during his 3-years thesis of the expertise and the scientific excellence of the CEA leti to attend objectives with a high level of innovation through international patents and publications.
The dynamic and autonomous candidate, will have a microelectronic master degree, specialized in analog integrated circuit design. A good knowledge of circuit design CAD tools will be important (Cadence, and also Matlab) and good knowledge in image processing will be appreciated.
This thesis will start with the state of the art study, then the PhD student will define the optimal architecture. Finally, a test chip will be designed and tested. It will demonstrate the scientific and industrial potentialities of the proposed solutions.

EDUCATION LEVEL:

Engineer / Master degree

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NONLINEAR COMPRESSIVE IMAGING FOR MACHINE LEARNING

Thesis Reference: **SL-DRT-19-0299**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : L3i** (Smart IC's for Image Sensors & Display) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

In a context where the deployment of image sensors combined with computer vision tend to grow very quickly, the major challenges lie in information and signal processing. In the field of smart low-power sensors, the emerging breakthrough technology named Compressive Sensing is of major interest. In the case of embedded systems, autonomous decision-making becomes one of the core device feature while available resources (i.e., memory load, computing complexity and power consumption) remain highly limited. Indeed, the power consumption due to the sensor with dedicated signal processing is largely related to the overall data bandwidth and involved signal dimensionality. In particular, recent theoretical results demonstrate that standard Machine Learning approach can be advantageously applied in the compressed signal domain. However, those results are only restricted to the methods said as « linear », i.e. based on linear projections. The first objective of this PhD will thus be to properly identify theoretical limitations related to the combination of advanced Machine Learning with Compressive Sensing. It will aim at providing cutting-edge algorithm principles outperforming state-of-the-art tradeoffs between resources and inference accuracy. Thanks to a solid background in the laboratory on these fields of research, the goal of this thesis will be to evaluate the interest of introducing non-linearity during the acquisition process in order to improve the overall efficiency. This will help to define proper levers for smart sensor design enabling close-to-sensor context recognition (e.g., specific object detection with a highly limited hardware).

EDUCATION LEVEL:

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ARCHITECTURES TO ENSURE THE FUNCTIONAL SAFETY OF NEURAL NETWORK BASED SYSTEMS

Thesis Reference: **SL-DRT-19-0296**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LISAN** (Digital Design & Architectures Laboratory) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

Neural networks are increasingly used in mission critical systems such as those used for image recognition in autonomous vehicles. These systems must comply with standards for functional safety, therefore it is essential to ensure they operate correctly in the presence of certain types of faults and that they can detect those faults which could result in dangerous situations.

The same formal neural network can be implemented on different hardware platforms (CPUs, FPGAs, etc.), depending on the required performance. In some cases, implementations based on spike coding and neurons can result in significant power savings.

It is well understood how to analyze and improve the reliability of classical digital circuits (micro-controllers, RAMs, etc.), however, these approaches are not directly applicable to neural networks, especially those using spike coding and analog neurons.

The goal of this PhD thesis is to develop new approaches to improve the fault tolerance of spiking neural networks. As the first part of the thesis, new fault models and quantitative metrics to measure the correct operation of the system will be developed. Test cases using both classic coding and spiking networks will be prepared, to provide a reference for the studies. These will include cases using both off-line learning and unsupervised learning. Then the candidate will look for new techniques for detecting and managing faults in order to make the full system more robust. One avenue will be techniques for testing the system while it is operational (on-line test). Another research direction consists of studying how the architecture of the formal network and training data can be adapted to improve fault tolerance.

EDUCATION LEVEL:

Engineer / Master degree in Microelectronic design

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MASSIVELY PARALLEL IN-MEMORY COMPUTING ARCHITECTURE

Thesis Reference: **SL-DRT-19-0364**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LISAN** (Digital Design & Architectures Laboratory) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

Systems-on-chip (SoCs) for embedded computing have always been constrained by memory bandwidth. Nowadays, with the development of application data-intensive, cost (latency, energy) related to memory access for data computation are significantly increasing.

A new computing paradigm consisting in performing data computation within the memory (IMC: In-Memory Computing) has been proposed: the idea is to process data where they are stored in order to save energy and latency. Clear separation between computing and storage units is vanishing leading to very new architectures.

The objective of this thesis work is to define a massively parallel in-memory computing architecture supporting the interconnection of a matrix of computing tiles based on IMC memory for parallel execution (multiprocessor) and parallel data access (multiple memory banks).

The thesis will be based on on-going work in the lab related to SRAM memory and will address higher density memory types.

The subject will require an exploratory approach through modeling of the proposed architecture in relation with the targeted applications (big data, artificial intelligence). Design and silicon implementation of innovative blocks of the architecture will validate to proposed concepts.

EDUCATION LEVEL:

Engineer / Master degree in Microelectronic design, System on Chip Architectures

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CIRCUIT DESIGN OF AN INNOVATIVE LOGIC/MEMORY CUBE FOR IN-MEMORY-COMPUTING

Thesis Reference: **SL-DRT-19-0844**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LISAN** (Digital Design & Architectures Laboratory) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

For integrated circuits to be able to leverage the future “data deluge” coming from the cloud and cyber-physical systems, the historical scaling of Complementary-Metal-Oxide-Semiconductor (CMOS) devices is no longer the corner stone. At system-level, computing performance is now strongly power-limited and the main part of this power budget is consumed by data transfers between logic and memory circuit blocks in widespread Von-Neumann design architectures. An emerging computing paradigm solution overcoming this “memory wall” consists in processing the information in-situ, owing to In-Memory-Computing (IMC).
However, today’s existing memory technologies are ineffective to In-Memory compute billions of data items. Things may change with the emergence of three key enabling technologies, under development at CEA-LETI: non-volatile resistive memory, new energy-efficient nanowire transistors and 3D-monolithic integration. CEA-LETI received a prestigious European ERC grant to support a 5 year project and 3 new PhD students on a new project. This project will leverage the aforementioned emerging technologies towards a functionality enhanced system with a tight entangling of logic and memory. A 3D In-Memory-Computing accelerator circuit will be designed, manufactured and measured, targeting a 20x reduction in (Energy x Delay) Product vs. Von-Neumann systems. This project that adds smartness to memory/storage will not only be a game changer for artificial intelligence, machine learning, data analytics or any dataabundant computing systems but it will also be, more broadly, a key computational kernel for next low-power, energy-efficient integrated circuits.
The PhD candidate will be in charge of the memory architecture definition, the circuit design and the benchmarking of the IMC cube.

EDUCATION LEVEL:

Engineer / Master degree in Microelectronic design, System on Chip Architectures

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HARDWARE/SOFTWARE CO-DESIGN OF COUNTERMEASURES AGAINST FAULT INJECTION ATTACKS

Thesis Reference: **SL-DRT-19-0748**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LIALP** (Software Infrastructure & Tools for IC Laboratory) Location: **Grenoble** Start date of the thesis: 01/09/2019

ABSTRACT:

The thesis will focus on the hardware/software co-design of countermeasures against physical attacks, in particular, fault injection attacks. We will aim at developping new securing solutions that can be applied to all software components whatever their algorithmic nature (e.g. contrary to cryptography-specific countermeasures), able to exploit hardware security properties if available on the target architecture. To do so, we will modify the processor micro-architecture, and exploit code transformation and optimization strategies of the compiler to design new countermeasures with a high security level and a low performance overhead. The thesis is supported by the ANR projet COFFI, starting february 2019 (duration 42 months).

EDUCATION LEVEL:

Engineer / Master degree in Computer science or Electronic Enginering

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STUDY AND IMPLEMENTATION OF NON-RECURRENT DEEP LEARNING ALGORITHMS FOR TEMPORAL SEQUENCES PROCESSING

Thesis Reference: **SL-DRT-19-0393**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LCE** (Computing and Design Environment Laboratory) Location: **Saclay** Start date of the thesis: 01/09/2019

ABSTRACT:

Recurrent neural networks - and notably the Long-Short Term Memory (LSTM) variant - are today at the state of the art for solving many temporal sequence classification problems and in particular used in speech recognition applications (from 2015 for Android) and automatic translation (from 2016 at Google, Apple and Facebook). This type of algorithm is also successfully applied in various applications such as audio event recognition, denoising, language modeling, sequences generations, etc.
The success of these approaches comes however with the cost of huge computing power requirements. This is why most of this algorithms are run on the Cloud, and not on the Edge. Moreover, recurrent neural networks are very sensitive to training parameters and can be difficult to converge because gradients internal to their recurrent structure can easily explode or vanish to zero. The adaptation of these algorithms for an embedded implementation is therefore not straightforward, because the recurrence requires a high precision and partially sequential (large latency) computing.
Some technics for overcoming these difficulties are starting to appear, but are still in their infancy. Among them, a non-recurrent technic allowing sequence processing with less constrain than LSTM seems promising: hierarchical networks. Temporal convolution networks (TCN) are one of their application. The advantages and drawbacks of this model are studied notably in "An Empirical Evaluation of Generic Convolutional and Recurrent Networks for Sequence Modeling" (Shaojie Bai, J. Zico Kolter, Vladlen Koltun). A basic implementation of each structure showed that TCN are more efficient in almost every test cases. Internal gradients are much more stable and computation can be easily parallelized thanks to the elimination of the recurrence.

EDUCATION LEVEL:

Engineer / Master degree (Deep Learning)

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OPTIMIZATION OF COUNTERMEASURE INSERTION FOR THE SAFETY OF INTEGRATED CIRCUITS

Thesis Reference: **SL-DRT-19-0681**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LCE** (Computing and Design Environment Laboratory) Location: **Saclay** Start date of the thesis: 01/09/2019

ABSTRACT:

Hardware Trojans (HTs) are malicious blocks inserted into Systems on Chip (SoC) by untrusted parties in the IC design/manufacturing flow. They have been identified as a realistic threat, among others to the car safety and military. HTs aim to change SoCs' behavior, ranging from denial of service, decreased reliability, to confidential information leakage. Such attacks lead to multi-billions dollars loss per year for the semiconductor industry. Countermeasures against HTs exist, divided into two categories: detection and prevention. Ten years of research have shown that detection is a very challenging task, knowing the stealthy nature of the threat and the multiple possible forms of HTs. Prevention consists in modifying the design flow to take into account security issues. Despite its potential cost, it represents a more effective way to overcome HT insertion. So-called Design-for-Hardware-Trust (DfHT) methods exist, with various goals and impacts on performance. The MOOSIC project proposes a framework dedicated to security that can be integrated into the conventional IC design flow. The goal is to take into account, as early in the design phase, both countermeasures against HTs and performance, to ensure that the SoC behavior is guaranteed despite untrusted IPs vendors or foundry. Towards this objective, the project envisions to establish and evaluate security properties and then integrate them during synthesis with multi-objective optimization techniques, which will be built on a mathematical modeling of the problem that takes into account both the performance and the HTs'effects. It is indeed necessary to find a good compromise between the level of security sought after and performance.

The candidate will have to propose a complete mathematical model of the problem that supports all the constraints and objectives (security, area, frequency, consumption). He will then have to develop optimization algorithms to effectively solve the problem of insertion of countermeasures on conventional criteria (time, area, consumption). Finally, a validation of the methodology on simple first examples is envisaged as well as some test on industrial use cases improvement with some improvement if necessary. The thesis will take place at the CEA LIST LCE and will be led by the LIP6 / Sorbonne University in Paris.

EDUCATION LEVEL:

Engineer / Master degree (Recherche opérationnelle / Optimisation combinatoire)

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A QUANTUM ALGORITHM TOWARD A PRACTICAL EVALUATION OF WORST-CASE EXECUTION TIMES (WCETS) FOR REAL-TIME TASKS

Thesis Reference: **SL-DRT-19-0568**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : L3S** (SW components for System Security & Safety) Location: **Saclay** Start date of the thesis: 01/09/2019

ABSTRACT:

Schedulability analysis is an old research field related to both real-time systems and performance of systems. An important requirement of the schedulability analysis is the availability of upper bounds of execution times. As a consequence, the research field of Worst Case Execution Times (WCETs) started to flourish in the 90s.
For safety critical real-time systems, missing a deadline can lead to catastrophic results, with important damages or even loss of human lives. As such event must be avoided, the schedulability analysis must provide a safe result.
So if exact WCETs cannot be expressed, which is usually the case because they depends on too many parameters including a perfect model of inner-work of the target microprocessor, then a safe upper bound of the WCETs must be provided instead.
However, if it is indeed easy to show overly pessimistic WCETs, e.g. by disabling caches, and serializing instructions in the pipeline, the usefulness of a given WCET estimation decreases as its accuracy is reduced. So a useful WCET should be both safe and as accurate as possible, which is a tricky problem because execution times in modern systems are heavily context dependent, and the mathematical models of WCETs are NP-hard problems.
Within this PhD work we aim at two target objectives: The first si to find a way of modeling the evaluation of WCETs with a quantum algorithm, and the second is to open up another field of application of quantum computing outside of the usual fields of research.

EDUCATION LEVEL:

Engineer / Master degree (Informatic, Applied Mathematic)

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REAL-TIME SYSTEM DESIGN USING FORMAL VERIFICATION OF TEMPORAL PREDICTABILITY

Thesis Reference: **SL-DRT-19-0824**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : L3S** (SW components for System Security & Safety) Location: **Saclay** Start date of the thesis: 01/09/2019

ABSTRACT:

Real-time systems are interested in the use of more and more complex hardware architectures in order to cope with the continuous Increase in complexity and in performance requirements of software, in particular of so called mixed-criticality systems. The temporal predictability of the execution of programs is however not the goal of the designers of these hardware architectures, who instead target the optimization of the average case performances of a system.
In this PhD proposal, we target the design of formal models of hardware components of computer architecture and of their Instruction Set Architecture (ISA) to identify code-specific timing predictability issues. The following two constributions are expected of this PhD thesis:
- the design of appropriate abstractions for a feasible identification of code-specific timing pre dictability issues, a major concern as most commercial architectures are non-predictable. Automatic detection of anomalous timing behaviors is useful to later insert mitigation mechanisms in order to support the design of predictable systems.
- the exploration of the trade-off between average and worst-case performances in order to support the efficient execution of mixedcriticality real-time systems over multicore architectures. Both software and hardware mitigations will be considered, such as the definition of appropriate Real-time system design using formal verification of temporal predictability compilation and/or scheduling rules or adapting the behavior of the hardware to the type of task currently being executed.
As use cases, several hardware architectures will be considered, such as the predictable platform Patmos, but also close to COTS architectures such as RISC-V based processors.

EDUCATION LEVEL:

Engineer / Master degree in computer science or formal methods

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ANALYSIS OF MECHANICAL CONSTRAINTS ON TRANSMISSION LINES BY INSTRUMENTATION WITH SENSITIVE MATERIALS

Thesis Reference: **SL-DRT-19-0683**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LFIC** (Reliability & Sensor Integration Laboratory) Location: **Saclay** Start date of the thesis: 01/09/2019

ABSTRACT:

Reflectometry is as old as electromagnetism itself and share the same principle with radar technologies. CEA LIST has been working on reflectometry to make it available for cable diagnosis through the use of signal processing algorithms and embedded hardware, such as FPGA or SoC. Nowadays, progress in this field opens new possibilities, like transforming cables in distributed sensors, especially for detection of mechanical constraints. This is even more possible by adding to the cable materials with both electromagnetical and mechanical effects, such as magnetostrictive layers.
Previous work on the subject has shown great potential for this combination. Thus the objective of this thesis will be to design a new cable integrating materials sensible to mechanical constraints and reflectometry. First the work will focus on the study of the best material combined with signal processing methods and then the new design will be proposed and tested.
For this PhD project a sound knowledge in the field of electromagnetics is mandatory. It is also expected that the candidate has some basic knowledge in the fields of reflectometry and magnetostriction which are the core technologies used in this PhD project. Additionnaly, a solid background in signal processing techniques will be necessary for both the modelling and the analysis of experimental results. Those skills will also be useful for preparing a potential technological application. An important part of this thesis will also rely on the design of experimental set-ups. It is therefore expected that the candidate has motivation for experimental work.

EDUCATION LEVEL:

Engineer / Master degree (Electromagnetism, signal processing)

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DETECTION AND LOCATION OF FAULTS IN A MULTICONDUCTOR TRANSMISSION LINE

Thesis Reference: **SL-DRT-19-0758**	**Division: DACLE** (Architecture, Design & Embedded Software Division) **Laboratory : LFIC** (Reliability & Sensor Integration Laboratory) Location: **Saclay** Start date of the thesis: 01/09/2019

ABSTRACT:

The proper functioning of a distribution network depends on the ability to quickly detect the occurrence of faults, such as discharges, short circuits or the penetration of moisture in the cables. If the nature of these defects depends on the application context, the techniques used to detect them depend essentially on the ability to request a cable with test signals, and to monitor the appearance of response signals that would testify to the existence of a modification in the cables. While this approach is clear in the case of standard cables consisting of two conductors, the case of Multiconductor cables remains more complex to deal with. Indeed, applying test signals to a pair of conductors typically causes parasitic excitation of nearby conductors, because of the electromagnetic coupling that connects them. This phenomenon can considerably complicate the interpretation of the results of a test, by creating an ambiguity in the identification of the faulty driver, because several drivers can couple with those actually under test.

In this thesis, the coupling will be considered as an opportunity, because it allows to probe a larger number of drivers at the same time. The intrinsic ambiguity of such a proposition can be removed by repeating the tests on several pairs of conductors. It then seems interesting to define optimum choice strategies of drivers to test to cover the largest number of neighboring drivers, without testing all possible combinations. In this sense, this proposal is parsimonious, introducing the concept of effective test surface covered from a pair of conductors.

A promising decision strategy for identifying a failing driver is provided by Bayesian tree and graph-based approaches. These tools make it possible to cross the information obtained in order to identify an explanatory model, here the faulty driver. Among the advantages of this approach we can count on their ability to integrate qualitative information, such as the typology of the defect, and to provide a result formulated in terms of probabilities associated with each possible scenario, thus qualifying the interpretation of results and to assess their reliability, unlike purely numerical methods.

It will then be necessary to carry out a preparatory work, making it possible to evaluate the probability a priori of observing parasitic signals from a fault on a neighboring conductor. This work will be based on the study of line theory and will provide the link between the physical aspects of Multiconductor propagation and the observables considered during the tests.

EDUCATION LEVEL:

Engineer / Master degree (Electromagnetism, signal processing, Applied Mathematic, modelisation, Hyper frequency)

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