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Logică digitală

-Curs 7-

Circuite logice combinaționale

-2021-

Agenda discutie

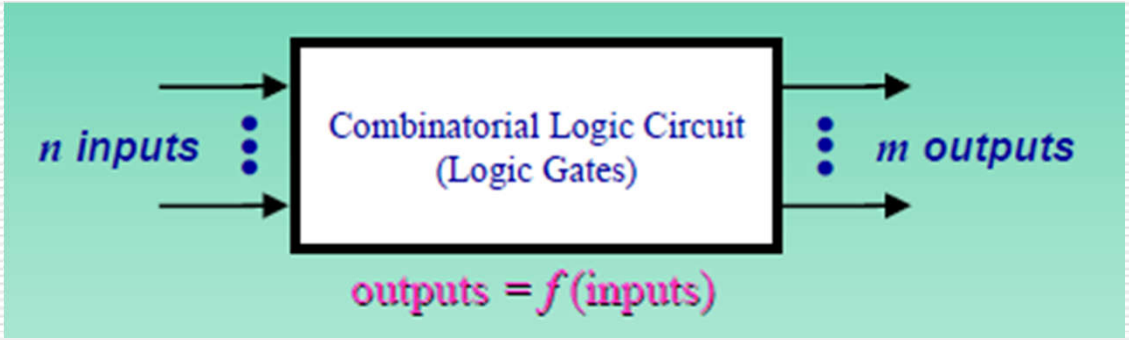
- Administrativ
  - Probleme?
  - Video interactive: MUX, DEC
- Circuite combinationale, clasificare
- Sumatoare: RCA
- ALU
- MUX, DEC

Circuite logice combinaționale

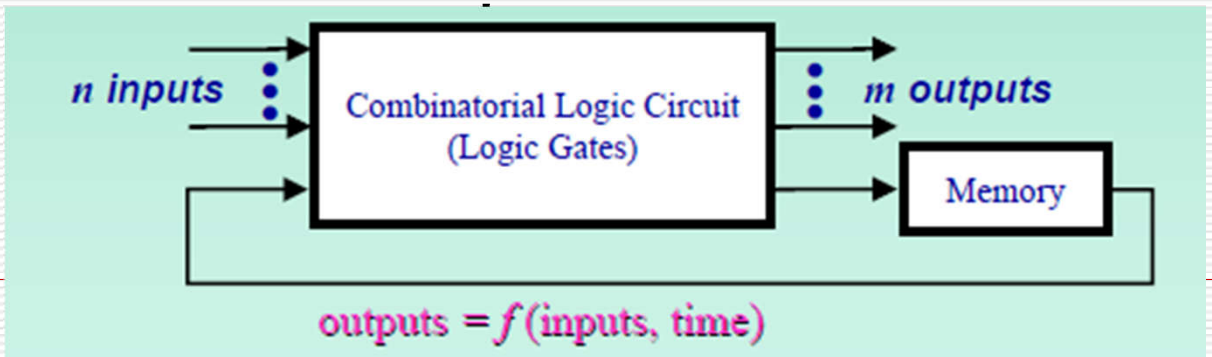
- Circuite de procesare
- Circuite de conversie
- Circuite de interconectare
- Componente universale

Clasificare componente digitale

- Componente combinaționale
  - Ușor de analizat, partiționat, verificat



- Componente secvențiale



Clasificare circuite combinaționale (I)

- Procesare
  - Operații aritmetice (Adunare, Scădere, Înmulțire, Împărțire)
  - Operații logice (ȘI, SAU-Exclusiv, Negare, etc.)
  - Comparare
  - Operații de manipulare la nivel de bit (shift-are, rotație, ...).

Clasificare circuite combinaționale (II)

- Conversie date
  - Codificatoare
  - Decodificatoare
- Interconnect-uri
  - Selecția sursei/destinației
  - Magistrale și interfete magistrală
- Alte componente (blocuri din UC)
  - ROM
  - PLA

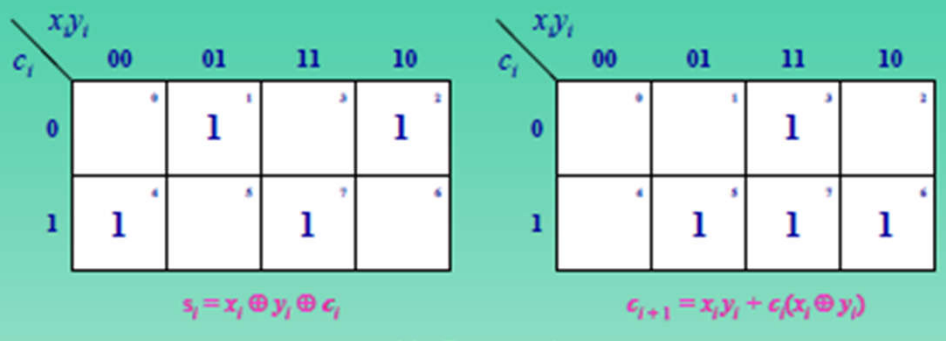
Cuvinte cheie design digital

- Încapsulare
  - Definirea unor componente/blocuri simple
- Iterare
  - Replicarea/Instanțierea componentelor în design
- Ierarhie
  - Realizarea unor blocuri mai mari din blocuri mai mici

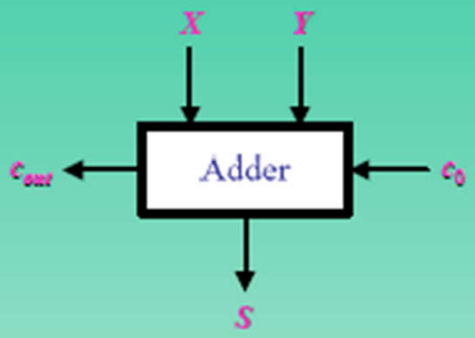
Exemplu – Sumatorul cu propagare serială a transportului

x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

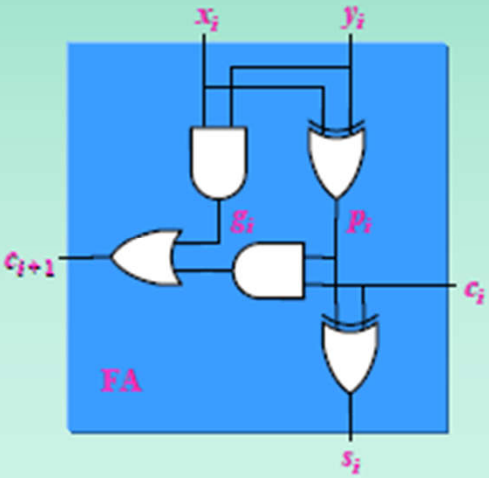
Truth Table



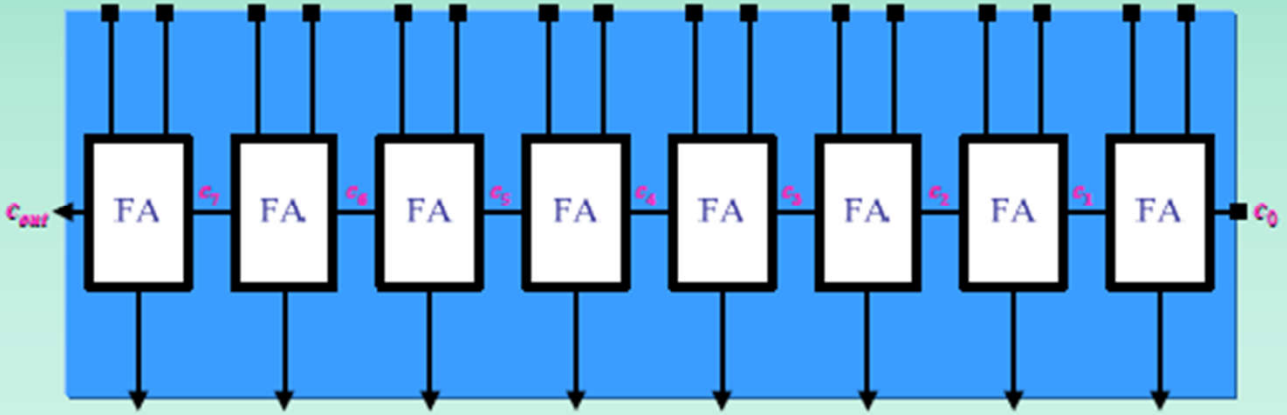
Map Representation



Graphic Symbol



Logic Schematic



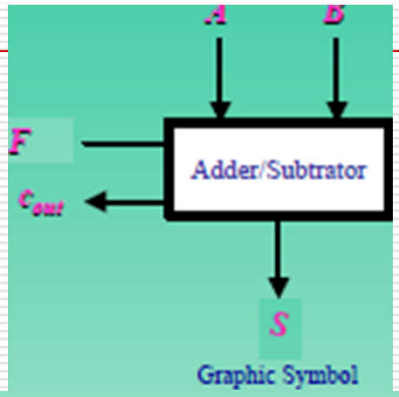
8-bit Adder Unit Schematic

Slides by Philip Pham, University of California, Irvine

Unitate sumator/scăzator C_2

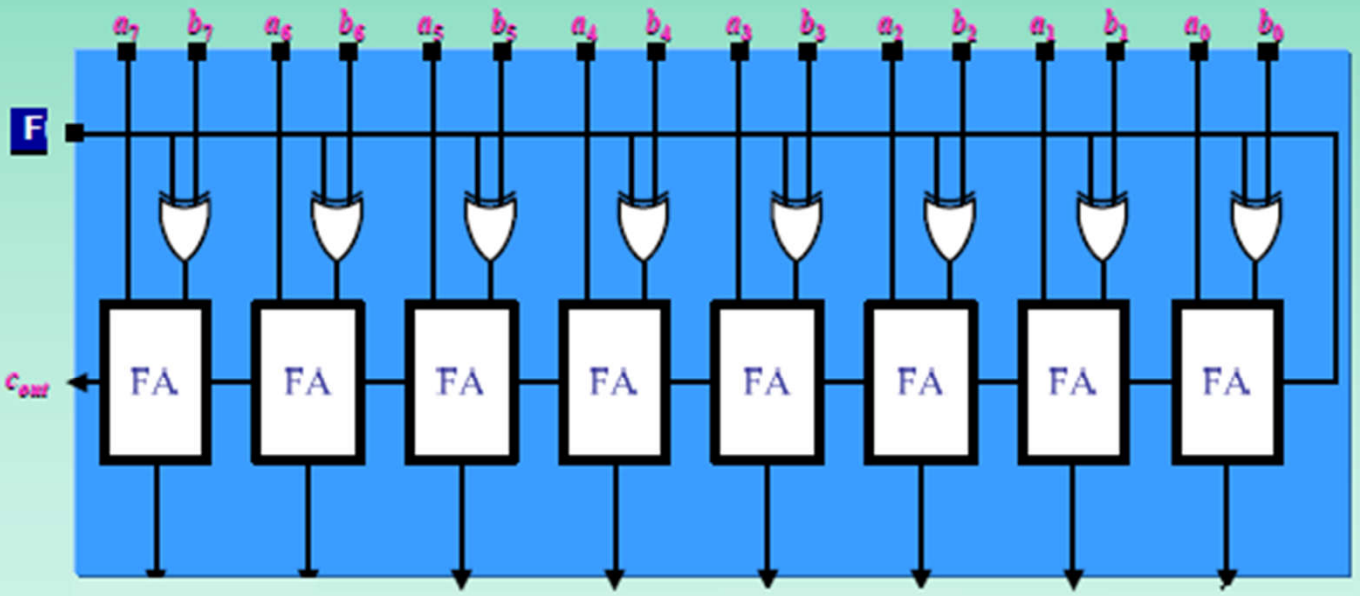
- Scădere

$$A - B = A + B' + 1$$



F	Function	Comment
0	$A + B$	Addition
1	$A + B' + 1$	Subtraction

Truth Table



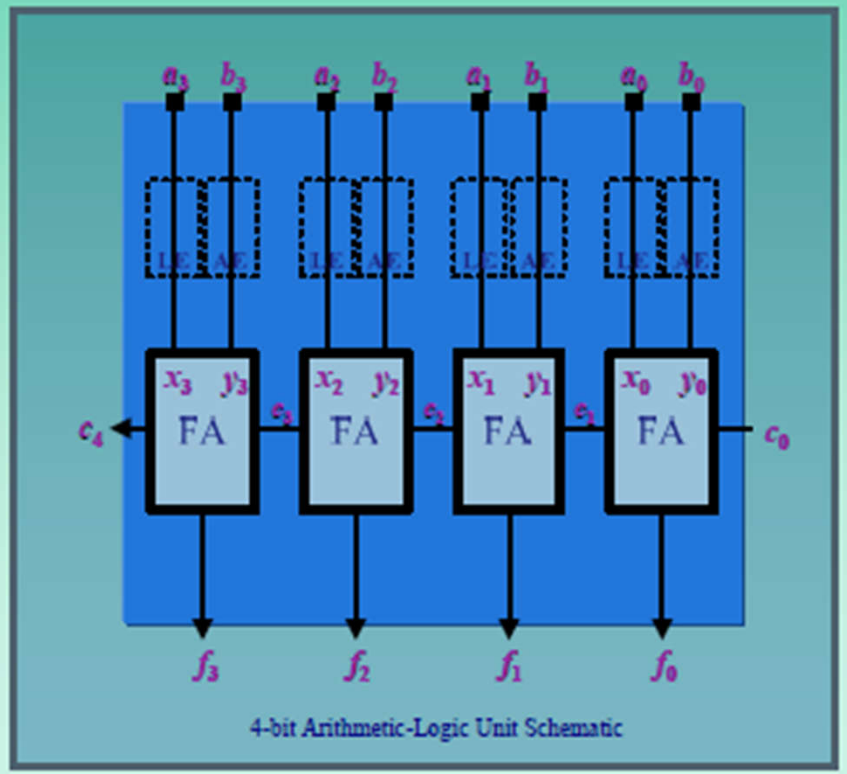
8-bit Adder/Subtractor Unit Schematic

Slides by Philip Pham, University of California, Irvine

Unitate Aritmetico-Logică (ALU)

- Realizează operațiile operațiile aritmetice și logice elementare:
  - Aritmetice: adunare, scădere, incrementare, decrementare
  - Logice:ȘI, SAU, Identitate, Negare
- Toate operațiile aritmetice se bazează pe sumator → blocul de bază este sumatorul
- Trebuie configurați corespunzător operanzii → bloc dedicat de extensie op.aritmetice

ALU



4-bit Arithmetic-Logic Unit Schematic

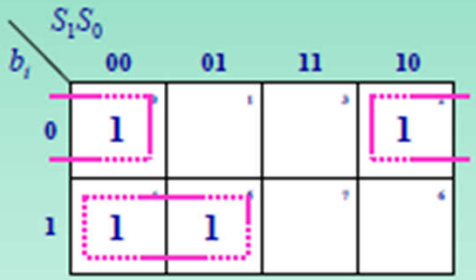
Bloc extensie aritmetică

M	S_1	S_0	Function Name	F	X	Y	c_0
1	0	0	Decrement	$A-1$	A	all 1's	0
1	0	1	Add	$A+B$	A	B'	0
1	1	0	Subtract	$A-B$	A	B'	1
1	1	1	Increment	$A+1$	A	all 0's	1

Functional Table

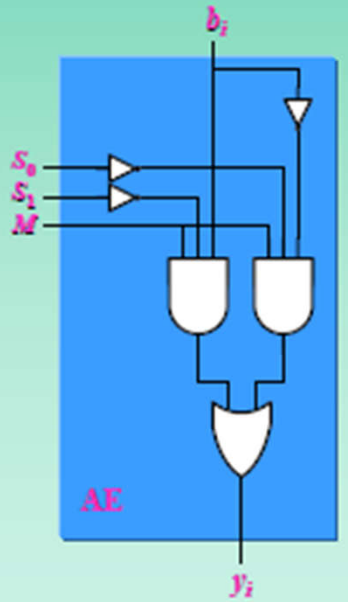
M	S_1	S_0	b_i	y_i
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Truth Table



$y_i = M S_1' b_i + M S_0' b_i'$

Map Representation



Logic Schematic

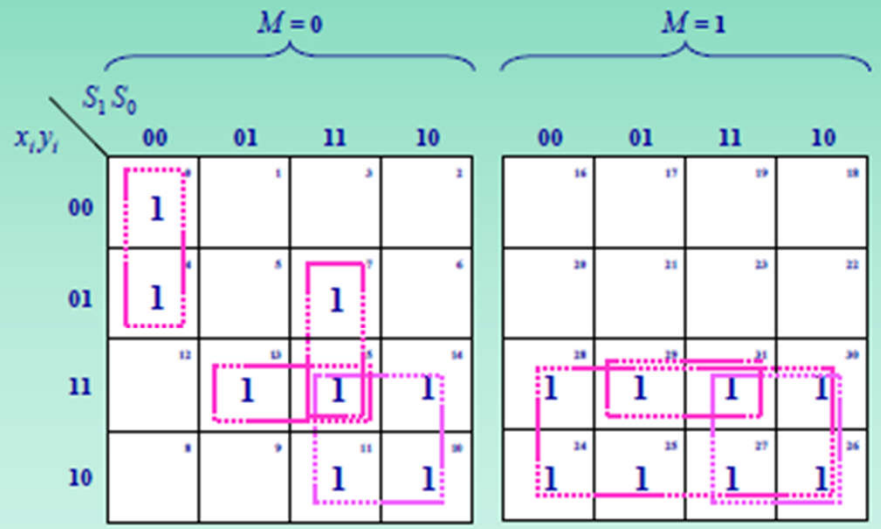
Bloc extensie operații logice

M	S_1	S_0	Function Name	F	X	Y	c_0
0	0	0	Complement	A'	A'	0	0
0	0	1	AND	A AND B	A AND B	0	0
0	1	0	Identity	A	A	0	0
0	1	1	OR	A OR B	A OR B	0	0

Functional Table

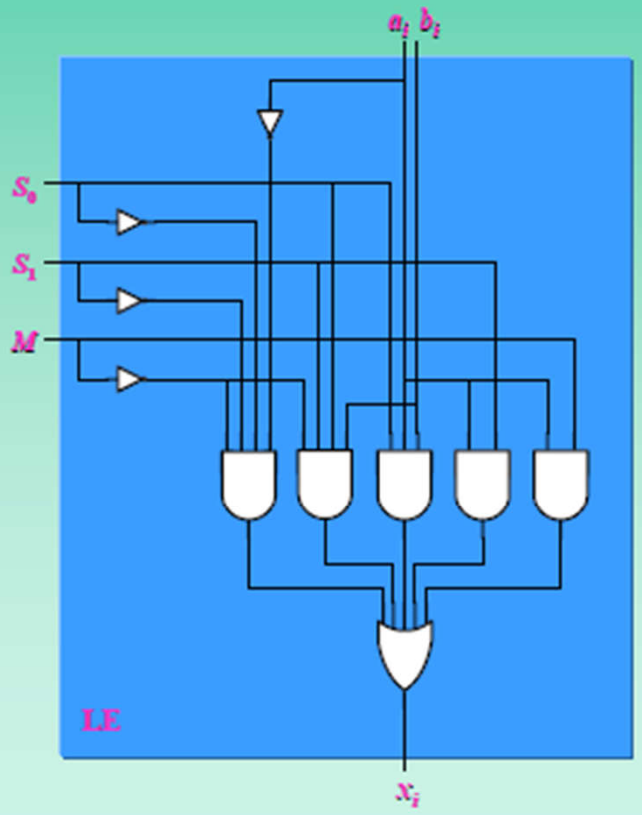
M	S_1	S_0	x_i
0	0	0	a'_i
0	0	1	$a_i b_i$
0	1	0	a_i
0	1	1	$a_i + b_i$
1	X	X	a_i

Truth Table



$$x_i = M' S'_1 S'_0 a'_i + M' S_1 S_0 b_i + S_0 a_i b_i + S_1 a_i + M a_i$$

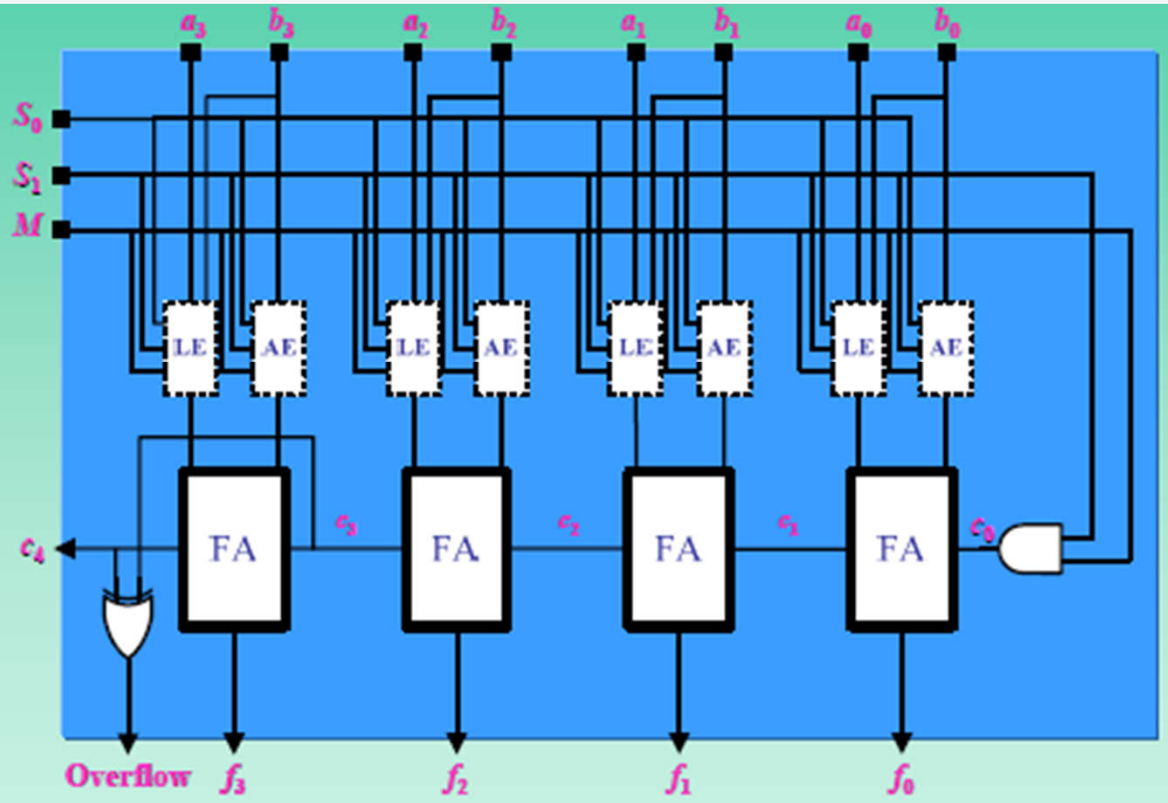
Map Representation



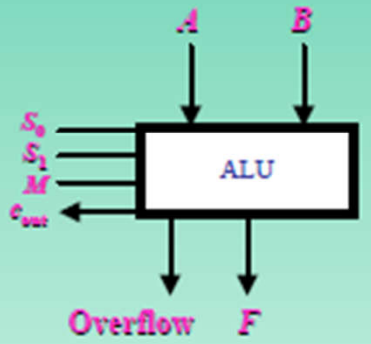
Logic Schematic

Slides by Philip Pham, University of California, Irvine

Arhitectură ALU



4-bit Arithmetic Logic Unit Schematic



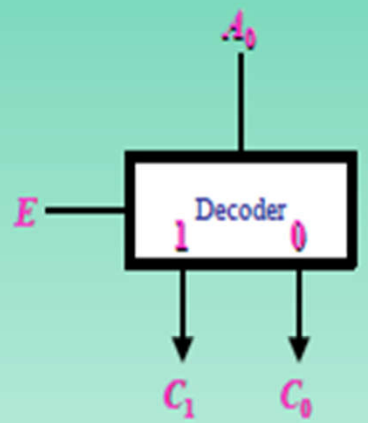
Graphic Symbol

Slides by Philip Pham, University of California, Irvine

Decodificator

- circuite logice combinaţionale ce prezintă un anumit *n* intrări şi până la 2^n ieşiri, care activează **ieşirea (UNA SINGURĂ)** corespunzătoare valoarii combinaţiei vectorului de intrare
- Pot avea intrări de activare, astfel încât ieşirea selectată nu pot fi activată decât dacă intrarile de activare sunt active.
- Pt. n intrări şi cu m ieşiri → decodificator n-la-m.
- Uzual sunt folosite pt. activarea (EN) componentelor

Decodificatorul 1-la-2



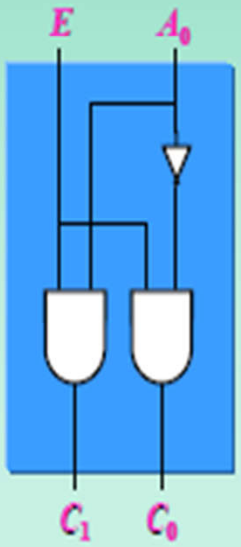
Graphic Symbol

E	A_0	C_1	C_0
1	0	0	1
1	1	1	0
0	X	0	0

Truth Table

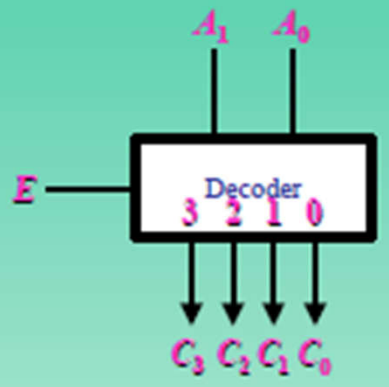
$$C_0 = EA'_0$$
$$C_1 = EA_0$$

Boolean Expression



Logic Schematic

Decodificatorul 2-la-4



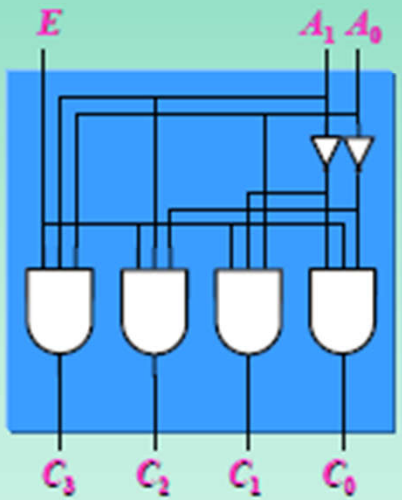
Graphic Symbol

E	A_1	A_0	C_3	C_2	C_1	C_0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0
0	X	X	0	0	0	0

Truth Table

$$C_0 = E_0 A'_1 A'_0$$
$$C_1 = E_0 A'_1 A_0$$
$$C_2 = E_0 A_1 A'_0$$
$$C_2 = E_0 A_1 A_0$$

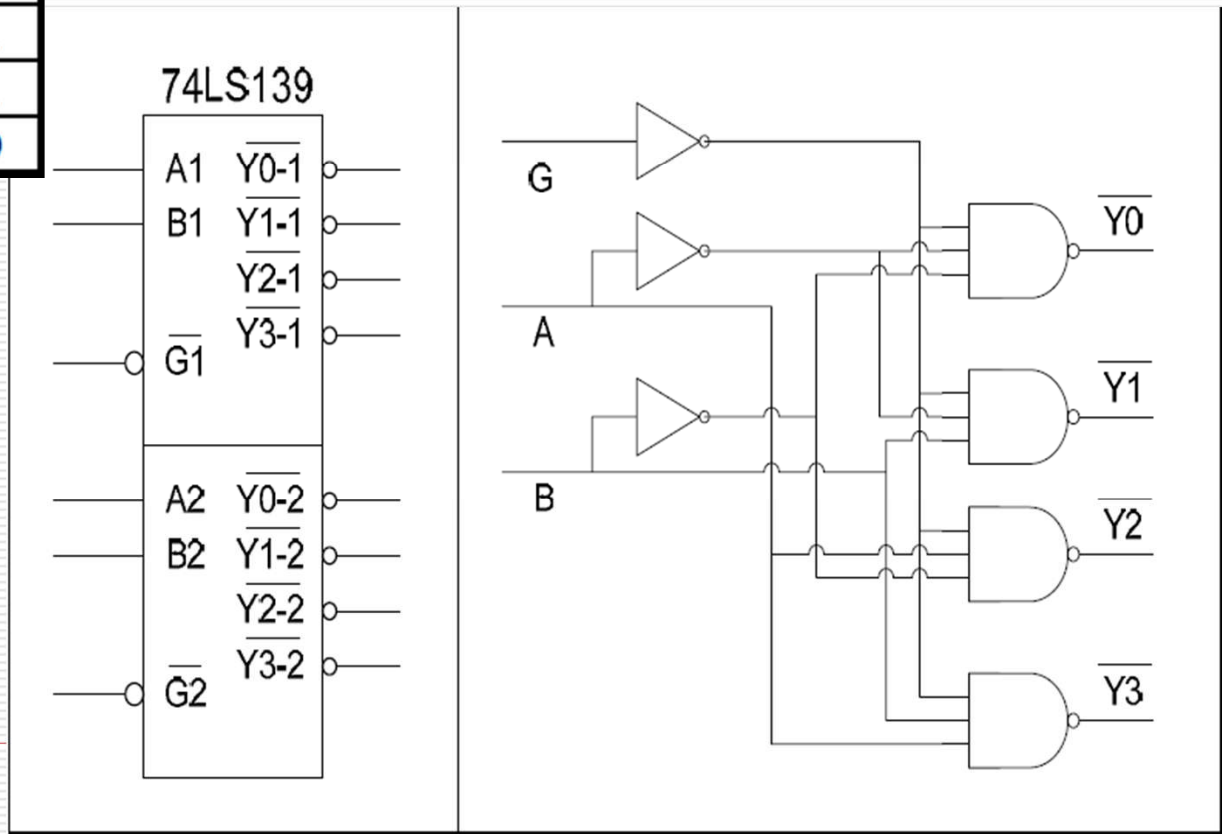
Boolean Expression



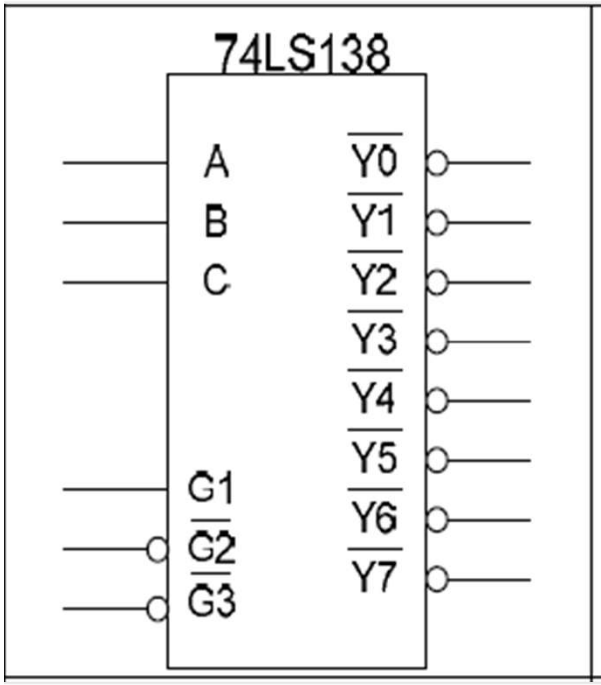
Logic Schematic

Circuite integrate pe scară medie ce îndeplinesc funcţia de decodificator

G	A	B	Y0	Y1	Y2	Y3
1	x	x	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

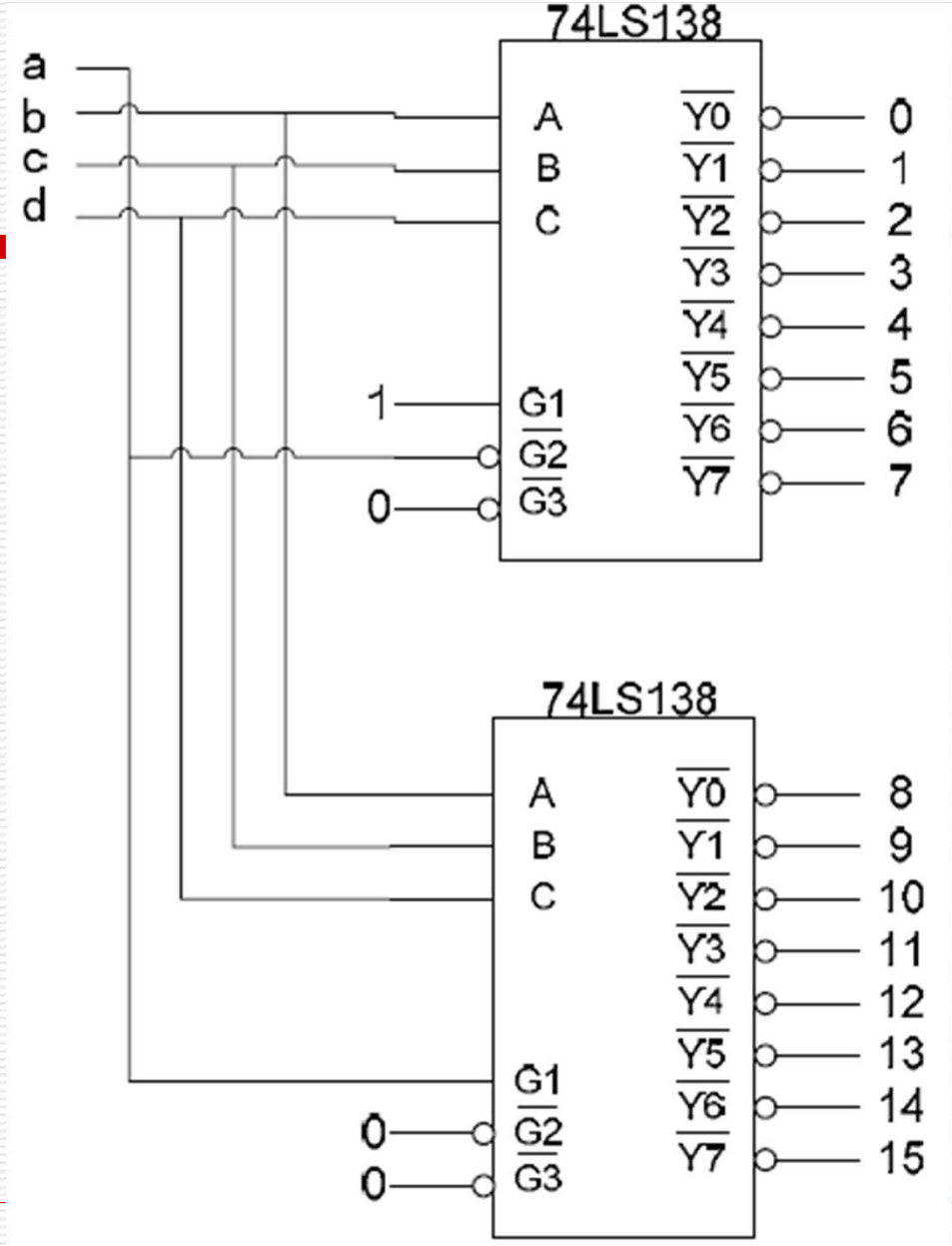


74LS138: decodificator 3-la-8

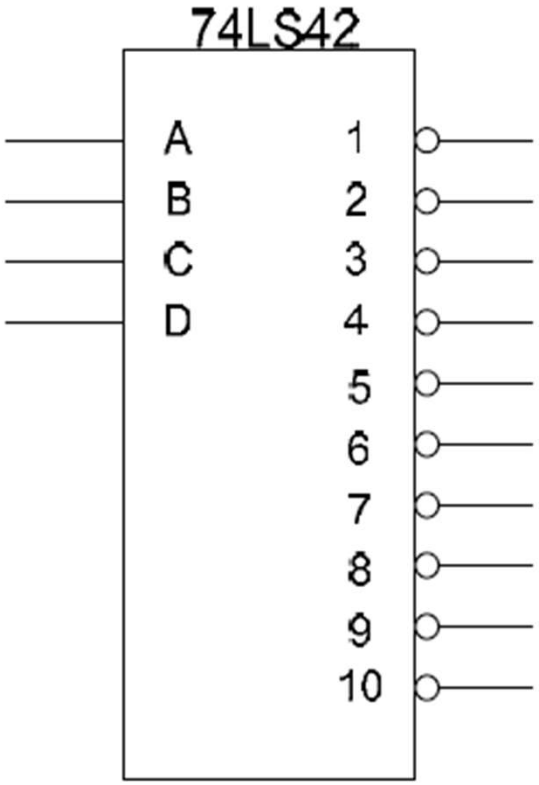


G1	G2	G3	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

DEC 4-la-16


74LS138
a
b
c
d
A
B
C
1
G1
G2
0
G3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
0
1
2
3
4
5
6
7
74LS138
A
B
C
G1
0
G2
0
G3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
8
9
10
11
12
13
14
15

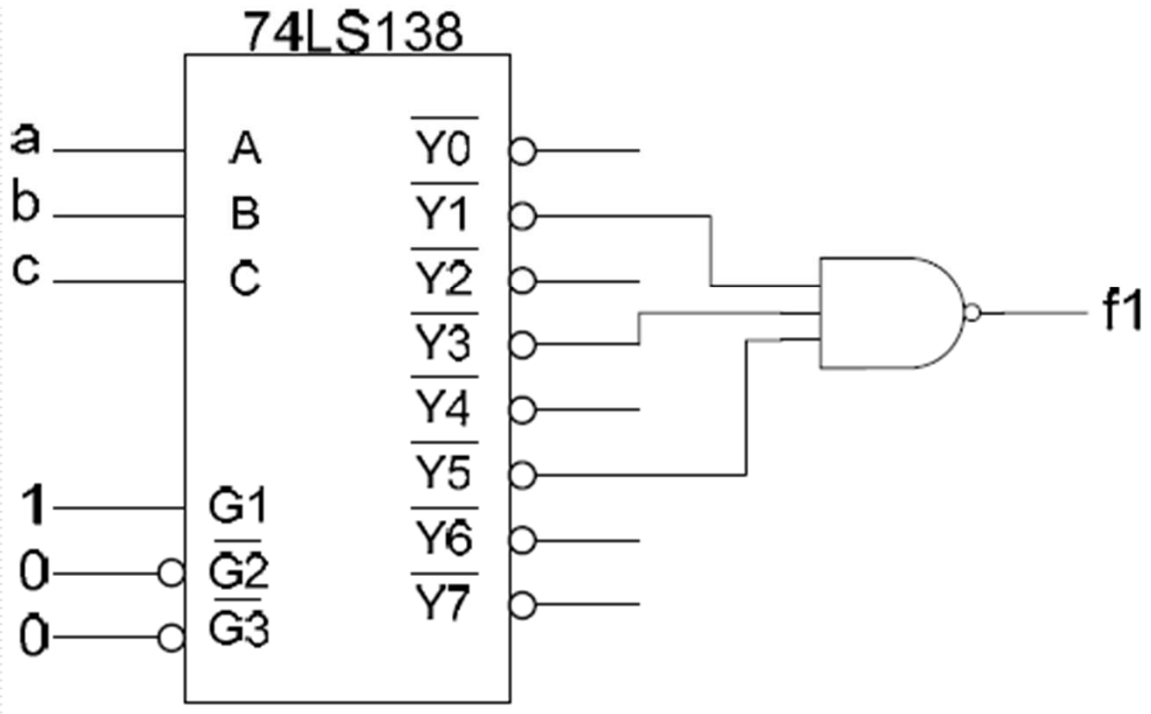
14LS42: Decodificator 4-la-10



A	B	C	B	1	2	3	4	5	6	7	8	9	10
0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	0	1		1	1
0	1	1	1	1	1	1	1	1	1	0		1	1
1	0	0	0	1	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Sinteza funcțiilor logice folosind decodificatoare

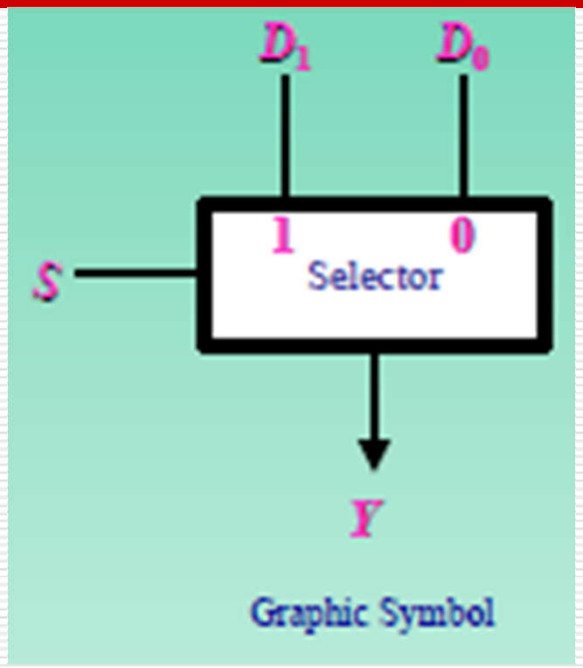
Să se implementeze cu ajutorul unui decodificator 74LS138 funcția logică $f1(a,b,c) = \sum(1,3,5)$



Multiplexor(Selector)

- Multiplexorul este un circuit logic combinaţional ce conectează ieşirea acestuia la una din cele *n* intrări.
- Selecţia uneia din cele n intrări se face cu ajutorul a $log_2 n$ intrări de selecţie.
- Poate fi privit ca un comutator digital.
- Este folosit pt.selecția unei singure surse de date din mai multe.

MUX 2-la-1

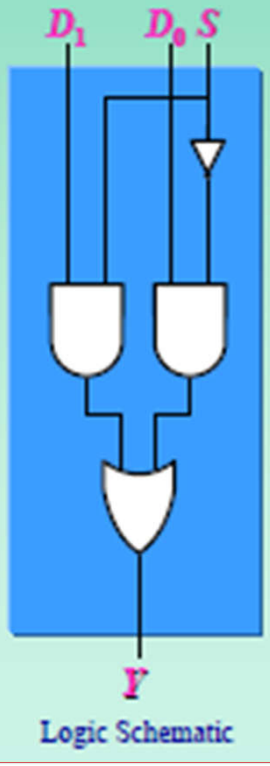


$$Y = S'D_0 + SD_1$$

Boolean Expression

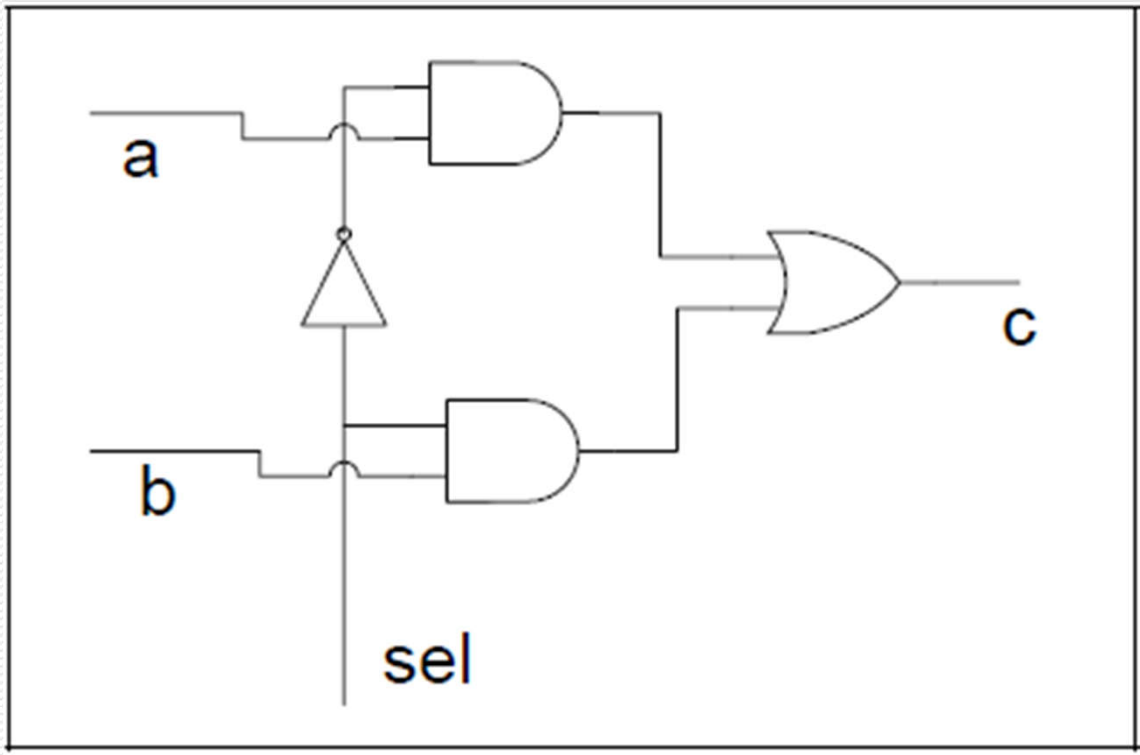
S	Y
0	D_0
1	D_1

Truth Table



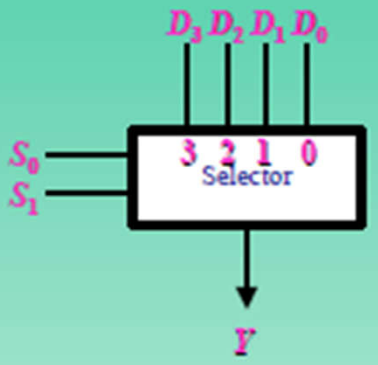
Logic Schematic

MUX 2-la-1



a	b	sel	c
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

MUX 4-la-1



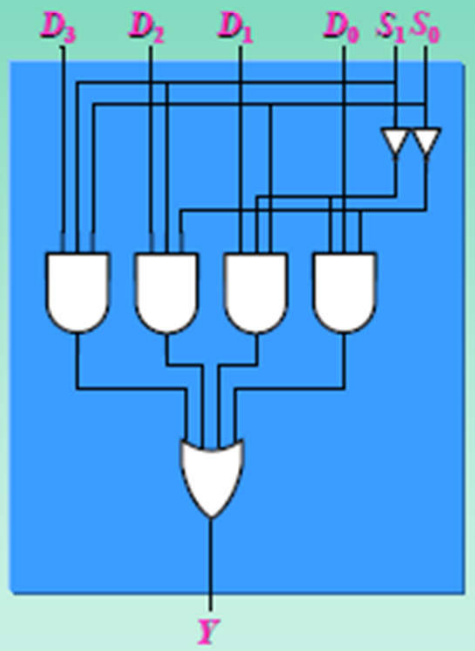
Graphic Symbol

$$Y = S'_1 S'_0 D_0 + S'_1 S_0 D_1 + S_1 S'_0 D_2 + S_1 S_0 D_3$$

Boolean Expression

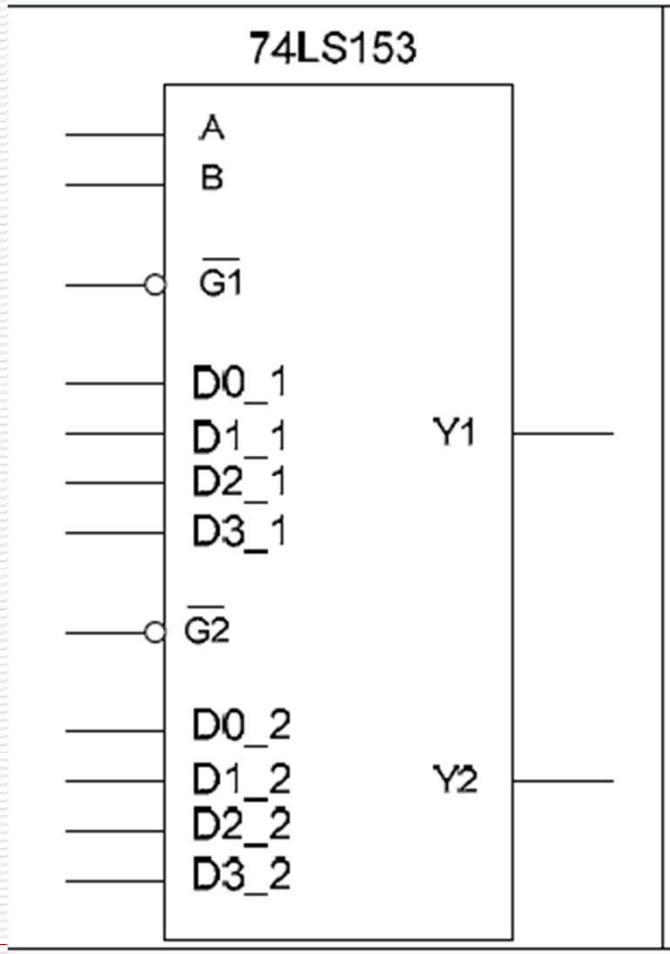
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Truth Table



Logic Schematic

74LS153: MUX 4-la-1

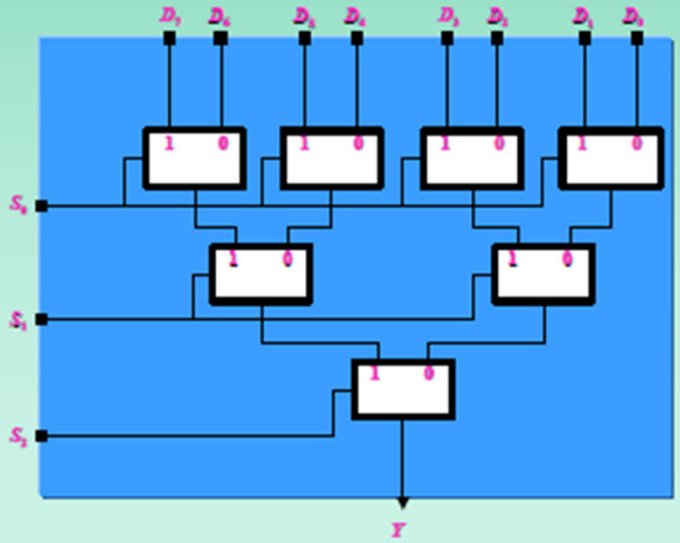


A	B	G1	G2	Y1	Y2
x	x	1	1	0	0
0	0	0	0	D0_1	D0_2
0	0	1	0	0	D0_2
0	0	0	1	D0_1	0
0	1	0	0	D1_1	D1_2
0	1	0	1	0	D1_2
0	1	1	0	D1_1	0
1	0	0	0	D2_1	D2_2
1	0	0	1	0	D2_2
1	0	1	0	D2_1	0
1	1	0	0	D3_1	D3_2
1	1	0	1	0	D3_2
1	1	1	0	D3_1	0

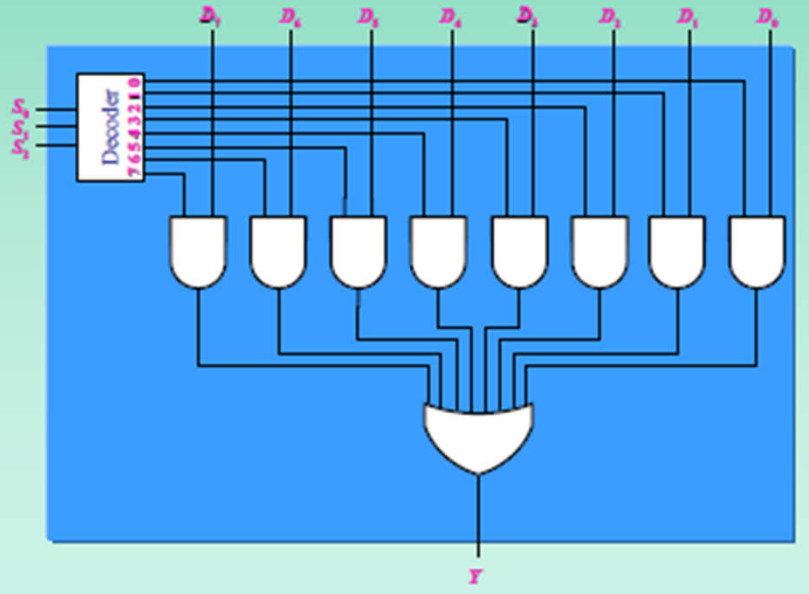
MUX 8-la-1

S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Truth Table

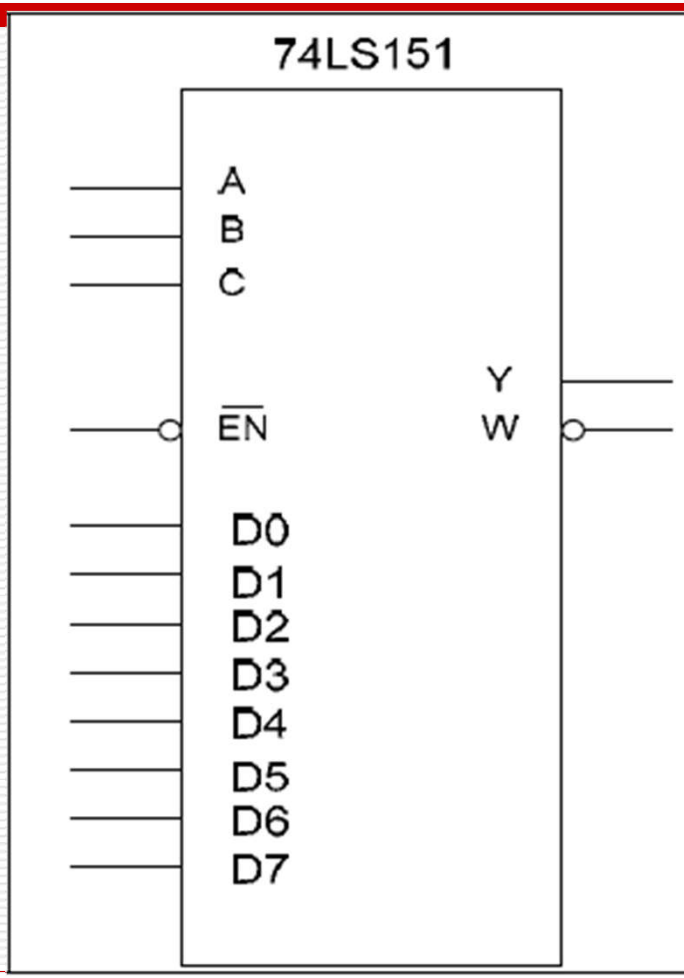


Implementation with 2-to-1 Selectors



Implementation with 3-to-8 Decoder

74LS151: MUX 8-la-1



A	B	C	EN	Y
x	x	x	1	0
0	0	0	0	D0
0	0	1	0	D1
0	1	0	0	D2
0	1	1	0	D3
1	0	0	0	D4
1	0	1	0	D5
1	1	0	0	D5
1	1	1	0	D7

Întrebări?

Enough Talking Let's Get To It
!!Brace Yourselves!!