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Logică digitală

-Curs 1-

INTRODUCERE

Oana Boncalo

B522

Bine ati venit la cursul de LD!

Personal didactic:

Curs: Oana Boncalo

Laborator: Sergiu Nimara, Alexandru Amaricai, Marian Ionascu, Cristian Vasiliu, Bogdan Mihailescu

Orar:

Curs: vineri 10-12

Laborator: luni: 8-10, 10-12: Alexandru;
miercuri: 8-10,10-12, 12-14: Oana;
joi: 8-10, 10-12:Bogdan;
12-14,14-16: Sergiu;
vineri:12-14, 14-16, 16-18: Marian;

De ce sunteti aici?

- Motive evidente
  - Curs obligatoriu
  - Necesar pentru toata ramura de HW/embedded
  - Notiuni care vizeaza toate dispozitivele moderne
    - Constructia componentelor complexe din componente mai simple
    - O alta perspectiva a ceea ce este un calculator

De ce sunteti aici?

- Motivele cele mai importante:
  - Conceptul de paralelism inerent pe care il prezinta HW-ul;
    prima expunere la ceea ce inseamna calcul paralel
  - Ofera o paradigma complementara design-ului si proiectarii software;
    folositor pentru a intelege ce conceptul de computatie

Ce veti invata la acest curs?

- Limbaje si concepte pentru proiectarea HW
  - Algebra booleana, minimizari logice, stare, timp, tool-uri CAD
  - Conceptul de stare in sistemele digitale
  - Analogie cu variablile si programe din SW
- Specificarea/compilarea/simularea design-urilor
- Analogie cu design-ul SW

Ce veti invata la acest curs?

- Limbaje si concepte pentru proiectarea HW
- Specificarea/compilarea/simularea design-urilor
  - Limbaje de descriere HW
  - Tool-uri de simulare pentru verificare
  - Copilatoare logice pentru sinteza blocurilor HW din design-ul nostru
  - Mapare
- Analogie cu design-ul SW

Ce veti invata la acest curs?

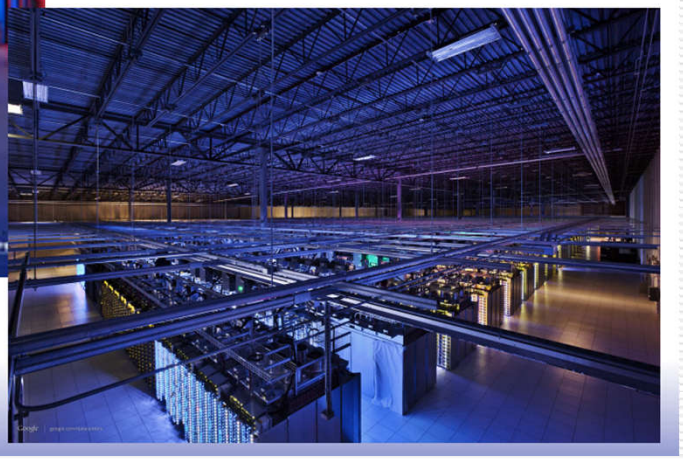
- Limbaje si concepte pentru proiectarea HW
- Specificarea/compilarea/simularea design-urilor
- Analogie cu design-ul SW
  - Amandoua mapeaza probleme bine intelese/specificate pe dispozitive
  - Amandoua trebuie sa functioneze corect…pretul platit pentru matematici discrete

Applicatii ale design-ului digital

Src: Berkley, EECS 151/251A Spring 2021

Applicatii ale design-ului digital

And then plenty more ...



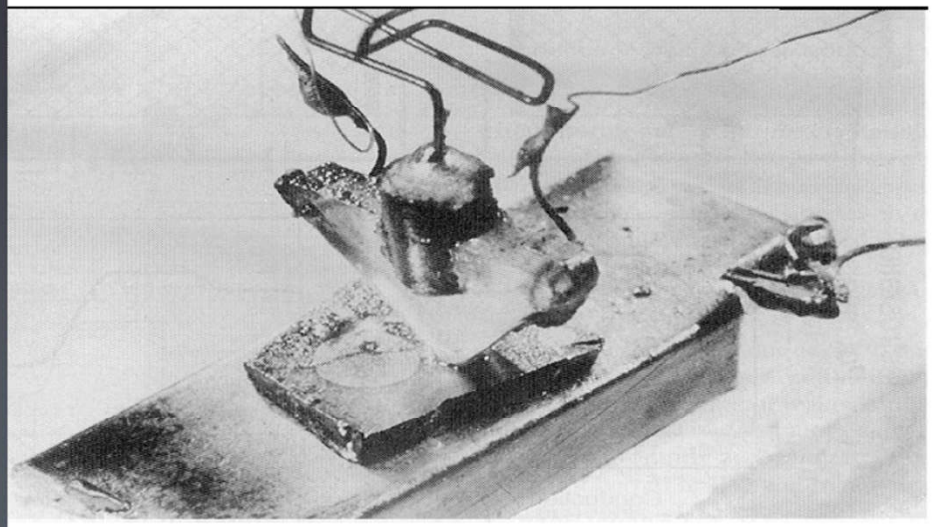
Src: Berkley, EECS 151/251A Spring 2021

O scurta incursiune istorica

- 1850: George Boole inventeaza algebra Booleana
  - Mapare propozitii logica in simboluri
  - Permite manipularea propoz.logice folosind instrumente matematice
- 1938: Claude Shannon face legatura intre algebra bool si dispozitive fizice (switch-uri/comutatoare)
  - Teza de master
- 1945: John von Neumann dezvolta primul program salvat in memorie
  - Tuburi vidate (un pas important de la relee electromagnetice)
- 1946: ENIAC—primul calculator electronic
  - 18,000 tuburi vidate
  - Cateva sute de inmultiri pe minut
- 1947: Shockley, Brittain, and Bardeen inventeaza tranzistorul
  - Permite integrarea mai multor dispozitive pe acelasi cip
  - Poarta catre electronica moderna

De unde a inceput totul …

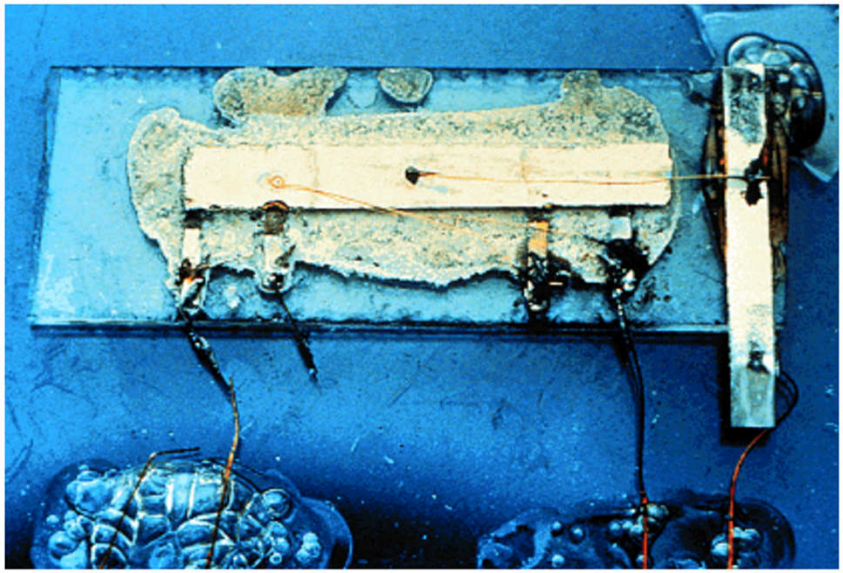
The Transistor Revolution



First transistor
Bell Labs, Dec 1947

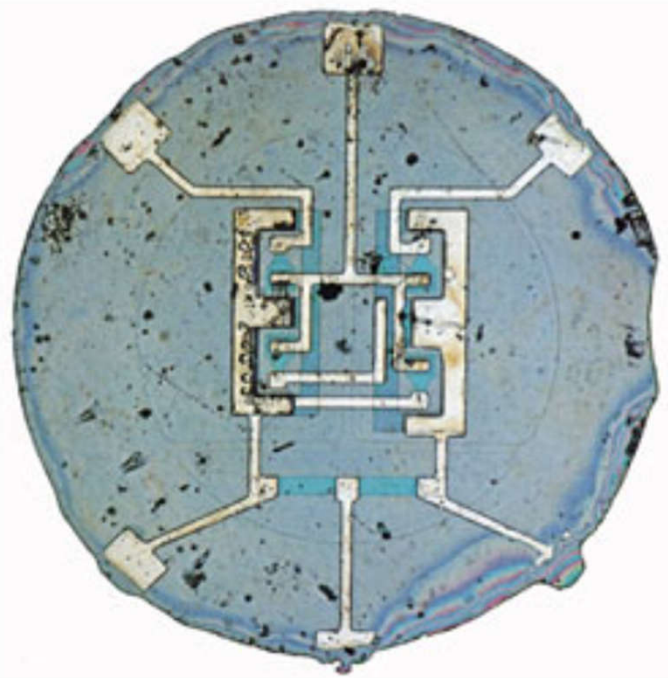
Src: Berkley, EECS 151/251A Spring 2021

Primul circuit integrat …



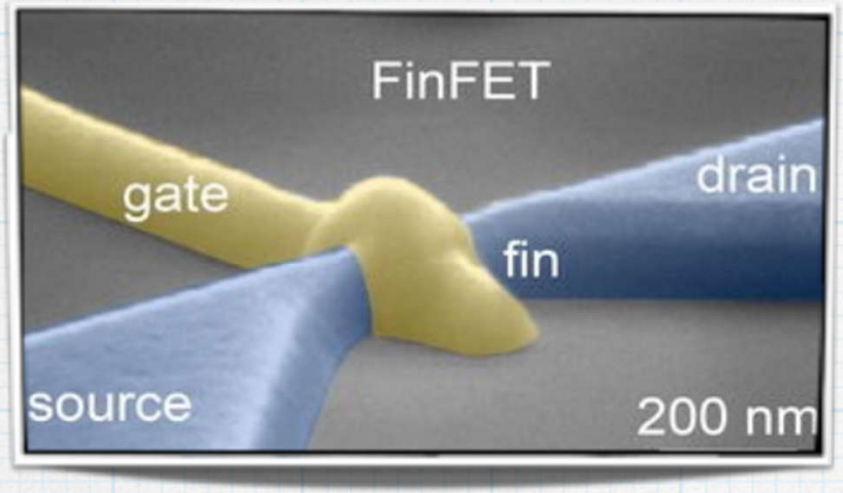
Jack Kilby, Texas Instruments

Bob Noyce, Fairchild



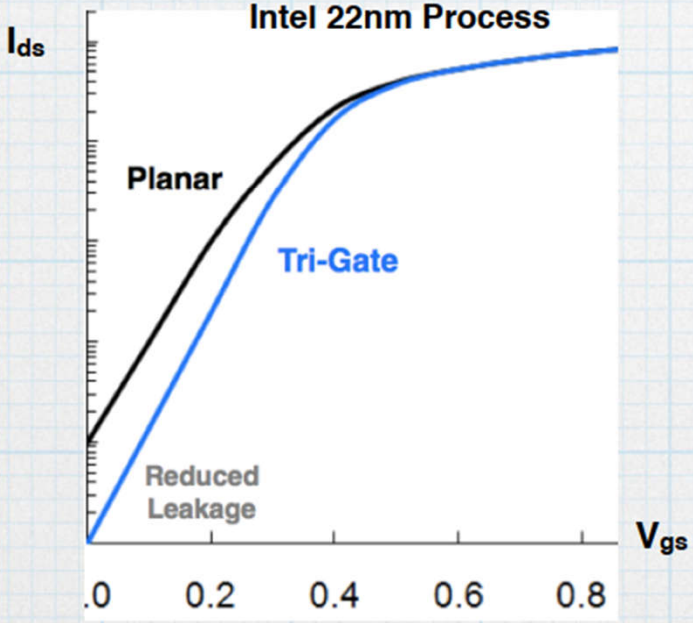
Src: Berkley, EECS 151/251A Spring 2021

Latest Modern Process



Transistor channel is a raised fin.

Gate controls channel from sides and top.



(12) **United States Patent**
Hu et al. Filed: **Oct. 23, 2000**

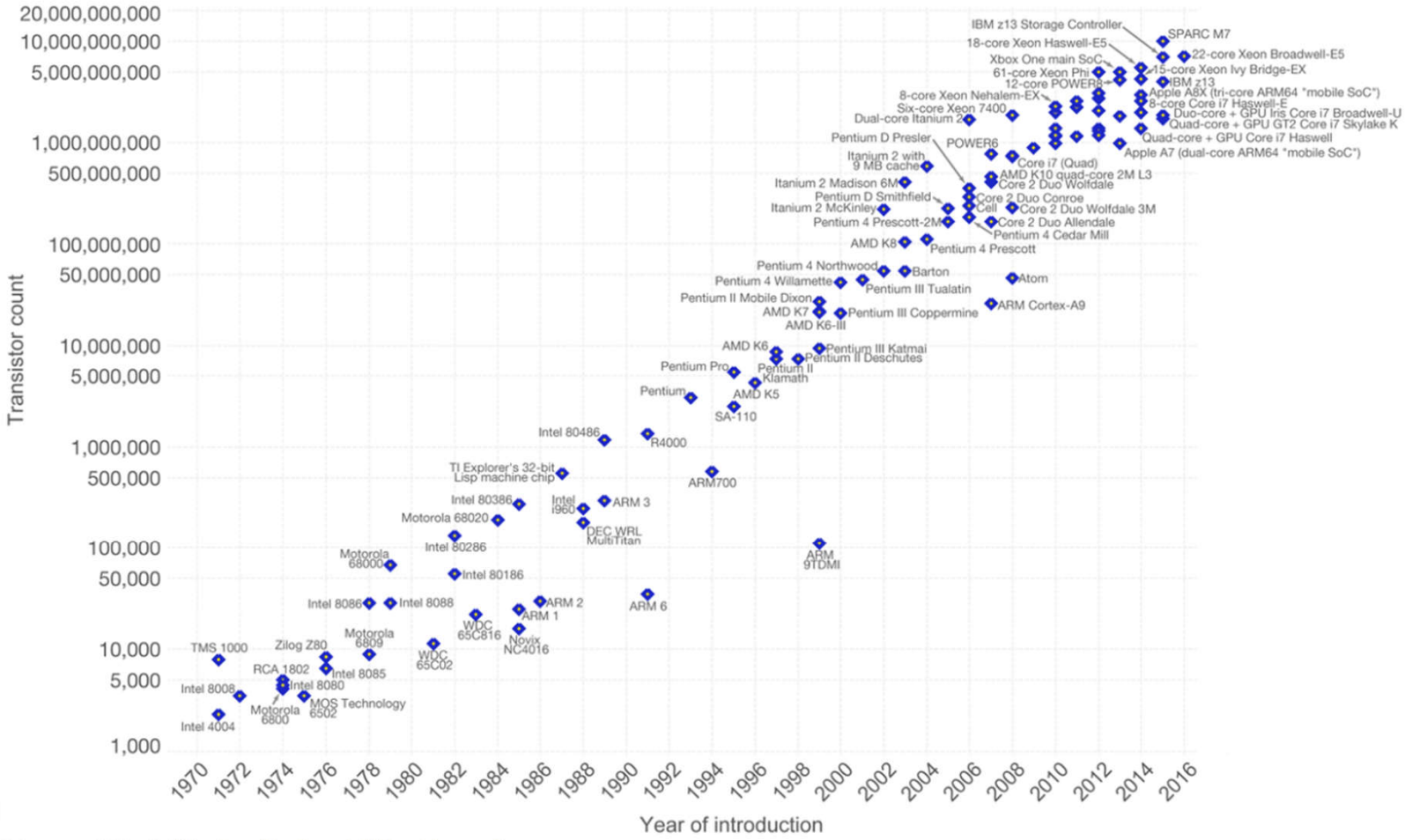
(54) **FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE**

(75) Inventors: **Chenming Hu**, Alamo; **Tsu-Jae King**, Fremont; **Vivek Subramanian**, Redwood City; **Leland Chang**, Berkeley; **Xuejue Huang**; **Yang-Kyu Choi**, both of Albany; **Jakub Tadeusz Kedzierski**, Hayward; **Nick Lindert**, Berkeley; **Jeffrey Bokor**, Oakland, all of CA (US); **Wen-Chin Lee**, Beaverton, OR (US)

Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Our World in Data

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.

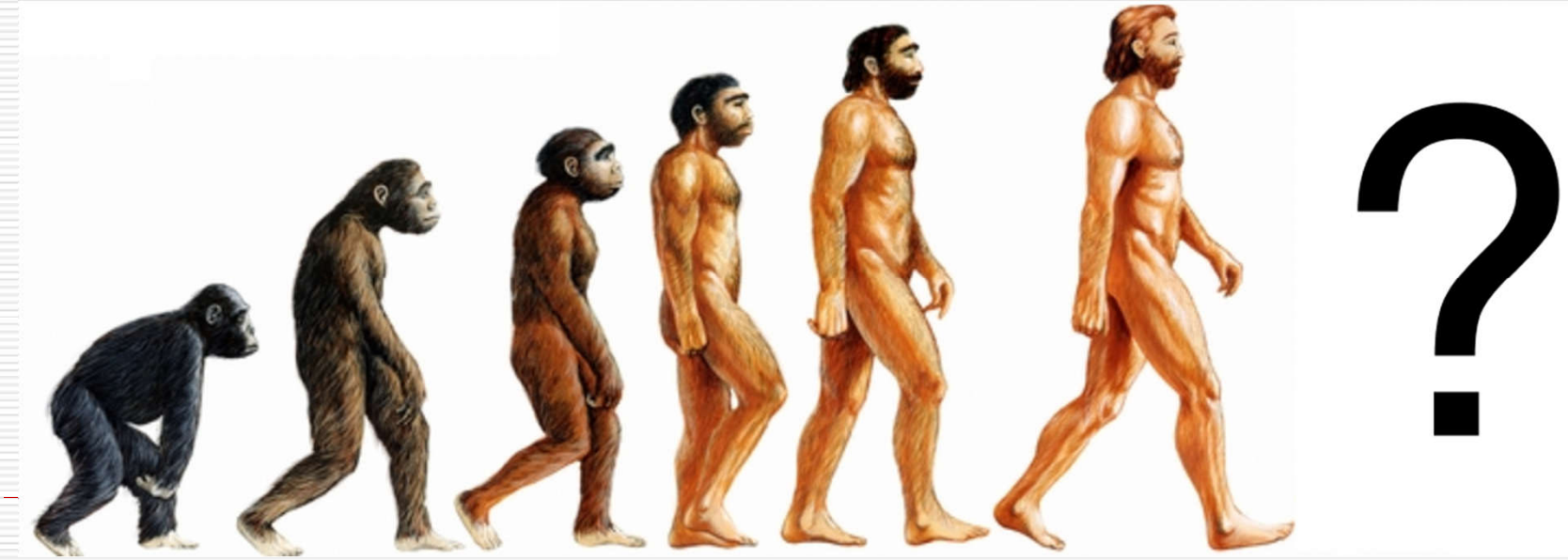


Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)

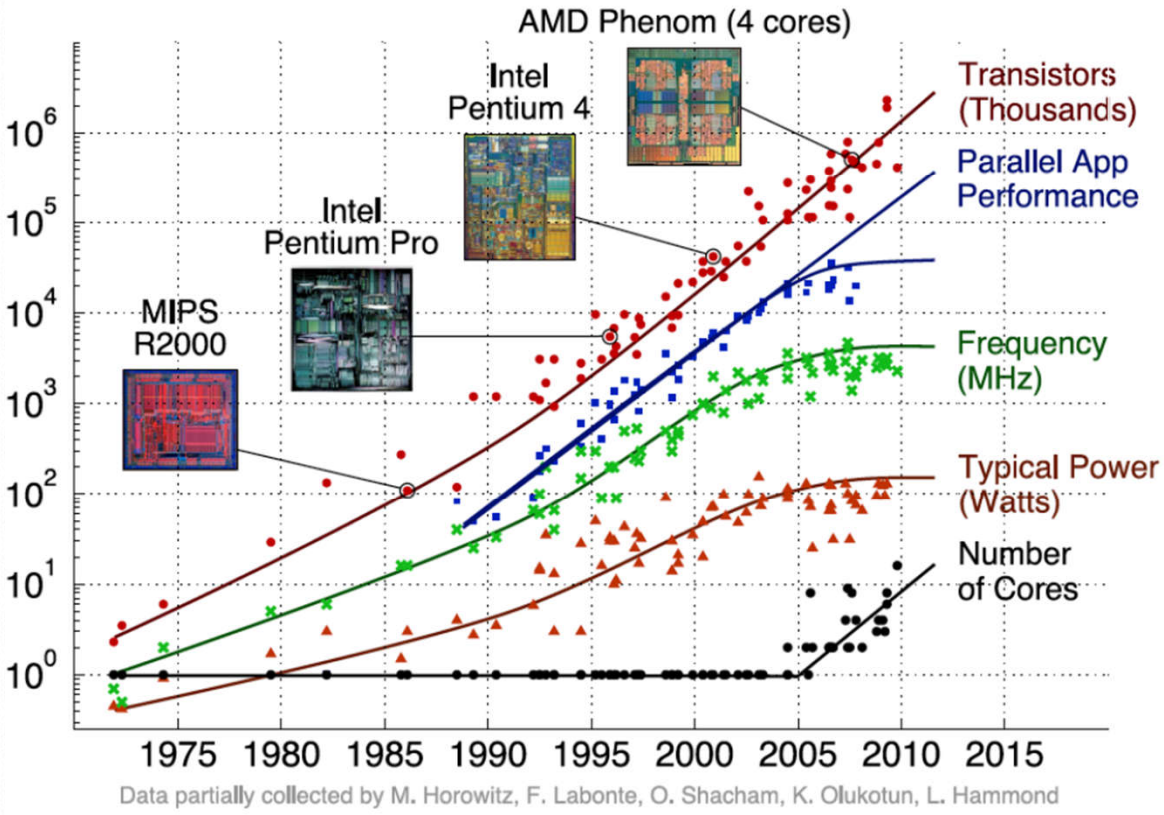
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Power becomes the key constraint

- For humans, Moore's Law scaling of the brain has ended a long time ago
  - Number of neurons and their firing rate did not change significantly
    - Remarkable advancement of civilization via **specialization**

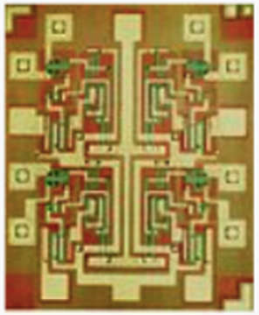


Power and Performance Trends



For reasons of power efficiency, performance scaling now comes from multiple cores and "accelerators", not from higher clock frequency.

Semiconductor manufacturing processes



10 μm – 1971
6 μm – 1974
3 μm – 1977
1.5 μm – 1982
1 μm – 1985
800 nm – 1989
600 nm – 1994
350 nm – 1995
250 nm – 1997
180 nm – 1999
130 nm – 2001
90 nm – 2004
65 nm – 2006
45 nm – 2008
32 nm – 2010
22 nm – 2012
14 nm – 2014
10 nm – 2017
7 nm – 2018
5 nm – *~2020*

State of the Art

7nm

As of September 2018, mass production of 7 nm devices has begun. The first mainstream 7 nm mobile processor intended for mass market use, the Apple A12 Bionic, was released at their September 2018 event. Although Huawei announced its own 7 nm processor before the Apple A12 Bionic, the Kirin 980 on August 31, 2018, the Apple A12 Bionic was released for public, mass market use to consumers before the Kirin 980. Both chips are manufactured by TSMC. AMD is currently working on their "Rome" workstation processors, which are based on the 7 nanometer node and feature up to 64 cores.

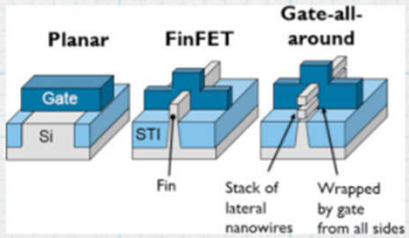
5nm

The 5 nm node was once assumed by some experts to be the end of Moore's law. Transistors smaller than 7 nm will experience quantum tunnelling through the gate oxide layer. Due to the costs involved in development, 5 nm is predicted to take longer to reach market than the two years estimated by Moore's law. Beyond 7 nm, it was initially claimed that major technological advances would have to be made to produce chips at this small scale. In particular, it is believed that 5 nm may usher in the successor to the FinFET, such as a gate-all-around architecture.

Although Intel has not yet revealed any specific plans to manufacturers or retailers, their 2009 roadmap projected an end-user release by approximately 2020. In early 2017, Samsung announced production of a 4 nm node by 2020 as part of its revised roadmap. On January 26th 2018, TSMC announced production of a 5 nm node by 2020 on its new fab 18. In October 2018, TSMC disclosed plans to start risk production of 5 nm devices in April 2019.

3.5nm

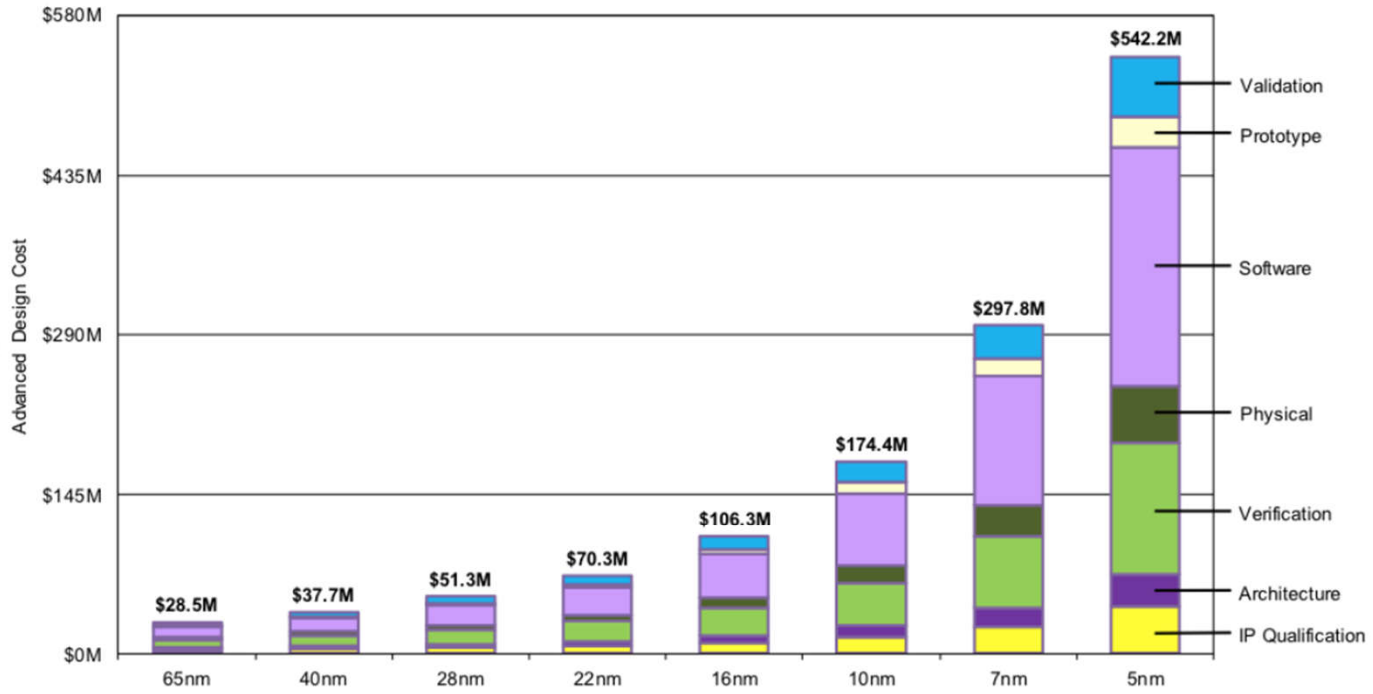
3.5 nm is a name for the first node beyond 5 nm. In 2018, IMEC and Cadence had taped out 3 nm test chips. Also, Samsung announced that they plan to use Gate-All-Around technology to produce 3 nm FETs in 2021.



* From Wikipedia

14/16→7 costul ≈ s-a dublat
7→5 costul ≈ s-a dublat

Cost Of Developing New Products



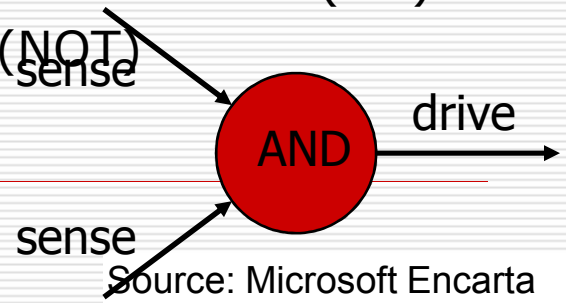
- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product

What is logic design?

- What is design?
  - Given a specification of a problem, come up with a way of solving it choosing appropriately from a collection of available components
  - While meeting some criteria for size, cost, power, beauty, elegance, etc.
- What is logic design?
  - Determining the collection of digital logic components to perform a specified control and/or data manipulation and/or communication function and the interconnections between them
  - Which logic components to choose? – there are many implementation technologies (e.g., off-the-shelf fixed-function components, programmable devices, transistors on a chip, etc.)
  - The design may need to be optimized and/or transformed to meet design constraints

What is digital hardware?

- Collection of devices that sense and/or control wires carrying a digital value (i.e., a physical quantity interpreted as a "0" or "1")
  - e.g., digital logic where voltage < 0.8v is a "0" and > 2.0v is a "1"
  - e.g., pair of transmission wires where a "0" or "1" is distinguished by which wire has a higher voltage (differential)
  - e.g., orientation of magnetization signifies a "0" or a "1"
- Primitive digital hardware devices
  - Logic computation devices (sense and drive)
    - two wires both "1" - make another be "1" (AND)
    - at least one of two wires "1" - make another be "1" (OR)
    - a wire "1" - then make another be "0" (NOT)
  - Memory devices (store)
    - store a value
    - recall a value previously stored



Source: Microsoft Encarta

Prezentare curs

Curs 1. Introducere în Design-ul Digital

Reprezentarea unui design; Niveluri de abstractizare; Procesul aferent unui design; Programe CAD

Curs 2-3. Tipuri de date și reprezentarea lor în sistemele de calcul

Sisteme de numerație pozitionale; Sisteme de numerație: binar, octal, hexazecimal; Reprezentarea numerelor binare în sistemele de calcul; Reprezentarea numerelor de virgulă flotantă; Coduri binare pentru numere zecimale

Prezentare curs

Curs 4-5. Algebra Booleană și logica digitală

Axiomele și teoremele algebrei booleene; Funcții booleene; Forma canonică; Forma standard; Porți logice; Aspecte legate de implementarea portilor logice;

Curs 6-7. Simplificarea funcțiilor booleene

Metoda hărților Karnaugh; Metoda tabulară Quine McCluskey; Sinteza funcțiilor folosind biblioteci standard de porți; Hazardul în design-ul digital;

Prezentare curs

Curs 8-9. Circuite combinaționale

Sumatoare; Multiplexoare; Demultiplexoare; Magistrale; Unități logice: Unitate Aritmetică-logică; Circuite combinaționale mai complexe;

Curs 10-12. Circuite secvențiale

Clasificarea circuitelor secvențiale; Elemente de memorare asincrone: tabelul caracteristic, tabelul excitațiilor, și ecuația de stare; Elemente de memorare sincrone: tabelul caracteristic, tabelul excitațiilor, și ecuația de stare; Analiza circuitelor secvențiale; Sinteza circuitelor secvențiale;

Prezentare curs

Curs 13. Componente pentru memorare

Registre; Numărătoare; Pila de registre; Stiva

Curs 14. Automate cu Stari Finite

Diagrame ASM; Sinteza circuitelor secvențiale folosind diagrame ASM;

Textbooks & resources

- https://sites.google.com/site/logicadigitala/home/couse
- John F. Wakerly „Digital Design: Principles and Practices”, 3rd Edition, Prentice Hall, 2000
- Daniel D. Gajski „Principles of Digital Design”, Prentice Hall, 1997
- http://store.digilentinc.com/
- http://www.testbench.in/;

Lucrări laborator

Lucrarea 1. FOLOSIREA CAD-URILOR XILINX ISE

Lucrarea 2. IMPLEMENTAREA UNUI CIRCUIT ÎN DISPOZITIVE FPGA

Lucrarea 3. IMPLEMENTAREA CIRCUITELOR COMBINAŢIONALE ÎN LIMBAJUL VERILOG HDL

Lucrări laborator

- **Lucrarea 4**. MINIMIZAREA FUNCŢIILOR LOGICE.

- **Lucrarea 5-6**. IMPLEMENTAREA DECODIFICATORULUI PENTRU AFIŞAJUL CU 7 SEGMENTE .

Lucrări laborator

- **Lucrarea 7**. IMPLEMENTAREA CIRCUITELOR DE DEPLASARE BARREL SHIFTER .
- **Lucrarea 8-9**. CIRCUITE SECVENŢIALE .
- **Lucrarea 10-11**. AUTOMATE CU STARI FINITE.

O prima concluzie
Logica digitala este despre:

- **Introduction to digital integrated circuit and system engineering**
  - Key concepts needed to be a good digital designer
  - Discover you own creativity!
- **Learn models that allow reasoning about design**
  - Manage design complexity through abstraction and understanding of tools
  - Allow analysis and optimization of the circuit's performance, power, cost, etc.
- **Learn how to make sure your circuit and system works**
  - *Do you want your block to be the one that screws up a 1 billion transistor chip?*

Digital design is not a spectator sport!
Learn by doing.

Notare

- 60 % Examen:
  - Întrebări de punctuale
  - Aplicații – problem solving
- 40 % Activitate pe parcurs:
  - 2-4 Quiz-uri
  - realizarea sarcinilor de laborator – 2,3,… lucrari neanuntate + Grad realizare sarcini laborator - validate prin interviu
  - ***Nota in cazul nepregatirii materialelor cerute pt lab respectiv este 0!!!!***

Copiat/Plagiat/Cheating policy

- Daca predai munca sau parti din munca altcuiva esti vinovat de frauda. Acest lucru se aplica la orice material de laborator, examen, cerinta predata, etc.
- Esti vinovat daca ajuti pe cineva sa triseze!
- E OK sa colaborezi si sa schimbi idei!
- Nu postati materiale predate/solutii public!
- La laborator problemele de copiat si colaborare prost inteleasa pot primi puncte NEGATIVE!
- La examen – picat cu referat in vederea exmatricularii!
- Toate cazurile sa aleg cu referat la decanat!