High Time Resolution Mirror Langmuir Probe Diagnostics for Transient Plasma Measurements in the MUSE Stellarator

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Abstract

Accurate and time-resolved measurements of plasma parameters are critical for understanding the dynamics of magnetic confinement devices. In the MUSE compact stellarator, the need for precise diagnostics is addressed using a high-time-resolution system based on the Mirror Langmuir Probe (MLP). Unlike conventional Langmuir probes, which sweep across a wide range of bias voltages, the MLP rapidly cycles through pre-selected voltages to extract electron temperature (T_e), electron density (n_e), and floating potential (V_f) from a single probe tip. This rapid cycling enables spatially and temporally localized measurements, essential for studying transient events in the core, edge, and scrape-off layer (SOL) regions.

The MLP system was implemented using a field-programmable gate array (FPGA), following the approach described by Vincent et al. [1]. During this internship project, the focus was on ensuring robust control and data acquisition software, diagnosing and resolving errors, and rebuilding the code within a Linux virtual machine using the Koheron make system. The FPGA implementation was subsequently deployed to hardware, and the system was integrated into the MUSE experimental platform. These efforts establish a foundation for high-fidelity measurements of transient plasma dynamics and demonstrate the feasibility of FPGA-based, high-speed diagnostics in stellarator research.

1 Introduction

Magnetic confinement fusion devices, including stellarators, require precise diagnostics to understand plasma behavior, confinement, and transport processes. Accurate measurements of transient events are crucial for developing predictive models of plasma performance and improving operational strategies for stellarators.

The MUSE stellarator is a compact experimental device designed to explore the physics of magnetically confined plasmas in complex three-dimensional geometries [11,12]. Its compact size and limited diagnostic ports necessitate compact, high-speed instrumentation capable of resolving both spatial and temporal variations in plasma. Traditional Langmuir probes, while widely used for localized measurements of electron temperature, density, and floating potential, rely on sweeping the bias voltage across a range to generate current-voltage (I–V) characteristics [3, 4]. While effective for steady-state or slowly varying plasmas, these probes are limited in temporal resolution, typically unable to capture fast fluctuations that occur on microsecond timescales.

Mirror Langmuir Probes (MLPs) overcome these limitations by rapidly cycling through a set of pre-selected bias voltages, targeting regions of the I–V curve corresponding to specific plasma parameters [1, 2, 9, 10]. This approach allows a single probe tip to extract electron temperature, electron density, and floating potential with high temporal and spatial resolution, making it suitable for observing transient phenomena. High-speed data acquisition and FPGA-based control systems further enhance the capability to resolve microsecond-scale dynamics.

The present work focuses on the implementation and integration of a high-speed MLP system in the MUSE stellarator. The primary objectives were to deploy FPGA-based control, stabilize the control software within a Linux environment using the Koheron make system, debug errors, and integrate the MLP into the MUSE experimental platform. These efforts aim to enable reliable, time-resolved plasma measurements and contribute to the broader understanding of transient events in stellarator plasmas.

2 Theory of the Mirror Langmuir Probe

A Langmuir probe determines plasma parameters by applying a controllable bias voltage V to a small conductive tip inserted into the plasma and measuring the resulting current I [3, 4]. By varying the probe potential relative to the plasma potential V_p, the probe samples different regions of the current–voltage (I–V) characteristic, each of which carries information about the electron temperature T_e, electron density n_e, and floating potential V_f.

When the probe is biased strongly negative with respect to the plasma, electrons are repelled and the probe collects an ion saturation current I_{sat} that depends primarily on the ion flux to the probe surface. Conversely, at sufficiently positive bias electrons dominate the collected current (electron saturation regime). At an intermediate potential, called the floating potential V_f, the electron and ion currents balance such that the net current to the probe is zero:

$$I(V_f) = 0. \tag{1}$$

For a Maxwellian plasma, the collected current can be related to the probe and plasma potentials through the classical Langmuir relation. The following algebraic rearrangements, used to extract I_{sat}, T_e, and V_f from discrete voltage measurements, follow the method described by Vincent et al. [1]:

$$I_{\mathrm{sat}} = \frac{I_{\mathrm{LP}}}{\exp\left(\dfrac{V_P - V_F}{T_e}\right) - 1}, \tag{2}$$

$$T_e = \frac{V_{pr} - V_F}{\ln\left(\dfrac{I_{LP}}{I_{sat}} + 1\right)}, \tag{3}$$

$$V_F = V_P - T_e \ln\left(\frac{I_{LP}}{I_{sat}} + 1\right), \tag{4}$$

where I_{LP} is the measured probe current at a given applied bias V_{pr}, V_P is the plasma potential, and T_e is expressed in electron volts.

Traditional swept Langmuir probes obtain these parameters by scanning V over a wide range and fitting the full I–V curve. Although accurate for steady plasmas, the sequential

sweep introduces averaging over the sweep duration, typically limiting temporal resolution to milliseconds and masking fast fluctuations.

The Mirror Langmuir Probe (MLP) overcomes this limitation by applying *discrete* bias voltages chosen to target key regions of the I–V [1, 2, 9]. Instead of a continuous sweep, the MLP rapidly cycles among three voltages:

- a strongly negative bias V_- (ion saturation region) to measure I_{sat},
- a near-floating bias V_F where $I(V_F) \approx 0$,
- and a positive bias V_+ (electron collection region) to measure the electron current.

These three current measurements provide independent points along the I–V characteristic. By inserting them into the Langmuir equations above, the electron temperature T_e, electron density n_e, and floating potential V_f can be determined without a full voltage sweep. Because the bias sequence can be cycled at rates of several hundred kilohertz, the MLP enables microsecond-resolution measurements of transient plasma events.

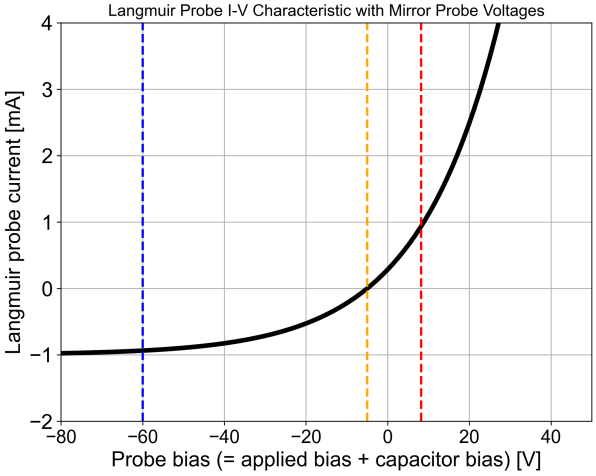

Figure 1: Idealized I–V curve of a Langmuir probe. The MLP applies three discrete voltages—ion saturation (V_-), floating potential (V_F), and electron collection (V_+)—to extract plasma parameters in real time.

3 Experimental Setup and FPGA Implementation

The MUSE stellarator has a minor plasma radius of approximately 0.075 m and a limited number of diagnostic access ports. These constraints necessitate compact, high-speed diagnostics capable of operating reliably under the influence of strong magnetic and electromagnetic fields.

The MLP system consists of a single-tip probe, a bias-switching module, a data acquisition system, and an FPGA-based control unit. The FPGA board used is a Red Pitaya Stemlab 125-14, which is capable of a master clock speed of 125 MHz, allowing for the desired temporal resolution. This board is equipped with two 14-bit analog-to-digital converters (ADCs), as well as two 14-bit digital-to-analog converters (DACs). All four SMA ports of the ADCs and DACs are utilized: the two ADC channels produce the voltage steps, which are scaled by a measured electron temperature calculation from the

previous cycle, while the two DAC channels serve distinct purposes—one forms a feedback loop to validate that the output signal leaving the system is correct, and the other receives the plasma current response from the probe. The plasma current is converted into a 0–1 V signal, which is digitized and processed by the FPGA for the calculation of electron temperature (T_e), electron density (n_e), and plasma potential (V_p).

The MLP device generates synchronized digital signals to control the probe bias voltages, cycling through pre-selected levels of

$$V_+ \approx T_e, \quad V_F = 0, \quad V_- \approx -3T_e$$

corresponding to the ion saturation (V_-), electron collection (V_+), and floating potential (V_F) regions of the I–V curve. The resulting currents are streamed to a host computer upon request from a Python script, allowing the FPGA to calculate T_e, n_e, and V_f in real time. This FPGA design enables microsecond-scale timing resolution and precise synchronization with other MUSE diagnostics.

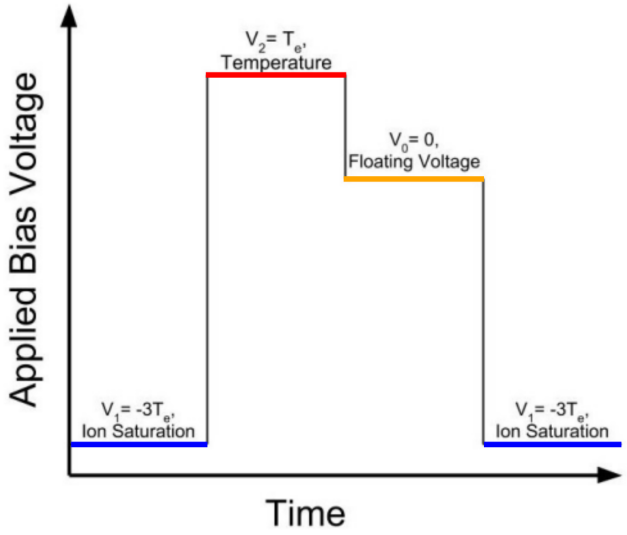

Figure 2: Discrete bias voltages applied by the MLP corresponding to specific regions of the I–V curve (adapted from Vincent et al. [1]).

4 MLP FPGA Program Overview and Functional Blocks

The FPGA design implements a closed-loop measurement and control system for plasma diagnostics using a Red Pitaya platform, based on the architecture described by Vincent [1]. The system is organized around synchronous data acquisition, real-time computation, and bias waveform generation. The design consists of several functional blocks that interact in a tightly coordinated pipeline.

4.1 ADCs and DACs (Red Pitaya ADC/DAC Core)

The system uses two ADC inputs and two DAC outputs, all synchronized to `adc_clk`:

- **ADC Inputs:**

  - `adc1` measures the plasma current.
  - `adc2` serves as a loopback/reference input.

- **DAC Outputs:**
  - Drive the probe to discrete voltage levels, generated in real time by the FPGA.

Both ADC channels sample simultaneously, and the DACs produce the bias waveform in phase with the acquisition.

4.2 Manual Calibration

The `Calibrate_PC` and `Calibrate_LB` modules perform per-channel linear corrections to align the ADC streams with the corresponding instruments:

- Each ADC stream is adjusted using an offset and scale parameter (`Scale_PC`/`Offset_PC` and `Scale_LB`/`Offset_LB`) stored in control registers.
- The output remains 14-bit and synchronized to `adc_clk`.

4.3 Moving Average Filters

Noise reduction is achieved via 32-tap moving average filters (`moving_average_PC` and `moving_average_LB`):

- Reset at the start of each acquisition to ensure reproducible phase alignment.
- Smoothed outputs are used by computation modules and for telemetry snapshots.

4.4 Set-Voltage Module

The `set_voltage` block generates the bias waveform and coordinates phase control:

- Computes three bias levels per period based on the most recent temperature estimate.
- Cycles through bias phases ($1 \rightarrow 2 \rightarrow 3$) and generates the corresponding DAC output.
- Produces phase enable strobes (`iSat_en`, `Temp_en`, `vFloat_en`) for compute modules.
- Issues `store_en` strobes to mark precise instants for data collection.

4.5 Sequential Operation of the Three Calculation Cores

The three processing cores operate sequentially during each bias period as follows:

Phase 1 — *iSat* (ion-saturation region). Inputs: smoothed `volt_in` (plasma current proxy), `volt1` (first bias level), and v_{Float}. A ratio related to the sheath model is formed:

$$\text{dividend} \approx (\texttt{volt1} - v_{\text{Float}}), \qquad \text{divisor} \approx \text{Temp}$$

with a fallback to $\text{Temp}_{\text{guess}}$ if zero. The divider outputs drive a BRAM LUT address encoding the nonlinearity of the Langmuir I–V characteristic in the ion-saturation region. The LUT output scales a captured signal to yield i_{Sat}. A `data_valid` flag is asserted.

Phase 2 — T_e (electron temperature). Inputs: i_{Sat} from Phase 1, smoothed `volt_in`, `volt2` (second bias level), and v_{Float}. The ratio for the electron-side slope is computed:

$$\text{divisor} \approx i_{\text{Sat}}, \qquad \text{dividend} \approx \texttt{volt\_in}$$

with a fallback to $i_{\text{Sat,guess}}$ if zero. The quantity $(\texttt{volt2} - V_F)$ is also captured as the instantaneous electron-side voltage excursion. Divider outputs index a BRAM LUT implementing the Langmuir exponential mapping; the LUT output multiplies the stored excursion to produce Temp. A `data_valid` flag is asserted.

Phase 3 — *vFloat* (floating potential). Inputs: i_{Sat}, smoothed `volt_in`, and the phase's bias reference. The ratio is formed as

$$\text{divisor} \approx i_{\text{Sat}}, \qquad \text{dividend} \approx \texttt{volt\_in}$$

(with fallback to $i_{\text{Sat,guess}}$ if zero). The divider results provide the LUT address, and the LUT output scales the signal to compute v_{Float}. A `data_valid` flag is asserted.

Final Integration. After all three phases are complete, the calculated values of I_{sat}, T_e, and V_F are combined by the supervisory logic. This integration stage fuses the ion-saturation current, electron temperature, and floating potential into a self-consistent solution of the Langmuir probe I–V relationship, providing the key plasma parameters required for diagnostics and control.

4.6 Acquire Trigger

The `acquire_trigger` block manages acquisition windows:

- Combines external and software triggers to assert `acquire_valid`.
- Generates `clear_pulse` to reset filters and compute modules at acquisition start.
- Maintains a rolling timestamp counter for telemetry synchronization.

4.7 Output Multiplexer

The `output_mux` selects between the dynamic bias waveform from `set_voltage` or a constant/debug value, which drives both DAC channels.

4.8 Data Collector

Telemetry is packaged in 32-bit frames via the `data_collector`:

- **Voltage snapshots:** captured when `store_en` is active, containing a tag, timestamp, and smoothed ADC values.
- **Computed results:** captured when a compute module asserts `data_valid`, containing parameter estimates and timestamp.
- The module arbitrates between pending voltage and compute frames, outputting `tdata` and `tvalid` on an AXI Stream.

4.9 Clock Domain Crossing and FIFO

The ADC-domain telemetry stream passes through:

- An AXI Stream clock converter to the processor domain.
- An AXI Memory-Mapped FIFO for buffering, allowing software to read frames at its own pace without losing data.

4.10 Control and Status Registers

These registers provide:

- Configuration inputs (triggers, acquisition length, calibration parameters).
- Live monitoring outputs (ADC taps, computed plasma parameters, timestamp).

4.11 Interconnection and Dataflow

1. **Acquisition Lifecycle:** A run begins when a trigger is received. `clear_pulse` synchronously resets filters, compute modules, and bias state machines, ensuring phase-aligned sampling, bias output, and computation from the first sample.
2. **Signal Conditioning:**
   - `adc1` $\rightarrow$ calibration $\rightarrow$ moving average $\rightarrow$ compute modules.
   - `adc2` $\rightarrow$ calibration $\rightarrow$ moving average $\rightarrow$ bias reference for computations.
3. **Computation Pipeline:** Each compute module processes smoothed inputs, performs LUT-based transformations, and asserts `data_valid`. Output is synchronized with the bias phase.
4. **Bias Generation and Phase Control:** `set_voltage` determines DAC output and asserts compute enable strobes. `store_en` strobes mark sampling instants for the data collector. The bias values are informed by the previous parameter computations.
5. **Data Collection:** `store_en` triggers voltage snapshots. Compute module `data_valid` triggers parameter frames. Frames are multiplexed into an AXI Stream, timestamped, and buffered via FIFO for software access.

6. **Software Access and Synchronization:** Processor reads frames from FIFO. Status registers expose live ADC values and parameter estimates. Trigger and reset logic ensures deterministic alignment of bias, computation, and telemetry.

4.12 Reverse Engineering and Development Challenges

During development, several significant challenges arose due to incomplete documentation:

- **Vivado Block Diagram Reconstruction:** Reverse engineering was necessary to rebuild the FPGA design and verify module interconnections.
- **Lack of System Explanation:** Limited comments and documentation required significant effort to understand the VHDL descriptions of different block-diagram cores and how they synchronize into a working system.
- **Software Environment Dependencies:** Correct Python versions and Linux dependencies were critical to ensure FPGA toolchain scripts ran successfully.
- **Duplicate Modules:** The GitHub repository contained multiple instances of some modules, confusing synthesis and simulation. Careful code inspection and removal of duplicates ensured proper module instantiation.

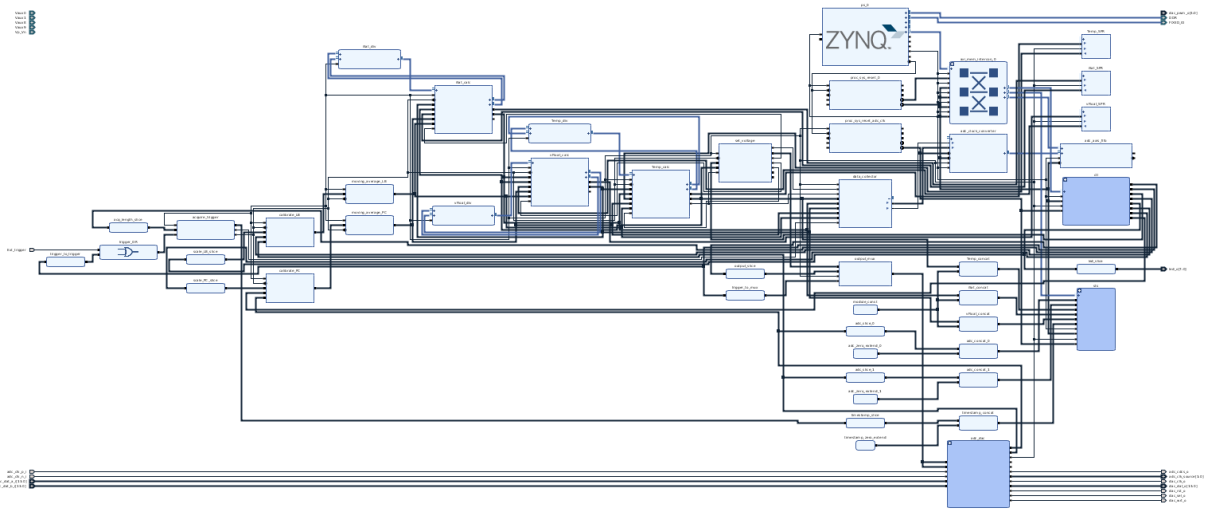

Figure 3: Block diagram of the FPGA implementation showing the custom IP cores, based on the design described by Vincent [1]. The design illustrates the interaction between data acquisition, parameter–calculation, and bias–control modules. Signal paths highlight how raw probe measurements are routed through filtering, divider logic, and BRAM-based lookup tables before producing key plasma parameters such as I_{Sat}, T_e, and V_F.

5 Deployment and Compilation of the FPGA Program

During this internship project, significant effort was devoted to software deployment and debugging. VHDL code was transferred to a Linux virtual machine, rebuilt using the Koheron make system with a Tool Command Language (TCL) script, and compiled with Vivado 2017.2.

Through this process, the FPGA program was rebuilt into a clean, phase-synchronized pipeline that integrates real-time acquisition, synchronous computation, and off-board streaming was achieved.

Data was streamed over the Ethernet port of the Red Pitaya, converted to the computer via a USB converter, and accessed using a static IP with a Python script that utilized the Koheron Python package to connect to the instrument.

To test the system, a dedicated test bench [1] was employed. This test bench uses a second Red Pitaya, referred to as the Plasma Current Response (PCR) unit, which accepts the bias voltage from the MLP Red Pitaya and outputs a simulated plasma response to validate that the MLP instrument is behaving correctly. A synchronized clock between the two Red Pitayas ensured accurate timing.

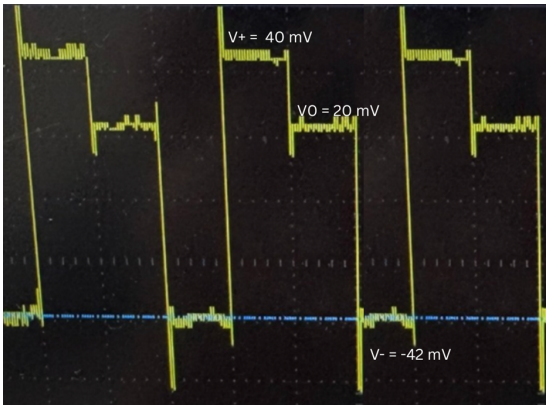

Figure 4: Measured probe bias waveform captured from the Red Pitaya output. The applied voltages closely follow the theoretical discrete levels shown in Fig. 2, confirming correct FPGA timing and amplitude control. The measured differences are $V^+ - V_0 \approx 20$ mV and $V^- - V_0 \approx -62$ mV. These results demonstrate that the device behaves as expected, following the relationship $V^+ = T_e$, $V_0 = 0$, and $V^- = -3T_e$.

6 Expected Results and Applications

The MLP system enables measurements of T_e and V_f in the core, edge, and SOL regions with high temporal resolution. Transient plasma phenomena, such as turbulence, blobs, and ELMs, can be characterized with microsecond accuracy.

For example, simulations of MUSE edge plasmas indicate electron temperature fluctuations of 5–10 eV on microsecond timescales. The MLP can resolve these fluctuations, allowing direct observation of filamentary structures, density bursts, and potential variations. Floating potential measurements enable estimation of local electric fields, which drive cross-field transport and influence confinement.

Compared to traditional swept probes, the MLP reduces averaging effects and captures transient events with higher fidelity. FPGA-based control also allows synchronization with other diagnostics, including magnetic probes and interferometers, enabling coordinated studies of plasma dynamics.

Potential applications include:

- Validation of gyrokinetic and fluid turbulence simulations
- Investigation of transport mechanisms in the SOL and edge regions
- Optimization of stellarator performance through feedback from real-time plasma diagnostics

7 Conclusion and Future Work

This internship project focused on the deployment of a high-time-resolution Mirror Langmuir Probe in the MUSE stellarator. Key accomplishments include:

1. Migration and stabilization of the control software within a Linux environment using the Koheron make system
2. FPGA deployment for rapid bias voltage cycling and real-time data acquisition

The resulting system will enable high-fidelity, time-resolved measurements of electron temperature, density, and floating potential in transient plasma environments. These measures will provide insight into turbulence, edge-localized modes, and other fast phenomena critical to confinement and transport studies.

Future work will focus on:

- Developing an analog front end to amplify Red Pitaya signals to an appropriate voltage with respect to the plasma potential.
- Deployment of the MLP on the MUSE experiment.
- Calibration and experimental validation of the MLP system during MUSE plasma discharges.

A successful implementation of the MLP system on the MUSE compact stellarator will demonstrate the feasibility and importance of FPGA-based, high-speed diagnostics for stellarators and will provide a foundation for future studies of transient plasma phenomena in fusion research.

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