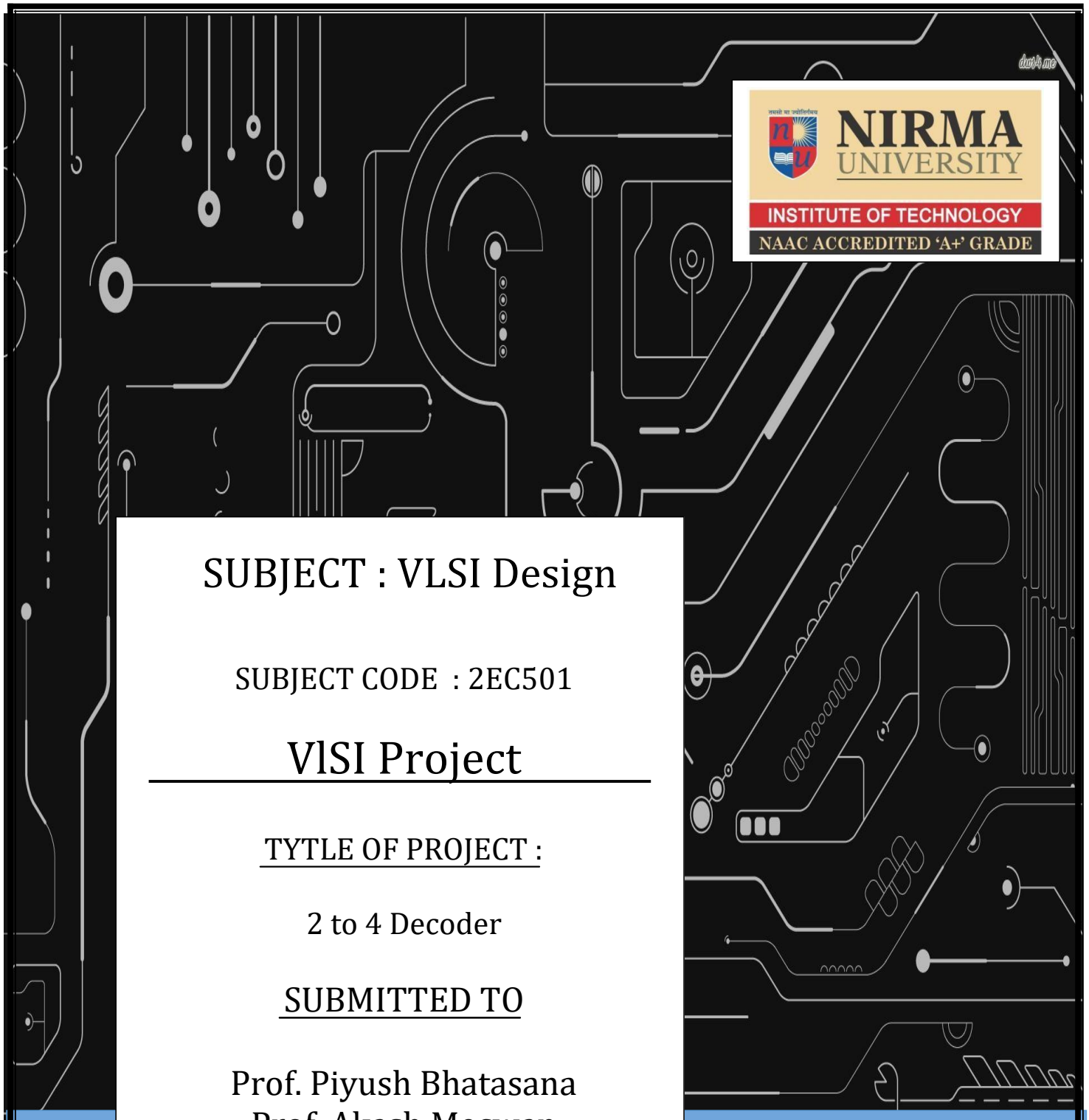

NIRMA UNIVERSITY
INSTITUTE OF TECHNOLOGY
NAAC ACCREDITED 'A+' GRADE

SUBJECT : VLSI Design

SUBJECT CODE : 2EC501

VlSI Project

TYTLE OF PROJECT :

2 to 4 Decoder

SUBMITTED TO

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Submitted By

BRIJESH PATEL (20BEC083)

❖ Abstract

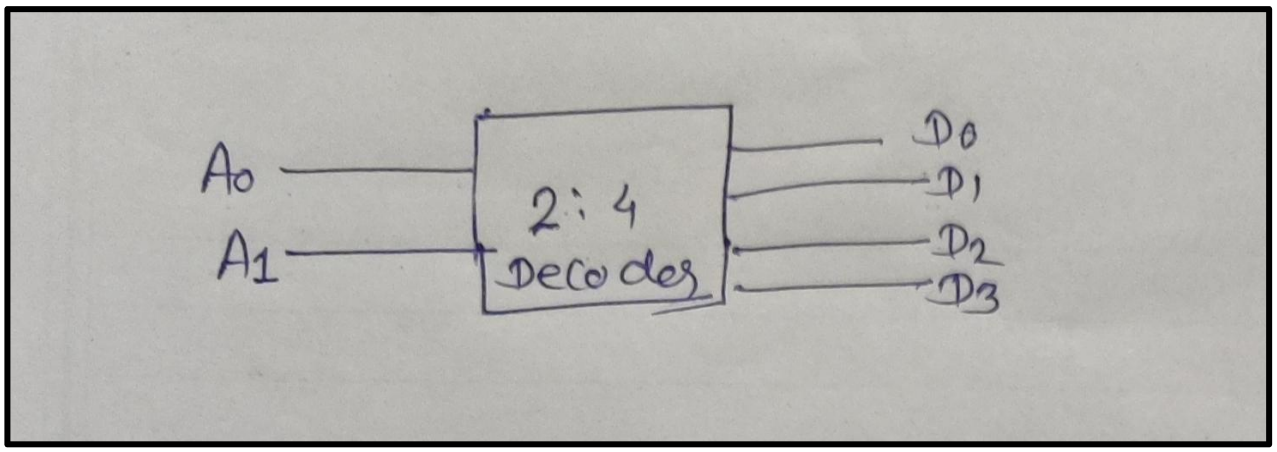
In this assignment, a static complementary metal-oxide semiconductor-based 2 to 4 bit decoder is introduced (CMOS). The gate level diagram is created using the Boolean Expression as a foundation, the truth table and gate level circuit of the decoder have first been presented. The Stick Diagram of the Circuit, which is derived from the CMOS Implementation Diagram, serves as the framework for the Microwind Design Layout. Microwind simulations at 120 nm demonstrate how the various observed parameters change depending on the input.

❖ INTRODUCTION TO LINE DECODERS

A decoder is a multiple-input, multiple-output logic circuit that changes coding from input to output, when the input and output codes are different. In most cases, the input code is less than the output code in terms of bits, and the words of the input code are mapped exactly onto the words of the output code.

❖ Binary decoder

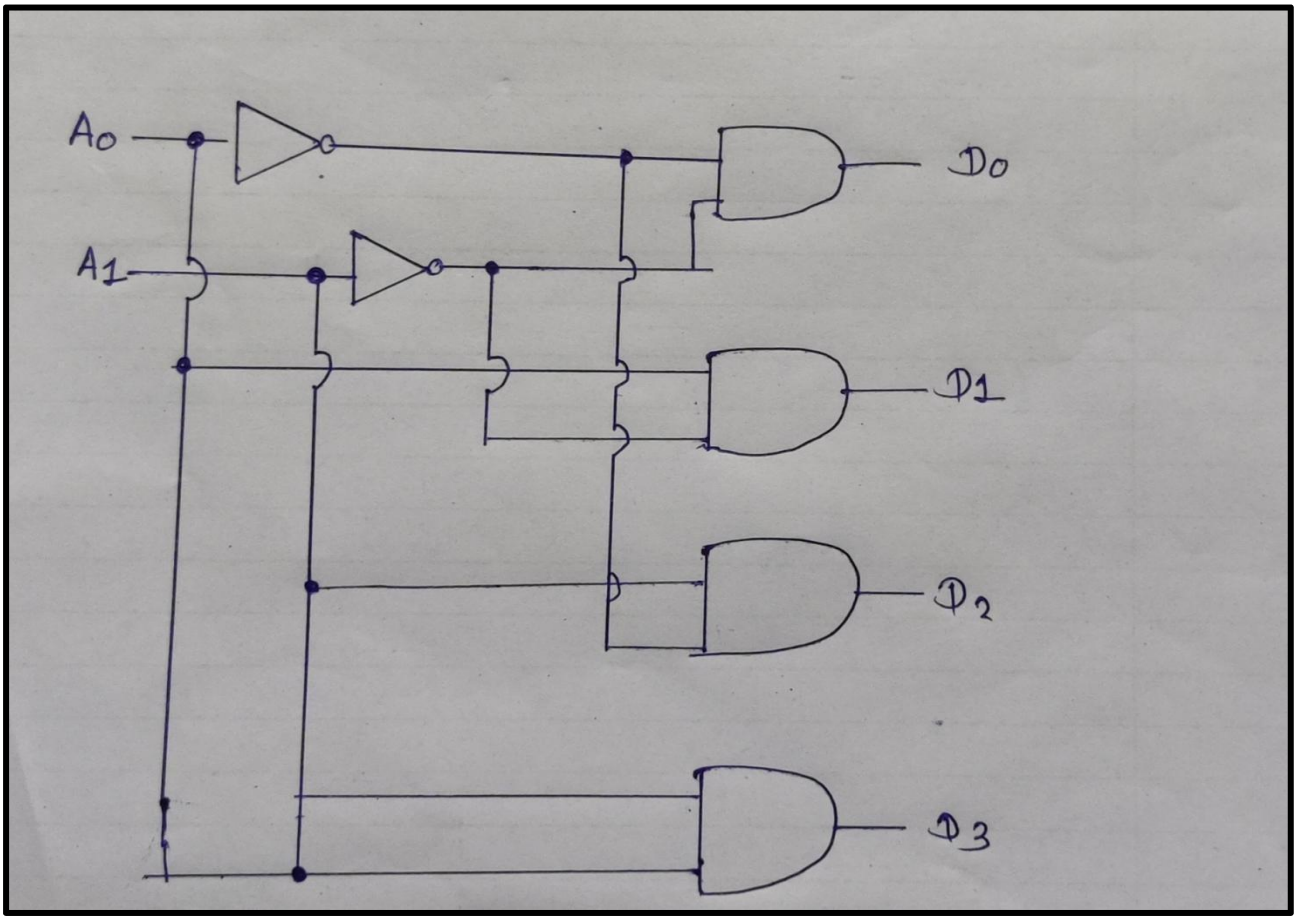
Binary decoder has n-bit input lines and 2 power n output lines. It can be 2-to-4, 3-to-8 and 4-to-16 line configurations. Binary decoder can be easily constructed using basic logic gates. 2 to 4 decoder can be easily implemented with structural and behavioral modelling.



❖ **Find out the optimized Boolean equation (If not given).**

D0 =A0'.A1'
D1 =A0'.A1
D2 =A0.A1'
D2 =A0.A1

❖ **Draw the optimized gate level circuit diagram.**



❖ Truth Table for 2 to 4 Decoder

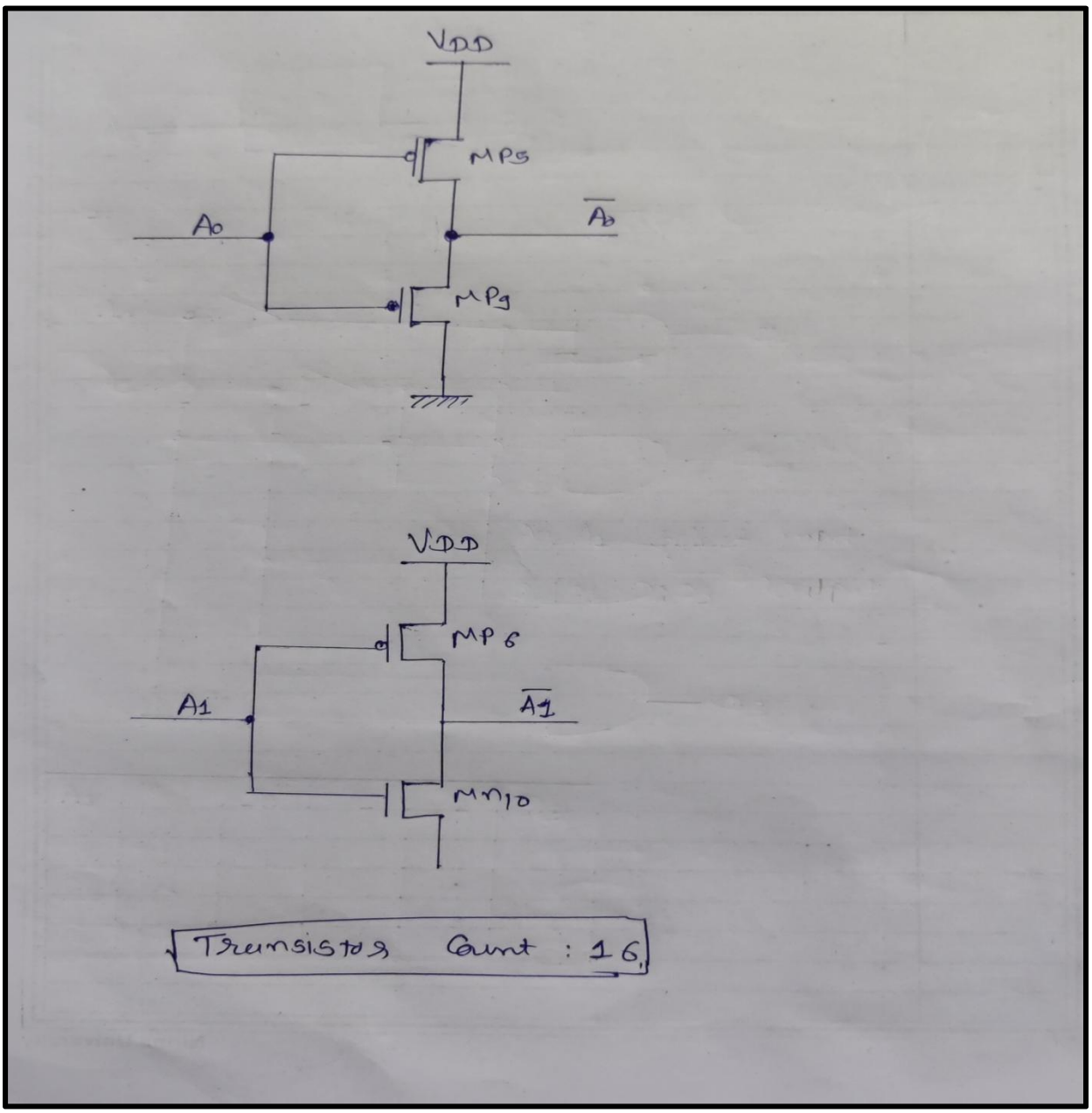
In this type of decoders, decoders have two inputs namely A0, A1, and four outputs denoted by D0, D1, D2, and D3. As you can see in the following truth table – for every input combination, one o/p line is turned on.

A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

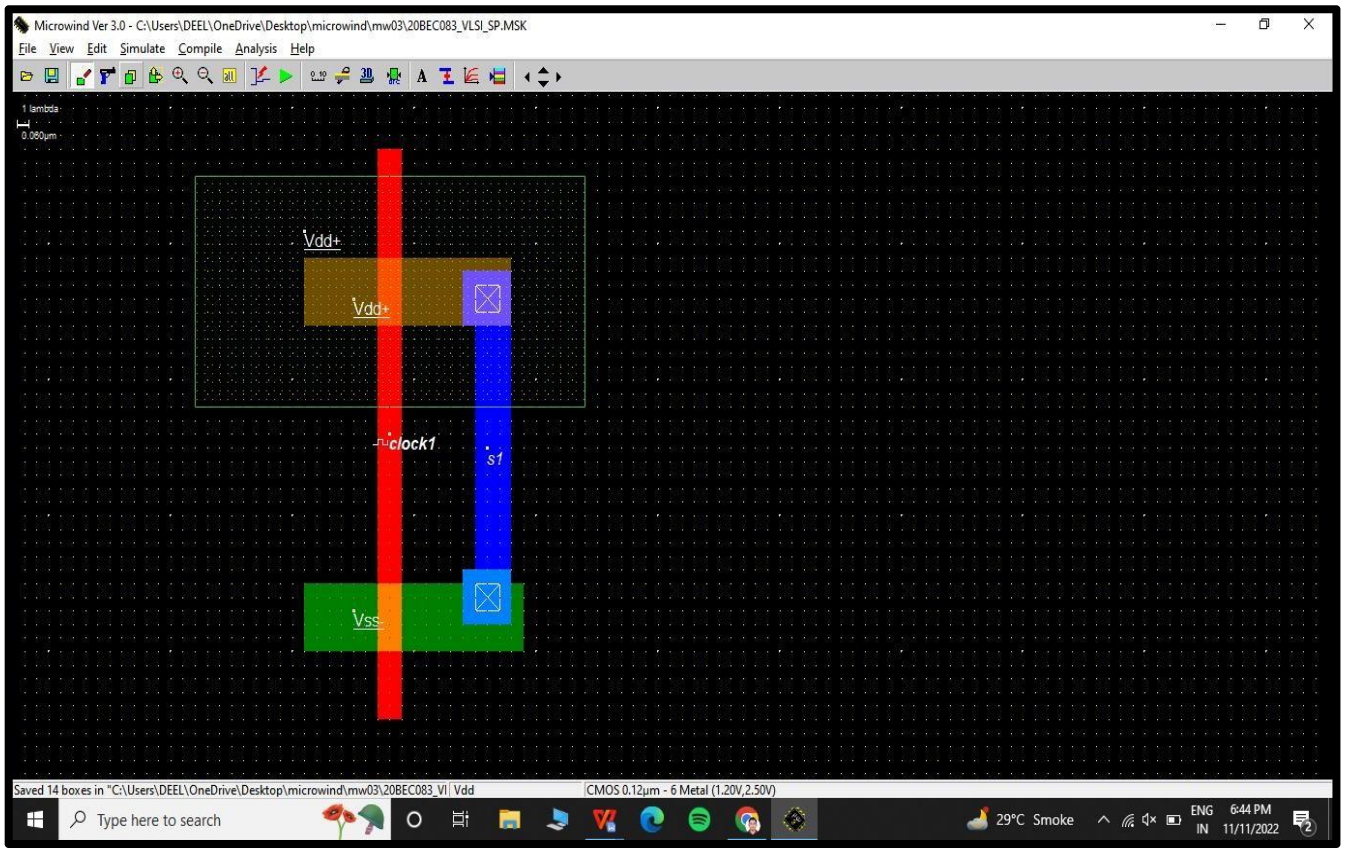
A_0, A_1 : Select input

D_0, D_1, D_2, D_3 : output

❖ **Find an equivalent CMOS inverter circuit.**



❖ In Microwind **CMOS inverter circuit.**



❖ For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?
Ans.

Lowest output Resistance

Here we are considering R=20K

For, VOH only PMOS is consider

No	NO. of transistor is ON	Active Transistor	Resistance
1.	2	A_0 -A_1	10K

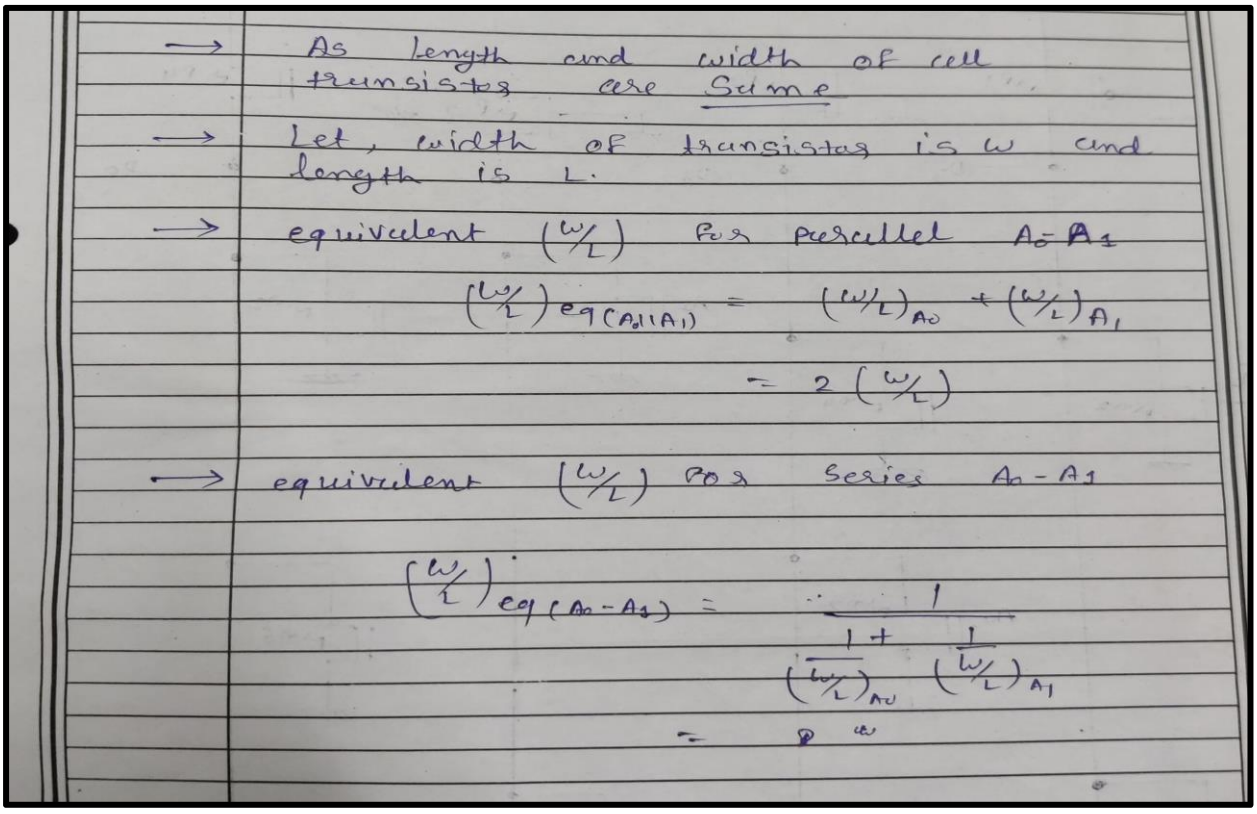
For VOH when transistor A_0 -A_1 are on low

❖ For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

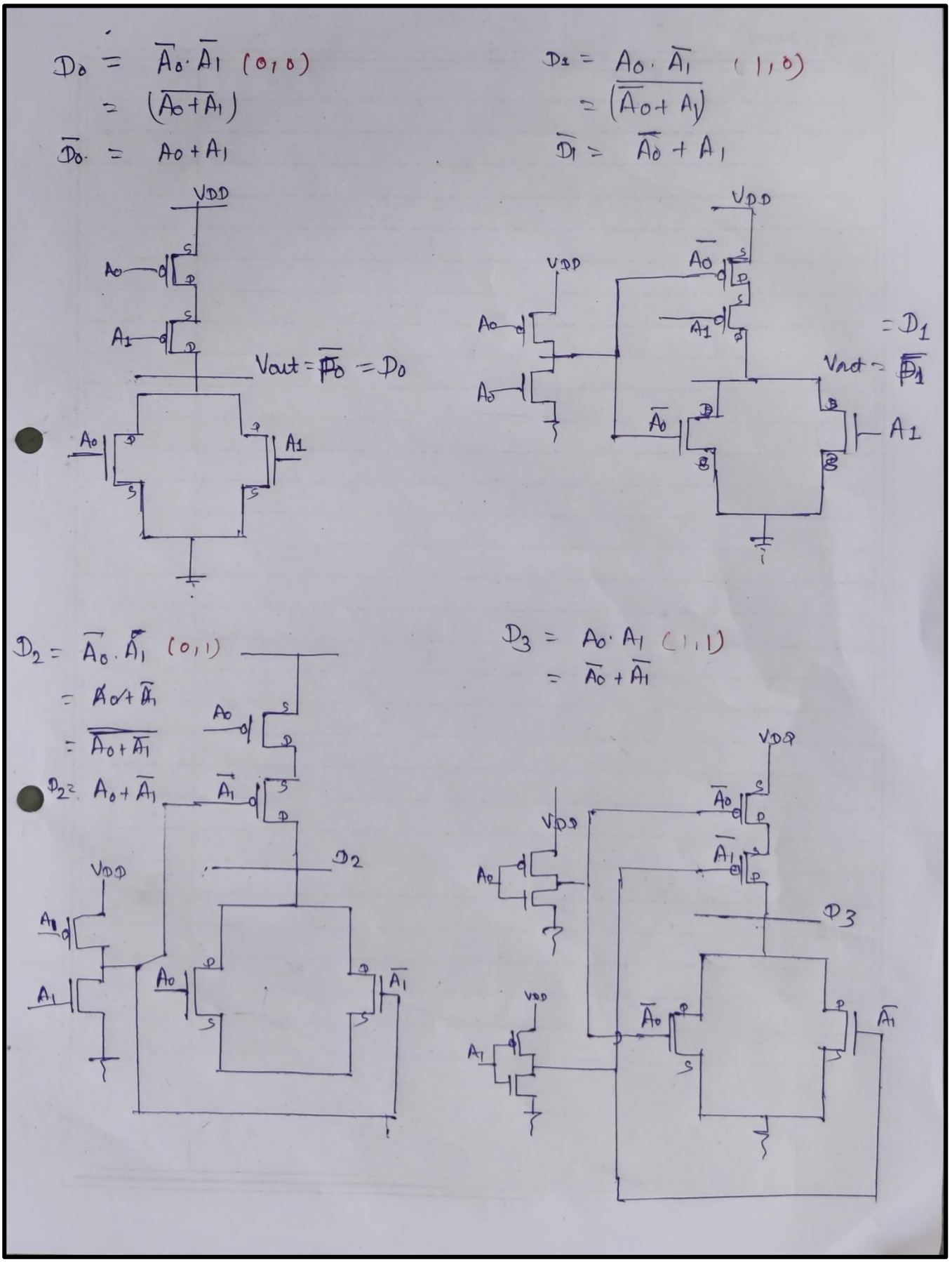
For VOL,only NMOS is consider,

No	NO. of transistor is ON	Active Transistor	Resistance
1	1	A_0 ,A1	20K
2	2	A_0 ,A1	10k

For VOL when transistor C-A-B are on lowest output resistance is achieved.



❖ **Draw the transistor level schematic for CMOS/MOS implementation.**



❖ **State the various level of VOL corresponding to various transistor statuses.**

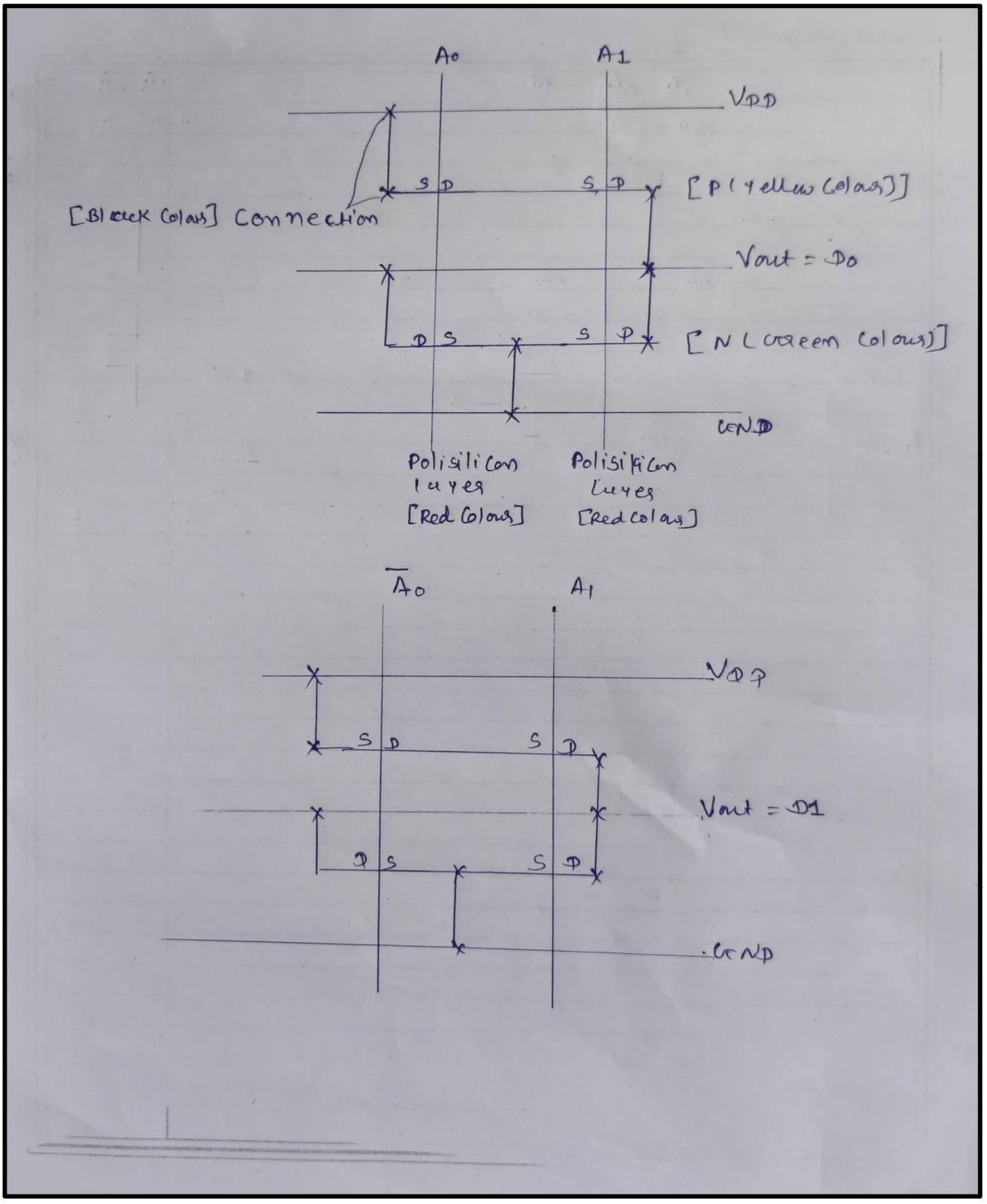
class	A_0	A_1	$(W/L)_n$ equaion	V_{out}
1	OFF	OFF	No	0
2	ON	OFF	$(W/L)_n$	V_{0L1}
3	OFF	ON	$(W/L)_n$	V_{0L2}
4	ON	ON	$2(W/L)_n$	V_{OL3}

❖ Stick Diagram

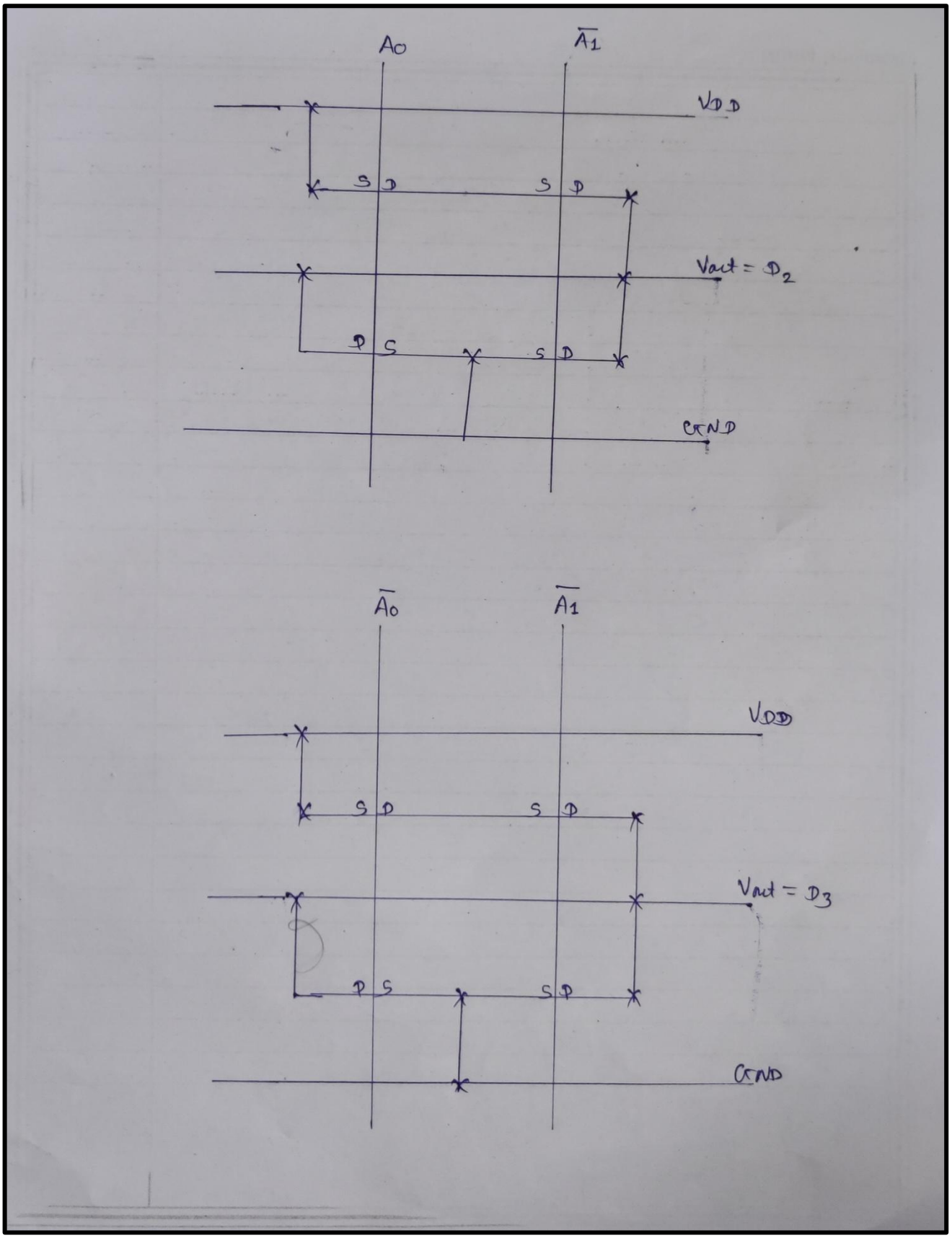
- Blue: Metal.
- Red: Polysilicon.
- Green: N+ diffusion.
- Yellow: P+ diffusion.
- Black: Contacts.

❖ Stick Diagram

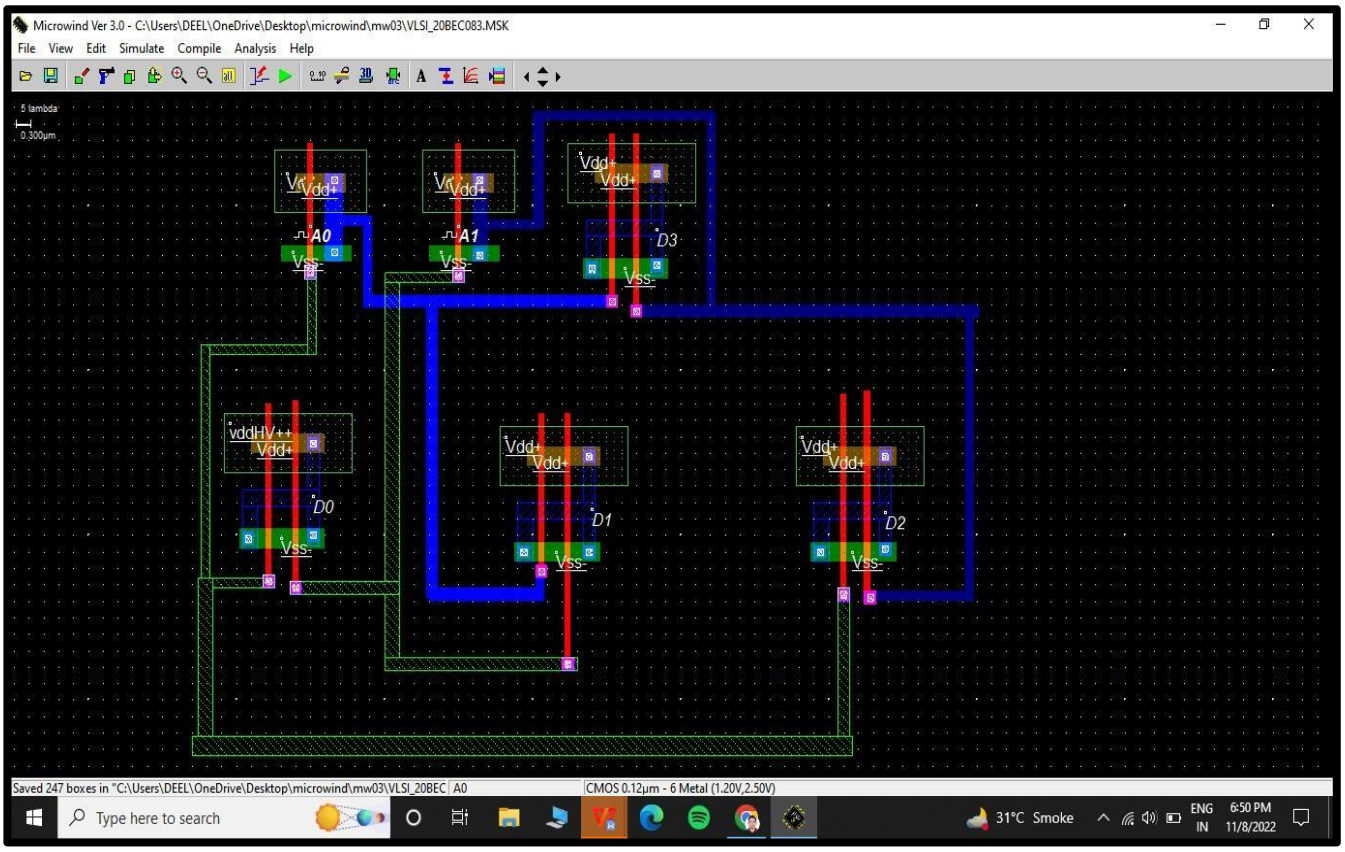
Stick diagramfor D0 and D1 is given below

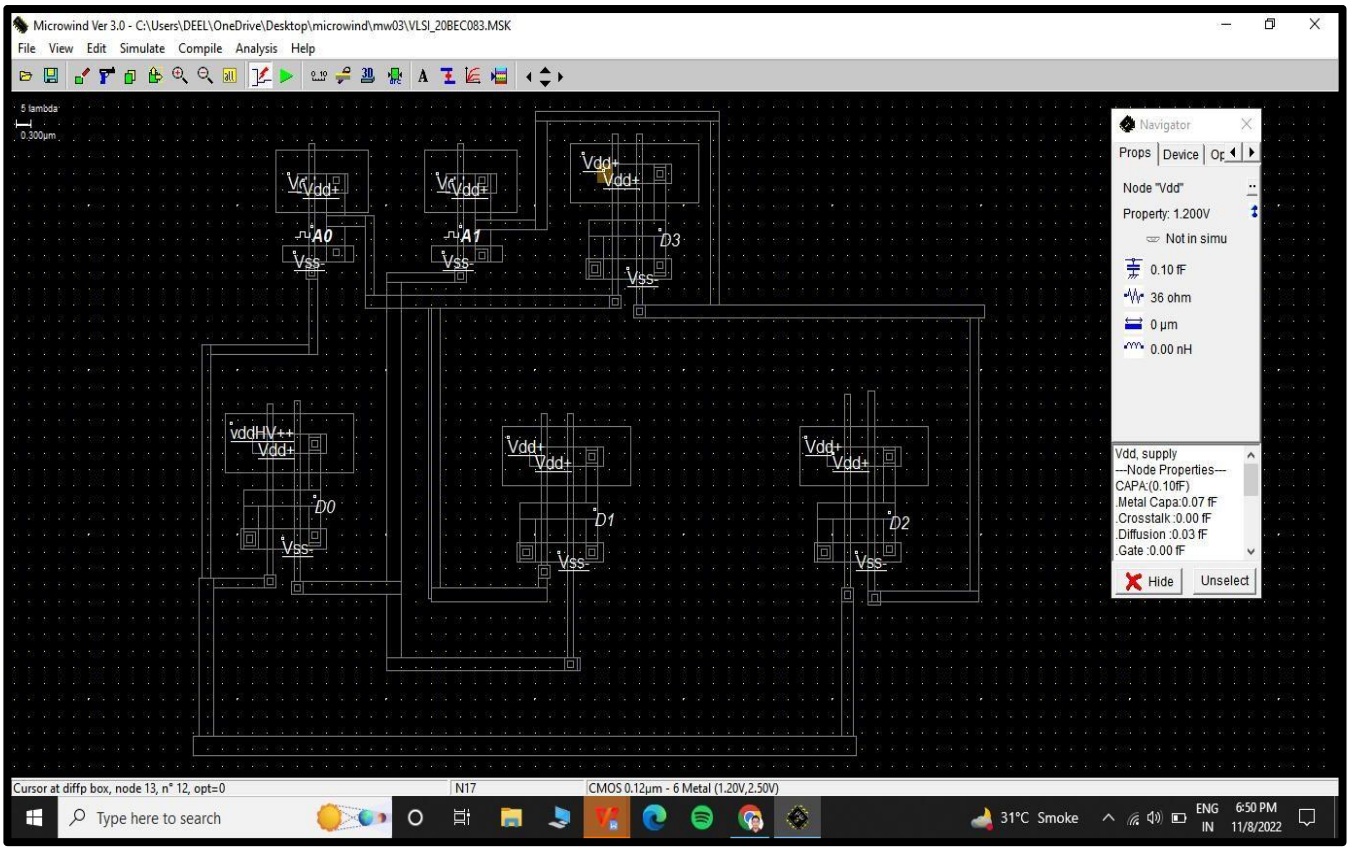


❖ Stick diagramfor D2 and D3 is given below



❖ Layout


Microwind Ver 3.0 - C:\Users\DEEL\OneDrive\Desktop\microwind\mw03\VLSI_20BEC083.MSK
File View Edit Simulate Compile Analysis Help
A0
A1
D3
D0
D1
D2
Vdd+
Vss-
vddHV++
Saved 247 boxes in "C:\Users\DEEL\OneDrive\Desktop\microwind\mw03\VLSI_20BEC A0
CMOS 0.12µm - 6 Metal (1.20V,2.50V)
Type here to search
31°C Smoke
ENG IN
6:50 PM 11/8/2022


Microwind Ver 3.0 - C:\Users\DEEL\OneDrive\Desktop\microwind\mw03\VLSI_20BEC083.MSK
File View Edit Simulate Compile Analysis Help
Navigator
Props Device
Node "Vdd"
Property: 1.200V
Not in simu
0.10 fF
36 ohm
0 µm
0.00 nH
Vdd, supply
---Node Properties---
CAPA:(0.10fF)
.Metal Capa:0.07 fF
.Crosstalk :0.00 fF
.Diffusion :0.03 fF
.Gate :0.00 fF
Hide
Unselect
A0
A1
D3
D0
D1
D2
Vdd+
Vss-
vddHV++
Cursor at diffp box, node 13, n° 12, opt=0
N17
CMOS 0.12µm - 6 Metal (1.20V,2.50V)
Type here to search
31°C Smoke
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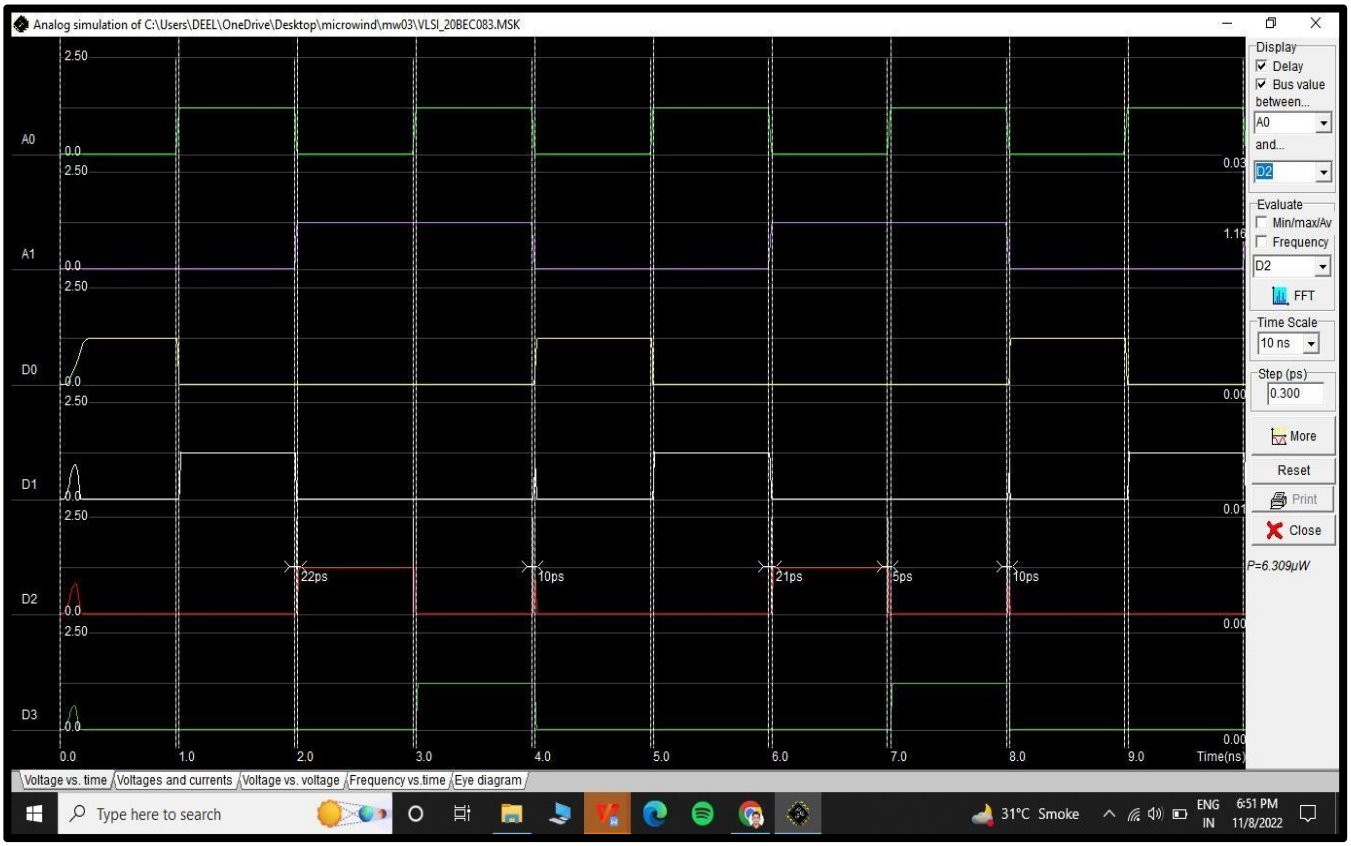
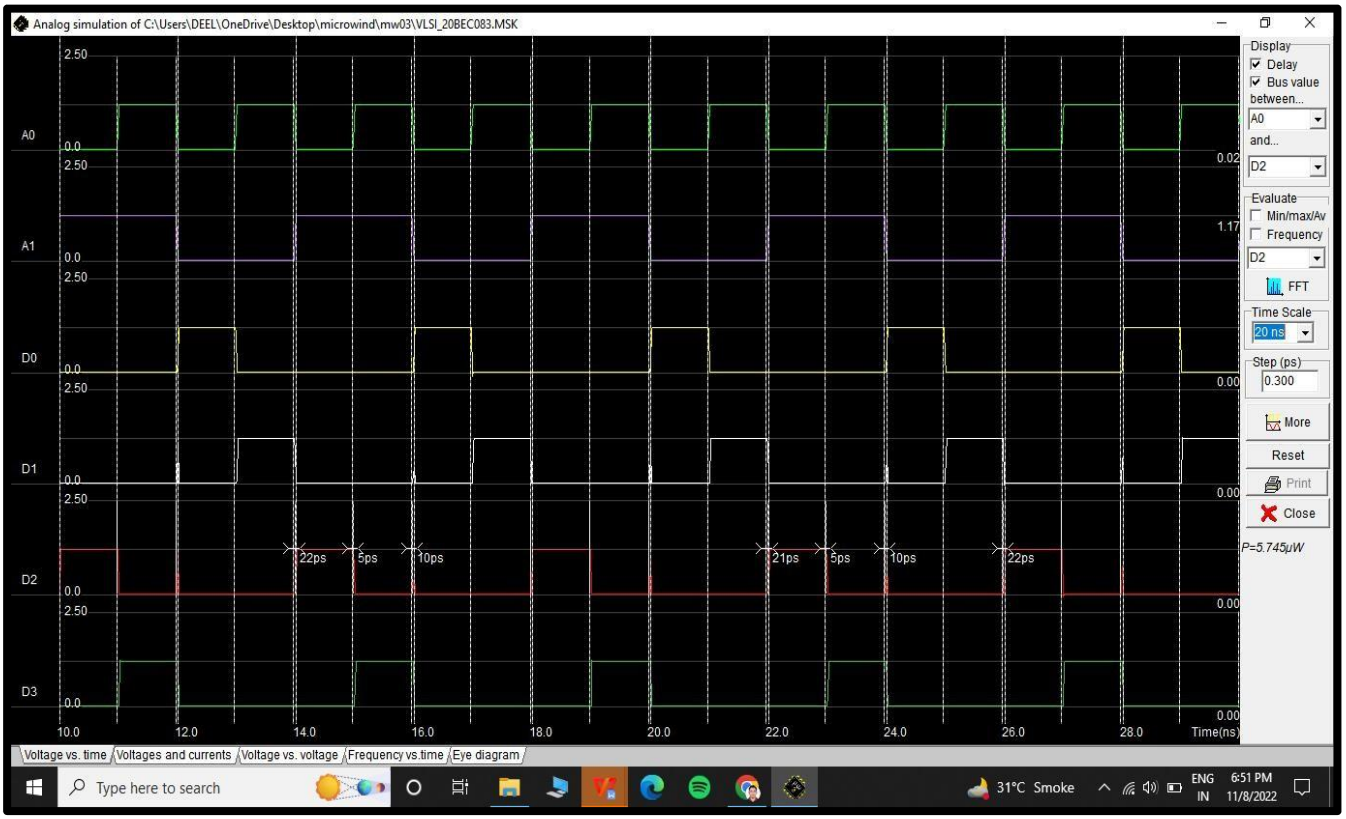
❖ Simulation:


Analog simulation of C:\Users\DEEL\OneDrive\Desktop\microwind\mw03\VLSI_20BEC083.MSK
A0
A1
D0
D1
D2
D3
22ps
10ps
21ps
5ps
10ps
Time(ns)
Display
Delay
Bus value between...
A0
and...
D2
Evaluate
Min/max/Av
Frequency
D2
FFT
Time Scale
10 ns
Step (ps)
0.300
More
Reset
Print
Close
P=6.309µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
Type here to search
31°C Smoke
ENG IN
6:51 PM 11/8/2022


Analog simulation of C:\Users\DEEL\OneDrive\Desktop\microwind\mw03\VLSI_20BEC083.MSK
A0
A1
D0
D1
D2
D3
22ps
5ps
10ps
21ps
5ps
10ps
22ps
Time(ns)
Display
Delay
Bus value between...
A0
and...
D2
Evaluate
Min/max/Av
Frequency
D2
FFT
Time Scale
20 ns
Step (ps)
0.300
More
Reset
Print
Close
P=5.745µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
Type here to search
31°C Smoke
ENG IN
6:51 PM 11/8/2022

❖ Measure the rise time, fall time, propagation delay and other parameters.

Rise time $T_{LH} = 22$ psFall
time $T_{HL} = 5$ ps
Propagation delay $= (T_{LH} + T_{HL})/2 = 27/2 = 13.5$ ps

❖ Applications of Decoder

- Robotic Vehicle with Metal Detector
- Decoder involve in the making of various electronic projects.
- It is used in high-performance memory- decoding or data-routing applications requiring very short propagation delay times.
- They are used in code conversions like binary to decimal, like the 2 to 4 decoder.
- It is used in data distribution as in de-multiplexing.

❖ Conclusion

In this assignment, a static complementary metal-oxide semiconductor-based 2 to 4 bit decoder is introduced (CMOS). The gate level diagram is created using the Boolean Expression as a foundation. For the reader's benefit, the truth table and gate level circuit of the decoder have first been presented. The Stick Diagram of the Circuit, which is derived from the CMOS Implementation Diagram, serves as the framework for the Microwind Design Layout. Microwind simulations at 120 nm demonstrate how the various observed parameters change depending on the input. The following observations have been made as well

- As the width of pMOS increases fall time decreases
- As the width of nMOS increases rise time decreases