Automotive Technologies for Ranging, Vision and Connectivity

LAB REPORT ON A PATCH ANTENNA

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Design a patch antenna working (SWR < 2) at the frequency of 2.6 GHz with a tolerance of $\pm 2.5\%$. The substrate is FR4 with $\varepsilon_r = 4.1 \cdot (3/f[GHz])^{0.025}$, $\tan(\delta) = 0.025$, and thickness $h = 1.6$ mm. The metal is copper with $t = 35$ μm thickness. The antenna must be centered on top of a square ground plane with side length equal to $c/(f\sqrt{\varepsilon_r})$ and must be fed by a microstrip transmission line connected to an edge-mount $50\,\Omega$ connector.

1 SUMMARY

The objective of this report is to present a detailed account of the laboratory experience with patch antennas. The document thoroughly outlines all the stages of the patch antenna design process, beginning with the theoretical framework, followed by the design phase, and concluding with the experimental analysis. Furthermore, it includes a comparison between the simulation results and the real-world measurements obtained during testing

2 INTRODUCTION

The objective of the laboratory experiment was to design a patch antenna with a resonant frequency of 2.6 GHz, as specified in the group specifications. A patch antenna, also referred to as a microstrip antenna, is a relatively straightforward type of antenna that offers numerous advantages, including its lightweight, cost-effectiveness, and simple integration with accompanying electronic components.

Developed in the early 1970s for spatial and aeronautics applications, this antenna gained popularity thanks to its lightweight and low volume, low fabrication cost due to mass production with PCB techniques, easy integration with printed circuits, and conformability. It is also suitable for mobile wireless applications.

However, it should be noted that this antenna type possesses a comparatively larger size in comparison to alternative antenna designs. For instance, some patch antennas are approximately half a wavelength on each side. Additionally, there are some disadvantages, such as low efficiency, narrow bandwidth, low gain, and poor polarization purity.

The architecture of a patch antenna is very simple: it consists of a ground plane, a dielectric material substrate, and a patch of metal. During the laboratory lectures, firstly we were designing the patch antenna using CST Studio. To do this, the first task was to retrieve, from the theory lectures, the method to compute the main parameters of a microstrip antenna. Subsequently, the design of the antenna block was initiated, followed by the execution of simulations to assess its performance. The utilisation of CST Studio enabled the exploration of various parameters, facilitating the optimisation of the antenna's configuration. The final laboratory lecture focused on the collection of measurements from the fabricated antenna, thereby enabling the comparison of the simulation outcomes with real-world observations.

3 THEORY

3.1 Patch Antenna Dimensions

In order to design a patch antenna, it is first necessary to define the different formulas used to derive antenna dimensions from a theoretical point of view.

A patch antenna, as we can see in the figure below, shares similarities with a microstrip transmission line, but there is a crucial distinction between the two. The patch antenna is designed to radiate, and consists of a metal patch that is placed on top of a dielectric substrate, which is then positioned on a metallic ground layer. The purpose of the substrate is to block radiation beyond it, thereby ensuring that the radiation is supplied exclusively in the positive axis, which, in this case, is the Z axis.
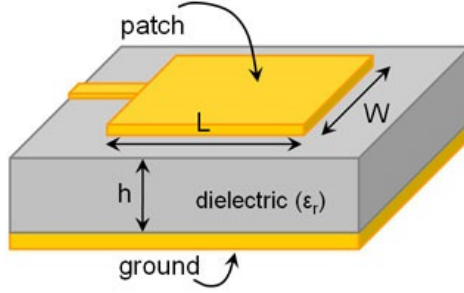

Figure 1: Structure of a Patch Antenna

As mentioned above, we can see the patch antenna as a microstrip line of L_p length and W_p thickness, in particular:

$$L_p = m\frac{\lambda}{2} \tag{1}$$

and

$$W_p = \frac{c}{2f_r}\sqrt{\frac{2}{\varepsilon_r + 1}} \tag{2}$$

where:

- λ is the wavelength

- $c = 3 \cdot 10^8 m/s$ is the speed of light

- f_r is the resonance frequency of the antenna

- ε_r is the dielectric constant of the substrate material, in our case is FR4

3.2 Fringing effect

The resonance condition for a patch antenna is typically given by $L = \frac{\lambda}{2}$. However, as we can see in the figure below, due to edge effects, the actual path length is slightly longer, with a variation ΔL.
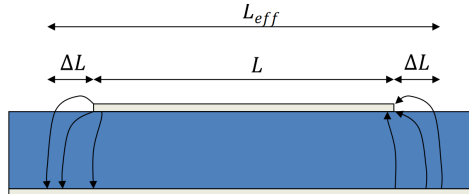

Figure 2: The electric field lines curve at the edges, increasing the electric length of the patch.

These fringing effects cause the patch to appear longer to electromagnetic waves, leading to the definition of an effective length L_{eff} defined as:

$$L_{eff} = L + 2\Delta L \tag{3}$$

where ΔL is derived from an empirical formula:

$$\Delta L \simeq h \cdot 0.412 \frac{(\varepsilon_{\text{eff}} + 0.3)\left(\frac{W_p}{h} + 0.264\right)}{(\varepsilon_{\text{eff}} - 0.258)\left(\frac{W_p}{h} + 0.8\right)} \tag{4}$$

and where ε_{eff} is the effective relative permittivity of a microstrip of width W_p:

$$\varepsilon_{\text{eff}} \simeq \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12\frac{h}{W_p}}} \tag{5}$$

By imposing $L_{\text{eff}} = \frac{\lambda}{2}$ and knowing that $\lambda = \frac{c}{\sqrt{\varepsilon_{\text{eff}}}f_r}$, it follows that:

$$L_p = \frac{c}{2f_r\sqrt{\varepsilon_{\text{eff}}}} - 2\Delta L \tag{6}$$

3.3   Impedance matching

When designing a patch antenna, it is essential to achieve impedance matching between the feed and the characteristic impedance of the transmission line, which is typically 50 Ω. This ensures optimal power transfer from the transmission line to the standing wave generated on the patch. It is not feasible to feed the patch at one edge, as the input impedance $R_i(0)$ exceeds 50 Ω. The connection between the patch and the feeding line is located within the patch.

To optimize the impedance matching, the length L should first be varied until an input reactance of zero is achieved at the desired resonance frequency. Following this, adjust the feed position x_0 to make the real part of the input impedance equal to 50 Ω at the same frequency. This process minimizes reflection and maximizes efficiency.

In order to achieve this value we have to exploit this formula:

$$R_i(x_0) = \frac{1}{2G_1}\cos^2(\frac{\pi}{L}x_0) \tag{7}$$

where:

$$G_1 = \frac{W_m}{120\lambda_0}(1 - \frac{1}{24}(\frac{2\pi h}{\lambda_0})^2) \tag{8}$$

and

$$\lambda_0 = \frac{c}{f_r} \tag{9}$$

So, by using the the (7) and isolate the x_0 term ,we are able to find the value of the feeding line slot in order to have the impedance of 50 Ω, having a final result similar to the image below.
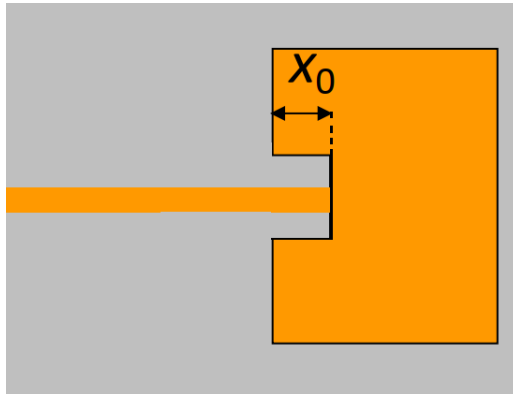

Figure 3: patch antenna with the two slot of lenght x_0 in orer to have the fedding line matched

4   DESIGN OF THE PATCH ANTENNA

4.1   Substrate and Ground plane size

As previously stated, the patch antenna will be mounted on an FR4 material substrate, with a ground plane situated behind it. The initial step is to calculate the dimensions of the board using the following formula:

$$W_s = \frac{c}{f_0\sqrt{\varepsilon_r}} \tag{10}$$

As can be seen, we need to know the value of ε_r, which is provided in the initial specifications and is equal to:

$$\varepsilon_r = 4.1 \cdot (3/f[\text{GHz}])^{0.025} \tag{11}$$

By substituting with our value of frequency in (11) we obtain

$$\varepsilon_r = 4.1 \cdot (3/2.6[\text{GHz}])^{0.025} = 4.11$$

so we can now substitute this value in the formula of W_s (10), but since we are gonna use a square board it will be:

$$W_s = L_s = \frac{c}{f_0\sqrt{\varepsilon_r}} = \frac{3 \cdot 10^8}{2.6 \cdot 10^9 \sqrt{4.11}} = 0,056882559m \simeq 56.9 \ mm$$

So, now we have the dimensions of the ground plane.

4.2   Patch size

In regard to the dimensions of the patch antenna, the width W_p will be calculated using the designated formula (2), so:

$$W_p = \frac{3 \cdot 10^8}{2 \cdot 2.6 \cdot 10^9} \sqrt{\frac{2}{4.11 + 1}} = 0,03607639 \simeq 36.1 \ mm$$

For the length L_p, the formula (6) will be employed, with consideration for fringing effects, so first of all we have to determine the value of ΔL, but before doing that we have to calculate the value of ε_{eff} using the equation (5):

$$\varepsilon_{\text{eff}} \simeq \frac{4.11 + 1}{2} + \frac{4.11 - 1}{2} \frac{1}{\sqrt{1 + 12\frac{1.6 \cdot 10^{-3}}{36.1 \cdot 10^{-3}}}} = 3,811381 \simeq 3,81$$

so we can now calculate the value of ΔL, by put all the value in the formula (4):

$$\Delta L \simeq 1.6 \cdot 10^{-3} \cdot 0.412 \frac{(3.81 + 0.3)\left(\frac{36.1 \cdot 10^{-3}}{1.6 \cdot 10^{-3}} + 0.264\right)}{(3.81 - 0.258)\left(\frac{36.1 \cdot 10^{-3}}{1.6 \cdot 10^{-3}} + 0.8\right)} = 0,00074509 \ m \simeq 0.745 \ mm$$

so, finally we can calculate the value of L_p, let's substitute all the value in (6):

$$L_p = \frac{3 \cdot 10^8}{2 \cdot 2.6 \cdot 10^9 \sqrt{3.81}} - 2 \cdot 0.745 \cdot 10^{-3} = 0,02804 \ m \simeq 28.0 \ mm$$

Subsequent to these preliminary calculations, the creation of the substrate may be initiated, with FR4 selected as the material and the various physical values given technical specifications. The subsequent steps involve the creation of the ground plane and the design of the patch, with copper chosen as the material for the latter two layers.

4.3   Microstrip design

After the creation of the substrate and the patch, the microstrip will be created; this should have a characteristic line impedance as close as possible to 50 Ω. To achieve this result, we used a macro from CST, the Impedance calculation selecting the 'thick microstrip' and by putting all our values we start searching for which width of the microstrip would give us an impedance value of 50 Ω, in our case a value of 3.2 mm was chosen as width. In the figure below, you can see the use of the macro and note that with the thickness of 3.2 mm, the line impedance is approximately 49.7 ohms.
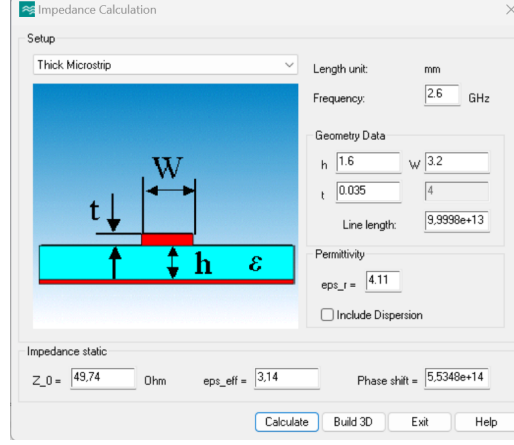

Figure 4: Macro impedance calulcation window of CST

4.3.1   Slots design and impedance matching

After an initial simulation (the discussion of the results is deferred to the next section), it was necessary to introduce slots on the microstrip in order to improve antenna performance. This intervention made it possible to electrically extend the length of the microstrip, feeding the patch more internally and increasing the impedance seen at the patch input.

In order to find how deep this slot must be, equation 6 was used by isolating x_0, obtaining:

$$x_0 = \frac{L}{\pi} \arccos\left(\sqrt{2G_1 R_i(x_0)}\right) \tag{12}$$

where, by substituting the value in (8) we have:

$$G_1 = \frac{W}{120 \cdot 115.38 \cdot 10^{-3}} \left[1 - \frac{1}{24}\left(\frac{2\pi 1.6 \cdot 10^{-3}}{115.38 \cdot 10^{-3}}\right)^2\right] = 0.002604694 \simeq 0.0026$$

so, put the value in (12) and obtain:

$$x_0 = \frac{14.4 \cdot 10^{-3}}{\pi} \arccos\left(\sqrt{2 \cdot 0.0026 \cdot 50}\right) = 0.009241228 \simeq 9.2 \ mm$$

so, according to calculations, we will need two slots of approximately 9.2 mm in length.
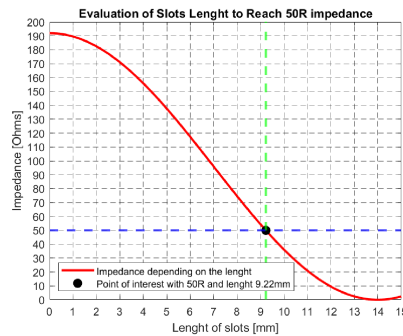

Figure 5: Graph representing the search for the optimum value for slot length, indicating approximately 9.2mm as the length to achieve matching

4.4   Simulation and tuning

4.5   First simulation result

Following the calculation of the parameters of the patch, the initial simulation was conducted, as illustrated in the subsequent graphs.
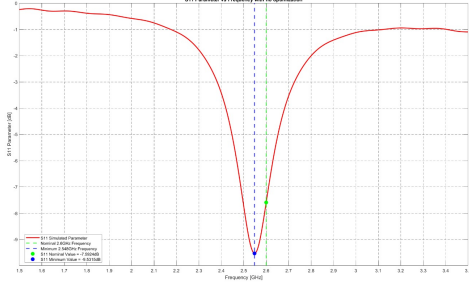

Figure 6: S1,1 graphs representing the return loss of the patch antenna during the first simulation without slots
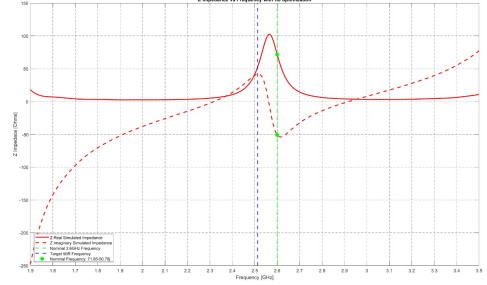

Figure 7: S1,1 graphs representing the return loss of the patch antenna during the first simulation without slots

As depicted in Figure (6), the outcome of the simulation did not meet expectations, exhibiting a peak return loss of approximately -9.5 dB. The figure (7) demonstrates that the microstrip is not entirely matched, exhibiting an impedance of 71.9 Ω in the real part and a value of approximately 50.8 Ω in the imaginary part. However, it is observed that the peak frequency falls within the 2.5% tolerance stipulated by the specifications.

4.6   Simulation and result with slots

After this first simulation, the slots were inserted following the measurements from the theoretical calculations. As can be seen in the figures below, the result improved slightly to a peak of -15.2 dB (figure (8)) and an impedance value of approximately 35.1 Ω in the real part and 0.14 Ω in the imaginary part (figure (9)).
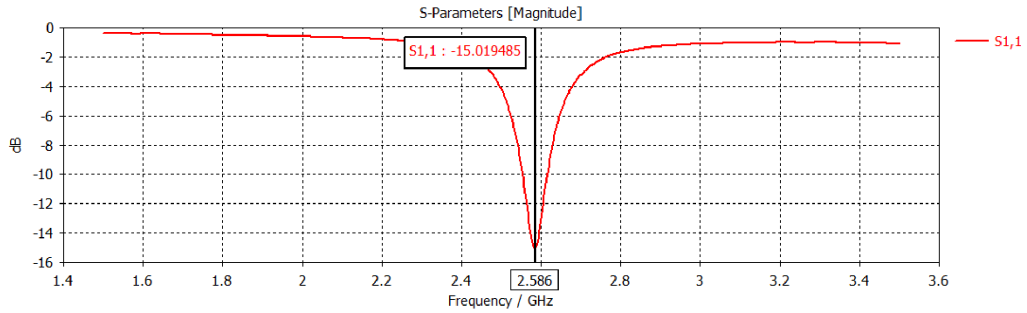

Figure 8: S1,1 graphs representing the return loss of the patch antenna with a slots of 9.2mm
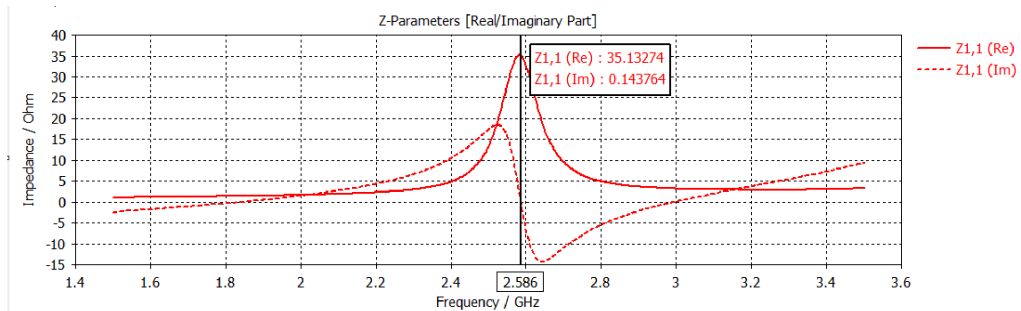

Figure 9: Z1,1 graphs representing the impedance of the patch antenna with a slots of 9.2mm

4.7   Tuning of the patch antenna

Starting from the previous results, in order to improve the performance of the antenna, it was necessary to modify certain parameters, in particular the length of the slots, until a value was found that would allow the desired impedance to be achieved and get even closer to the frequency required by the specifications.

In order to assess what was the best possible result, a sweep had to be made, simulating different slot lengths and finding the value that would satisfy the different requirements.
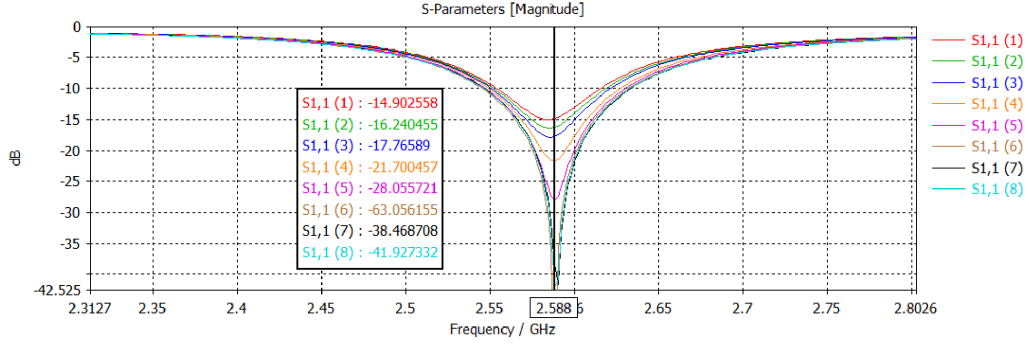

Figure 10: Graph representing the returnig loss of all different values of the slots tested

As can be seen from the image above, as the slot values were reduced, the peak of the return loss grew and grew until it reached its maximum value, which corresponds to a slot length of 7.6 mm.

With the final choice of slot, the design of the antenna patch is complete, below is the table (ref) containing the patch dimensions and a reference image.

Figure 11: References for the patch antenna dimensions reported in the table alongside
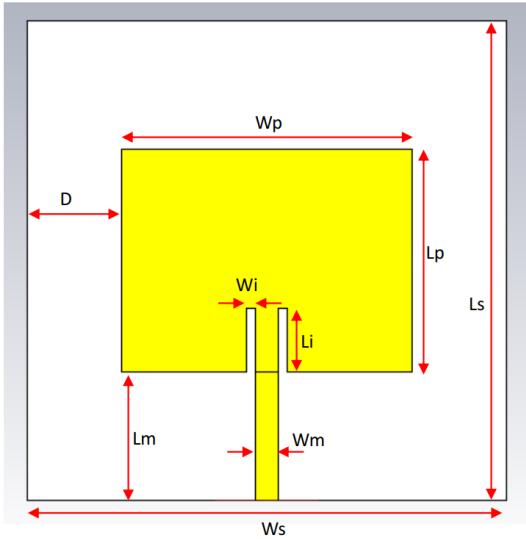
Dimension	Value (mm)
Substrate Width, W_s	56.9
Substrate Length, L_s	56.9
Microstrip Width, W_m	3.2
Microstrip Length, L_m	14.4
Distance, D	10.4
Slot Width, W_i	1.0
Slot Length, L_i	7.6
Patch Width, W_p	36.1
Patch Length, L_p	28.0

Table 1: Table of patch antenna dimensions

5   RESULTS AND MEASUREMENTS

5.1   Final simulation