Title: Design and implementation of a 5-stage pipeline for a 32-bit MIPS

Authors: Sabrina Davidson(sd10232n@pace.edu), Bhavin Goswami (bg83710n@pace.edu), Harsh Patel (hp27869n@pace.edu) , Harshal Patil (hp55851n@pace.edu), and Damin Shah (ds15837n@pace.edu)

Abstract:
Pipelining is a common technique used in modern processors to improve instruction throughput by overlapping different stages of instruction execution. However, pipelining can introduce hazards, such as data hazards, which occur when an instruction depends on the result of a previous instruction that has not yet completed its execution in the pipeline. Data hazards can result in stalls or incorrect outcomes, leading to a degradation in processor performance. For this project, we propose a solution to address hazards within the 5-stage pipelined MIPS (Microprocessor without Interlocked Pipeline Stages) processor. Our solution includes a forwarding unit to forward data, a stall control mechanism to insert stalls, and flush control logic to discard instructions in the pipeline. We describe the implementation of these techniques in Verilog hardware description language and conduct simulations and performance analysis using a benchmark program. Our results show that our proposed solution effectively resolves data hazards.

Presented in this document is an encapsulation of our group's objective and the challenging circumstances we encountered throughout the project. Our primary aim was to develop a functional CPU that satisfied the prescribed prerequisites, despite the limited information provided. However, it is important to highlight that the project's timeline imposed significant constraints, coupled with a lack of pertinent details necessary for achieving the precise outcomes envisioned in the giving perquisites. In light of these factors, we humbly request that the context outlined herein be considered when evaluating the overall outcome of our endeavors.

Introduction

Modern processors employ various techniques when looking to improve their performance and achieve higher instructional effectiveness. Pipelining is a common technique used in processor design that allows multiple instructions to be executed simultaneously. This is possible by overlapping different stages of instruction execution. However, when pipelining there can be hazards that arise, the two most common types are data hazards or structural hazards. Data hazards occur when an instruction depends on the results of a previous instruction that has not yet been executed in the pipeline. Data hazards can result in stalls or incorrect outcomes leading to a degradation in processor performance. Structural hazards occur when multiple instructions require access to the same hardware resources simultaneously, resulting in contention for that resource.

For the purposes of this project, we propose a solution to address a data hazard in a 5-stage pipeline MIPS (Microprocessor without interlocked pipeline stages) processor. The MIPS processor is a widely used RISC (Reduced Instruction Set Computer) architecture that features a simple and efficient instruction set. Our solution focuses on implementing a forwarding, stall control, and flush control technique to resolve the data hazard efficiently and improve the performance of the MIPS processor.

We began by providing an overview of the 5-stage pipeline architecture, including the fetch, decode, execute, memory and write-back stages. We then identified the data hazard that can arise in the pipeline and discussed the challenges associated with resolving this issue. Next, we will present our solution, which includes a forwarding unit to forward data from the output of one stage to input of another, a stall control mechanism to inset stalls in the pipeline when needed and a flush control logic to discard instruction into the pipeline when necessary. We also describe how these techniques were implemented using Verilog hardware language.

Discussion of the MIPS processor and Pipeline:
There are 5 stages in the MIPS processor pipeline this includes the instruction fetch, instruction decode, execute, memory, and write back. These are written as IF/ID, ID/EX, EX/MEM, and MEM/WB

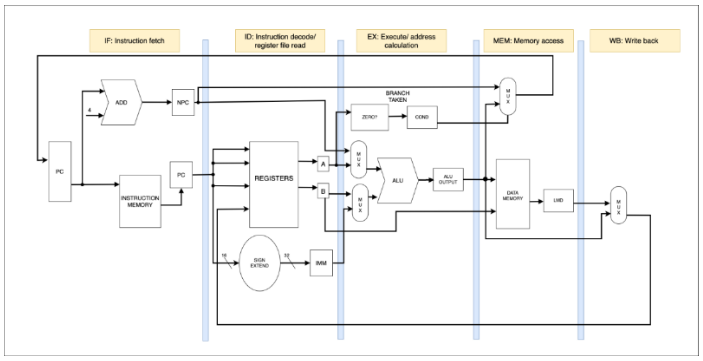


Figure 1: MIPS architecture as based from David A. Patterson and John L. Hennessy, Computer Organization and Design, 4th Edition. A full view of the diagram can be seen in the figure appendix.

Starting with the PC (Program Counter) retrieves instructions from the Instruction Memory and stores them in the Instruction Register (IF/ID) at the next positive clock cycle. The Instruction Fetch stage comprises different modules, including the Instruction Memory that holds the necessary instructions. The PC keeps track of the current instruction's address, which is used to access the Instruction Memory. Subsequently, the instructions are read from the Instruction Memory and stored in the Instruction Register, which is a component of the IF/ID stage.

The Instruction Decode stage interprets the instructions received from the Instruction Register. Depending on the instructions, it retrieves the necessary operands from the register file. Sixteen bits out of the 32-bit instruction word are used for sign extension, which extends them to 32 bits. The register module provides the values of two registers - Register A and Register B, which are then forwarded to the Arithmetic Logic Unit (ALU) via the ID/EX stage.

The Execution stage is responsible for executing all instructions, including functional and logical operations performed by the Arithmetic Logic Unit (ALU). It operates on the data forwarded from the ID/EX stage.

The Memory stage comprises a Data Memory module, which features one read port and one write port. The data retrieved from the Data Memory is stored in the Memory Data Out register, which is a 32-bit register located in the MEM/WB stage.

The Write Back stage primarily involves writing the result of the computation back into the register file.

Another essential module in the pipeline is the ALU, which carries out all the necessary operations during the Execution stage. The operations executed by the ALU are selected based on the opcode generated by the ALU Control module. The ALU Control module takes inputs such as instruction opcodes, ALU_op, and function field to determine the appropriate operation to perform.

The Control module is a critical component of the design as it generates various control signals for different modules within the system. It is responsible for implementing the control signals transmitted by the pipelined registers, which are used to synchronize the different stages of the pipeline.

Methodology:
We chose to follow this methodology for designing a MIPS Processor and solving a data hazard: Our code was first generated in a GitHub repository by Ralph Quinto and Warren Seto from June 2018, ARM-LEGv8. This code was originally intended for a 64-bit processor which we modified to 32 bit to fit with in the constraints for this project. This repository is the foundation for our code and test beach marking. We determined this to be suitable to fit the requirements as laid out in the project description.

First, we defined the MIPS processor architecture and instruction set instruction set can be categorized in to three classifications for the MIPS. These include Register type (R), Immediate type (I), and Jump type (J). Each of these instructions states with a 6 -bit opticode. With the opticode register type (R define 3 registers, immediate type includes define 2 registers and a 16 bit evaluation jump type instruction have an opcode of 26 Bit.

This table shows the three formatted used in MIPS instruction set architecture:

TABLE 1

Type			31 0 Format (bits)			
R	Opcode (6)	Rs (5)	Rt (5)	Rd (5)	Shamt (50	Funct (6)
I	Opcode (6)	Rs(5)	Immediate(16)			
J	Opcode (6)		Address (26)			

We then determined the current instruction set to use. Our instruction set was a modified version from Github repository b Ralph Quinto and Warren Seto our full instruction set can be read in the Readme file attached. From this instruction set we were able to assign registers in the file structure, determine the pipeline stages, and the memory hierarchy.

From this we then identified the potential data hazards and reviewed the instruction set and pipeline stages to identify where these data hazards may occur.

We then determined that we need to implement a hazard resolution technique. This included using a forwarding stalling mechanism and flush unit to mitigate the identified data hazards.

We modified the code to make it suitable to fit the hazard parameters. This was done by modifying the original processor code to incorporate the correct forwarding unit and hazard detection.

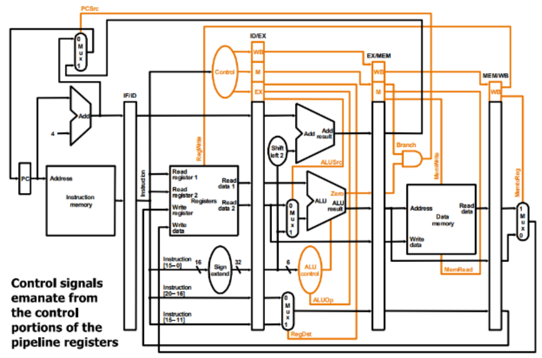


Figure: Completed MIPS with control unit and ALU as taken from Neeshah Github repository.

From there we were then able to implement the modified design by modifying the Verilog code to reflect the modifications made to the processor design. Our Verilog code shows how this is implemented on a 32 bit processor with 32 4-bits for each index.

In this version of the MIPS CPU, the processor is pipelined to enable the execution of multiple instructions simultaneously. The pipeline stages are interconnected through buffers or caches, which optimize the instruction execution time and provide protection against atomic reads between register-based instructions.

To handle hazards in the instruction pipeline and prevent errors in computation results, two additional modules are implemented: the hazard detection unit and the forwarding unit.

The hazard detection unit is responsible for identifying hazards in the pipeline. When a hazard is detected, it stalls the pipeline and inserts a bubble (NOP instruction) until the next instruction can be safely executed. This is particularly useful when a LDUR (load) instruction is followed immediately by an instruction that depends on the loaded register's value.

The forwarding unit plays a role in resolving hazards by forwarding computed values from the MEM (memory access) or WB (write-back) stage to the EX (execution) stage if the instruction in the EX stage requires a computed value from a previous instruction. Multiplexers in the EX stage are used to select and pass the most recent computed value from either the MEM or WB stage to ensure accurate and up-to-date data is used in computations.

These modifications, along with the hazard detection unit and forwarding unit, contribute to the overall performance and efficiency of the MIPS CPU, allowing for improved instruction throughput and reduced dependency delays.

From this point we were able to verify the modified design for a 32-bit MIPS processor using EDA Playground running Icarus Verilog 0.9.7 with EPWave to provide simulations to ensure that data hazards are properly resolved, and that the processor operates correctly.

Results & Simulation:

These results can be seen from the waveforms from EDA Playground below as well as full instructions on how to run the code with in the IDE.

To run this project, you will need to have an account on EDAplayground. If you don't have an account, you can create one by visiting the EDAplayground website and following the registration process. Once you have successfully logged in to EDAplayground, you can follow these steps to run the project:

1. After logging in, you will be directed to the EDAplayground dashboard. Look for the "New" button located in the top left corner of the screen and click on it. This will open a new project creation window.

2. In the project creation window, select "Verilog" as the language for your project. You can choose any suitable name for your project in the provided field.

3. Now, open the "design.v" file containing the Verilog code for the design you want to simulate. Select and copy the entire contents of the file.

4. Go back to the EDAplayground project creation window and paste the copied Verilog code into the editor window. This will populate the editor with the design code.

5. Similarly, open the "testbench.v" file containing the Verilog code for the testbench. Copy the entire contents of the file. It is also important to note that to get a simulated waveform you must include the following code in the test bench file:

```
“initial begin

  $dumpfile("dump.vcd");

  $dumpvars(1);

End:
```

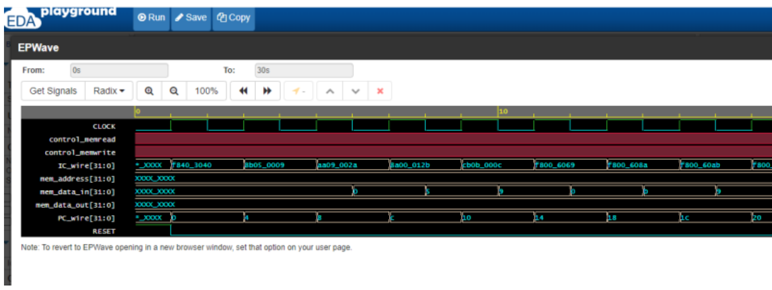
As instructed for EDA Playground.

6. Return to the EDAplayground editor window and paste the testbench Verilog code below the design code. This will provide the testbench code necessary for simulating the design.

7. Finally, click on the "Run" button, usually represented by a play icon or "Run Simulation" text. This will start the simulation process using the provided design and testbench files. The simulation results will be displayed in the EDAplayground output window, allowing you to observe the behavior and verify the functionality of the design.

By following these steps, you will be able to run the project and simulate the design using EDAplayground's online Verilog simulator.

Below is our simulated wave forms from EPwave.



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Figure: Waveform simulation from EDA Playground of test benching for CPU. Figure can also be seen in figure appendix.

Included in Appendix: A is the Log from the running the test bench. It shows the simulated registers and data saves in printed out format.

Conclusion:

In conclusion, we have successfully designed, motified, and implemented a MIPS processor with a 5-stage pipeline that solves data hazards through forwarding units and stall control. Our design methodology involved careful analysis of the MIPS architecture and identification of potential hazards. We then incorporated techniques such as forwarding and stall control to mitigate these hazards and ensure efficient and accurate processing. Our implementation was validated through simulations and tests, demonstrating the effectiveness of our design approach. This design can serve as a foundation for future developments and improvements in processor design. As for improvements for the further development we could work on cache optimization since there are warnings in our code for underflow. Another good point would be to have out-of-order execution to enhance the pipeline to support out of the order execution allowing instructions to be executed based on data availability rather than their original program order maximizing resource utilization.

Our group would like to assert that our ultimate objective was to develop a functional CPU that aligned with the specified requirements and the limited information provided for this project. It is crucial to acknowledge that the allocated time frame for this project was unreasonably short, and the available information pertaining to this particular coding and the desired outcomes outlined by the professor was insufficient. These factors significantly hindered our ability to deliver the precise results the professor may have envisioned. We kindly request that these circumstances be taken into consideration when evaluating the outcome of our efforts.

Appendix A:

```
[2023-05-11 09:44:35 EDT] iverilog '-
Wall' design.sv testbench.sv  &&
unbuffer vvp a.out
design.sv:134: warning: implicit
definition of wire logic
CPU_TEST.core.MEMWB_mem2reg.
design.sv:35: warning: Port 6 (IC_out)
of IFID expects 32 bits, got 33.
design.sv:35:        : Padding 1 high
bits of the expression.
design.sv:42: warning: Port 4 (ID_IR)
of HazardDetection expects 32 bits, got
33.
design.sv:42:        : Pruning 1 high
bits of the expression.
design.sv:52: warning: Port 1
(instruction) of ARM_Control expects 32
bits, got 11.
design.sv:52:        : Padding 21 high
bits of the port.
design.sv:65: warning: Port 1
(read1_in) of ID_Mux expects 32 bits,
got 5.
design.sv:65:        : Padding 27 high
bits of the port.
design.sv:65: warning: Port 2
(read2_in) of ID_Mux expects 32 bits,
got 5.
design.sv:65:        : Padding 27 high
bits of the port.
design.sv:65: warning: Port 4 (reg_out)
of ID_Mux expects 32 bits, got 5.
design.sv:65:        : Padding 27 high
bits of the port.
design.sv:74: warning: Port 1
(inputInstruction) of SignExtend
expects 32 bits, got 33.
design.sv:74:        : Pruning 1 high
bits of the expression.
design.sv:114: warning: Port 2
(ALU_INSTRUCTION) of ALU_Control
expects 10 bits, got 11.
design.sv:114:        : Pruning 1 high
bits of the expression.
design.sv:462: warning: @* is sensitive
to all 32 words in array 'Data'.
design.sv:469: warning: @* is sensitive
to all 32 words in array 'Data'.
VCD info: dumpfile dump.vcd opened for
output.
RAM[0] = 0
RAM[1] = 5
RAM[2] = 10
```

```
RAM[3] = 15
RAM[4] = 20
RAM[5] = 25
RAM[6] = 30
RAM[7] = 35
RAM[8] = 40
RAM[9] = 45
RAM[10] = 50
RAM[11] = 55
RAM[12] = 60
RAM[13] = 65
RAM[14] = 70
RAM[15] = 75
RAM[16] = 80
RAM[17] = 85
RAM[18] = 90
RAM[19] = 95
RAM[20] = 100
RAM[21] = 105
RAM[22] = 110
RAM[23] = 115
RAM[24] = 120
RAM[25] = 125
RAM[26] = 130
RAM[27] = 135
RAM[28] = 140
RAM[29] = 145
RAM[30] = 150
RAM[31] = 155
REGISTER[0] = 0
REGISTER[1] = 1
REGISTER[2] = 2
REGISTER[3] = 3
REGISTER[4] = 4
REGISTER[5] = 5
REGISTER[6] = 6
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REGISTER[9] = 9
REGISTER[10] = 10
REGISTER[11] = 11
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REGISTER[25] = 25
REGISTER[26] = 26
REGISTER[27] = 27
REGISTER[28] = 28
REGISTER[29] = 29
REGISTER[30] = 30
REGISTER[31] = 31
REGISTER[0] = 0
REGISTER[1] = 1
REGISTER[2] = 2
REGISTER[3] = 3
REGISTER[4] = 4
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REGISTER[5] = 5
REGISTER[6] = 6
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RAM[16] = 80
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RAM[18] = 90
RAM[19] = 95
RAM[20] = 100
RAM[21] = 105
RAM[22] = 110
RAM[23] = 115
RAM[24] = 120
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REGISTER[31] = 31
RAM[0] = 0
RAM[1] = 5
RAM[2] = 10
RAM[3] = 15
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RAM[5] = 25
RAM[6] = 30
RAM[7] = 35
RAM[8] = 40
RAM[9] = 45
RAM[10] = 50
RAM[11] = 55
RAM[12] = 60
RAM[13] = 65
RAM[14] = 70
RAM[15] = 75
RAM[16] = 80
RAM[17] = 85
RAM[18] = 90
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RAM[19] = 95
RAM[20] = 100
RAM[21] = 105
RAM[22] = 110
RAM[23] = 115
RAM[24] = 120
RAM[25] = 125
RAM[26] = 130
RAM[27] = 135
RAM[28] = 140
RAM[29] = 145
RAM[30] = 150
RAM[31] = 155
REGISTER[0] = 0
REGISTER[1] = 1
REGISTER[2] = 2
REGISTER[3] = 3
REGISTER[4] = 4
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REGISTER[28] = 28
REGISTER[29] = 29
REGISTER[30] = 30
REGISTER[31] = 31
Finding VCD file...
./dump.vcd
[2023-05-11 09:44:35 EDT] Opening
EPWave...
Done
```

Figure 1:

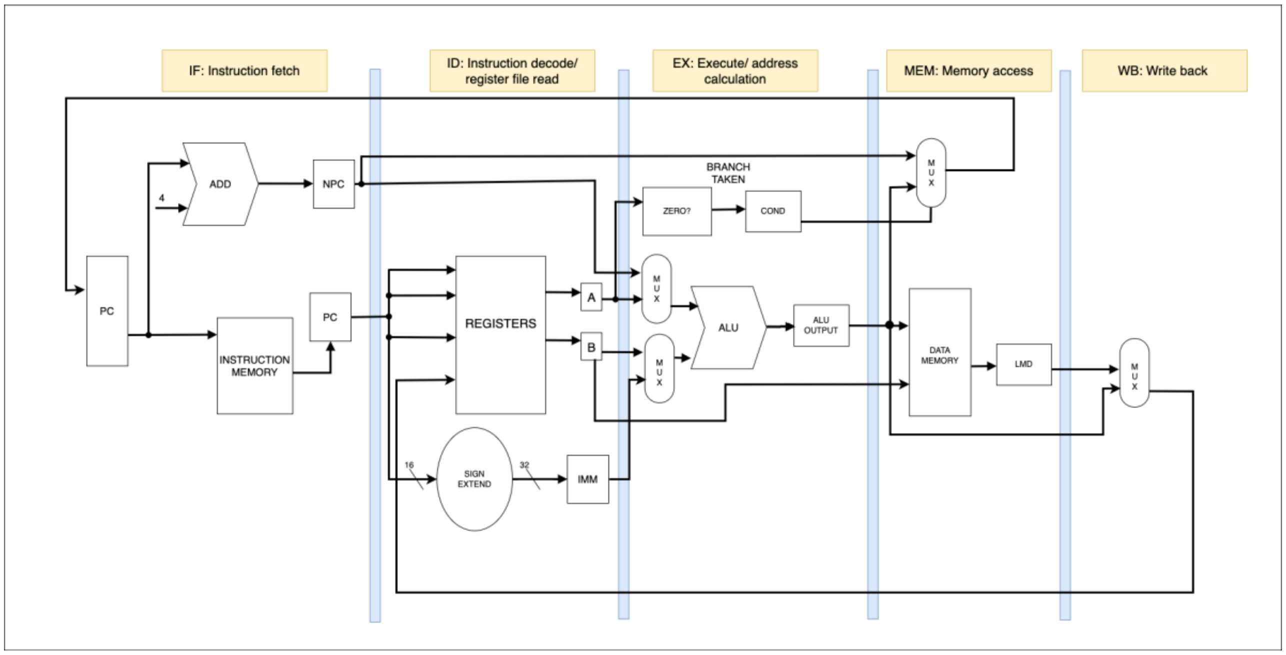
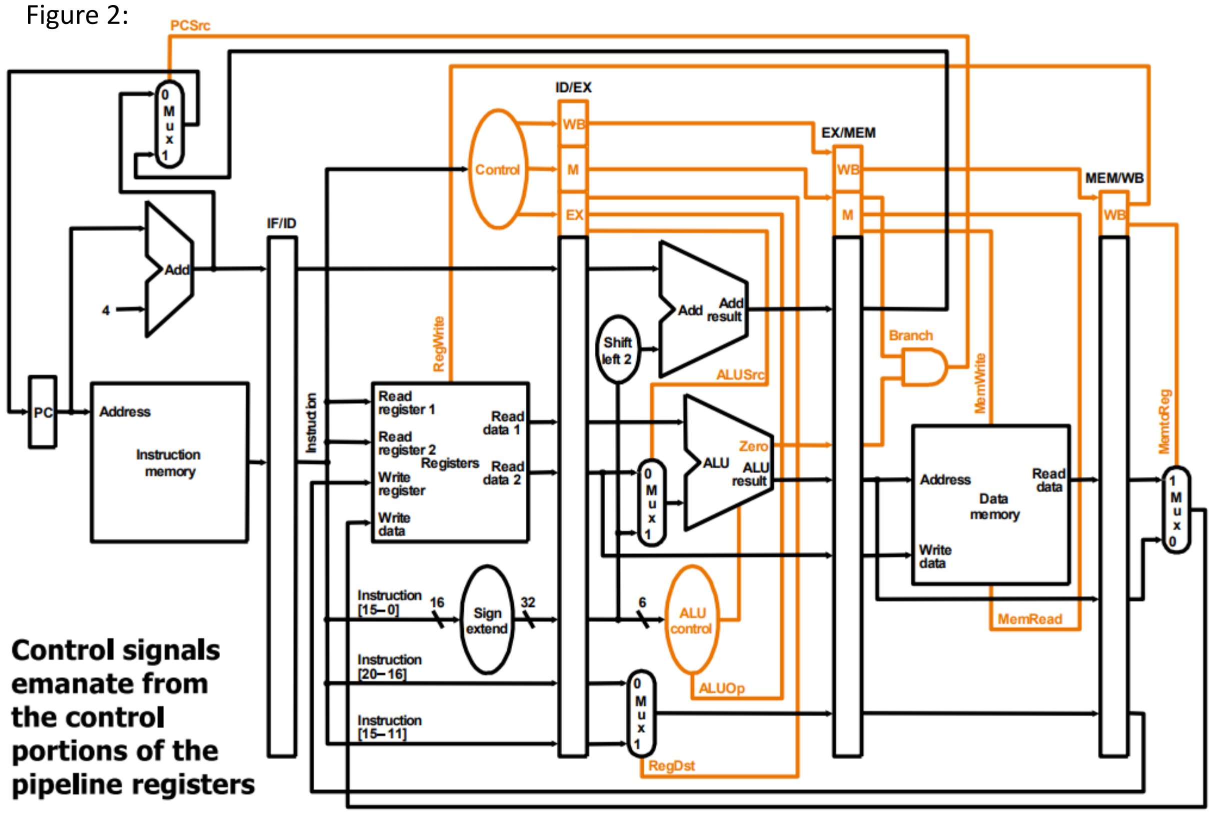
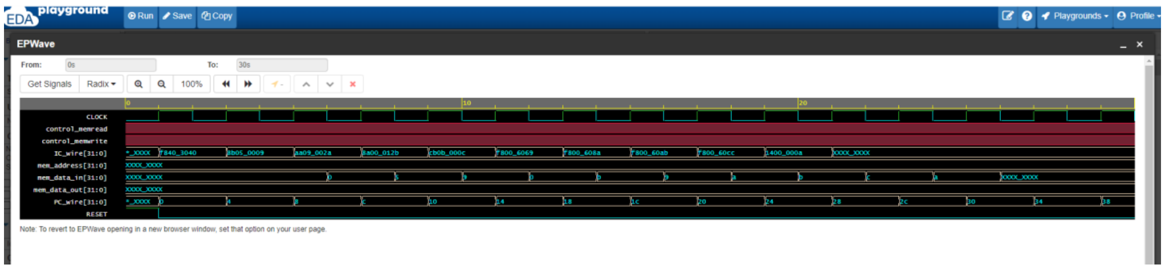


Figure 2:



Control signals emanate from the control portions of the pipeline registers

Figure 3:



```
From: 0s                To: 30s

                   0                                                10                                                20
CLOCK
control_memread
control_memwrite
IC_wire[31:0]      *_XXXX  f840_3040  8b05_0009  aa09_002a  8a00_012b  cb0b_000c  f800_6069  f800_608a  f800_60ab  f800_60cc  1400_000a  XXXX_XXXX
mem_address[31:0]  XXXX_XXXX
mem_data_in[31:0]  XXXX_XXXX  0  5  9  0  b  9  a  b  c  a  XXXX_XXXX
mem_data_out[31:0] XXXX_XXXX
PC_wire[31:0]      *_XXXX  0  4  8  c  10  14  18  1c  20  24  28  2c  30  34  38
RESET
```

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Reference:

Amazon. (n.d.) MIPS® Architecture for Programmers Volume II-A: The MIPS32® Instruction Set Manual. PDF. Amazon .

Bhardway, P. (n.d.). *Design & Simulation Of A 32-Bit Risc Based Mips Processor Using Verilog*. ReseachGate. Retrieved from https://www.researchgate.net/publication/321020107_DESIGN_SIMULATION_OF_A_32-BIT_RISC_BASED_MIPS_PROCESSOR_USING_VERILOG.

California State University, Stanislaus. (n.d.). MIPS Assembly Language Programming Tutorial. Retrieved from http://www.cs.csustan.edu/~rsc/CS3510/CS3510_17Fall/MIPSTutorial/

Harris, D., & Harris, S. (2017). Digital design and computer architecture. Morgan Kaufmann Publishers.

Hennessy, J. L., & Patterson, D. A. (2011). Computer architecture: A quantitative approach (5th ed.). Elsevier.

MIPSfpga. (n.d.). Retrieved from https://www.mipsfpga.org/

MIPS Technologies. (n.d.). Retrieved from https://www.mips.com/

Neelkshah, April 3rd 2020, MIPS- Processor, https://github.com/neelkshah/MIPS-Processor

Palnitkar, S. (2020). *Verilog HDL: A guide to digital design synthesis*. Pearson.

Patterson, D. A., & Hennessy, J. L. (2021). *Computer Organization and Design: The hardware/software interface, Arm edition*.

Quinto, Ralph and Seto, Warren, June 17^{17} 2018, ARM-LEGv8, https://github.com/nxbyte/ARM-LEGv8/tree/master/Pipeline-With-Hazard-And-Forwarding

Readler, B. C. (2014). *VHDL by example: A concise introduction for fpga design*. Full Arc Press.

Sweetman, D. (2009). See MIPS run. Morgan Kaufmann Publishers.