

FAMILIARISATION OF DSP PROCESSOR

Aim

To familiarise with the features of the **TMS320C6748** DSP Processor.

Theory

The TMS320C6748 fixed- and floating-point DSP is a low-power applications processor based on a C674x DSP core. This DSP provides significantly lower power than other members of the TMS320C6000™ platform of DSPs. The device DSP core uses a 2-level cache-based architecture. The level 1 program cache (L1P) is a 32-KB direct mapped cache, and the level 1 data cache (L1D) is a 32-KB 2-way, set-associative cache. The level 2 program cache (L2P) consists of a 256-KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by other hosts in the system, an additional 128KB of RAM shared memory is available for use by other hosts without affecting DSP performance.

FEATURES:

1. 375- and 456-MHz C674x Fixed- and Floating Point VLIW DSP.
2. **C674x** Instruction Set Features:
 - Superset of the C67x+ and C64x+ ISAs
 - Up to 3648 MIPS and 2746 MFLOPS
 - Byte-Addressable (8-, 16-, 32-, and 64-Bit Data).
 - 8-Bit Overflow Protection.
 - Bit-Field Extract, Set, Clear.
 - Normalization, Saturation, Bit-Counting.
 - Compact 16-Bit Instructions.

FUNCTIONAL BLOCK DIAGRAM

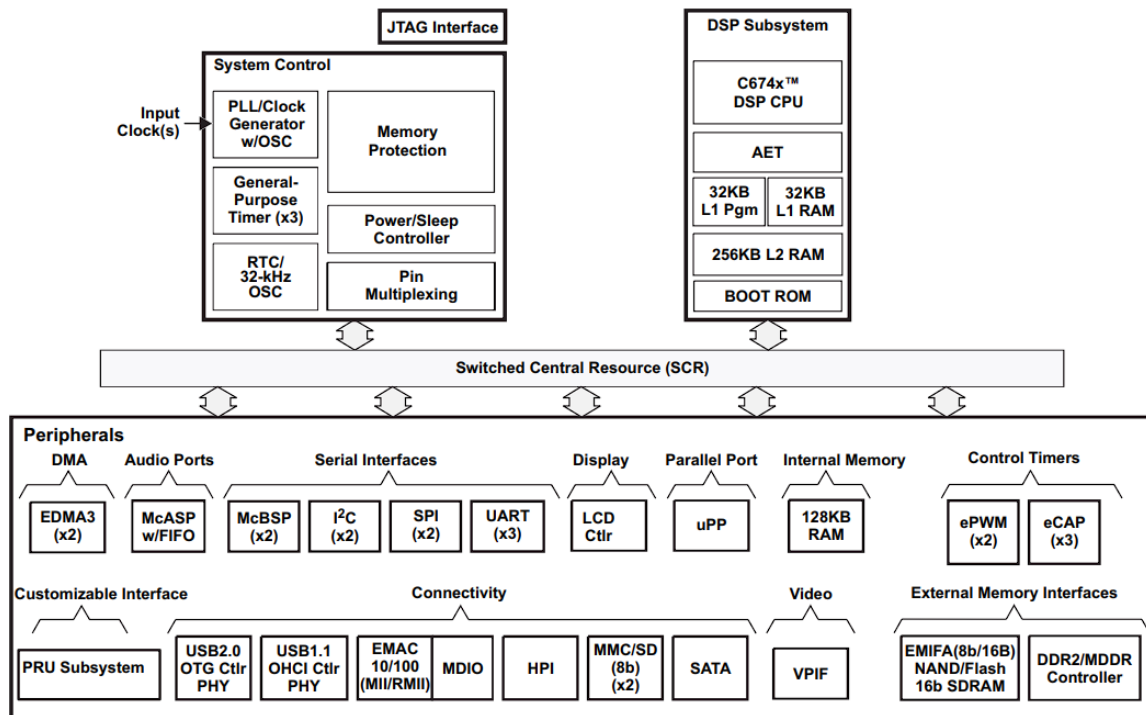


Figure 1-1. Functional Block Diagram

3. C674x Two-Level Cache Memory Architecture:

- 32KB of L1P Program RAM/Cache.
- 32KB of L1D Data RAM/Cache.
- 256KB of L2 Unified Mapped RAM/Cache.
- Flexible RAM/Cache Partition (L1 and L2).

4. Enhanced Direct Memory Access Controller 3 (EDMA3):

- 2 Channel Controllers
- 3 Transfer Controllers
- 64 Independent DMA Channels
- 16 Quick DMA Channels
- Programmable Transfer Burst Size

5. TMS320C674x Floating-Point VLIW DSP Core

- Load-Store Architecture With Nonaligned Support.
- 64 General-Purpose Registers (32-Bit).
- Six ALU (32- and 40-Bit) Functional Units.
 - Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit) and DP (IEEE Double Precision/64-Bit) Floating Point
 - Supports up to Four SP Additions Per Clock, Four DP Additions Every Two Clocks
 - Supports up to Two Floating-Point (SP or DP) Reciprocal Approximation (RCPxP) and Square-Root Reciprocal Approximation (RSQRxP) Operations Per Cycle.
- Two Multiply Functional Units:
 - Mixed-Precision IEEE Floating-Point Multiply Supported up to:
 - $2 \text{ SP} \times \text{SP} \rightarrow \text{SP}$ Per Clock
 - $2 \text{ SP} \times \text{SP} \rightarrow \text{DP}$ Every Two Clocks
 - $2 \text{ SP} \times \text{DP} \rightarrow \text{DP}$ Every Three Clocks
 - $2 \text{ DP} \times \text{DP} \rightarrow \text{DP}$ Every Four Clocks
 - Fixed-Point Multiply Supports Two 32×32 -Bit Multiplies, Four 16×16 -Bit Multiplies, or Eight 8×8 -Bit Multiplies per Clock Cycle, and Complex Multiplies.
 - Exceptions Support for Error Detection and Program Redirection.

C674x MEGAMODULE BLOCK DIAGRAM

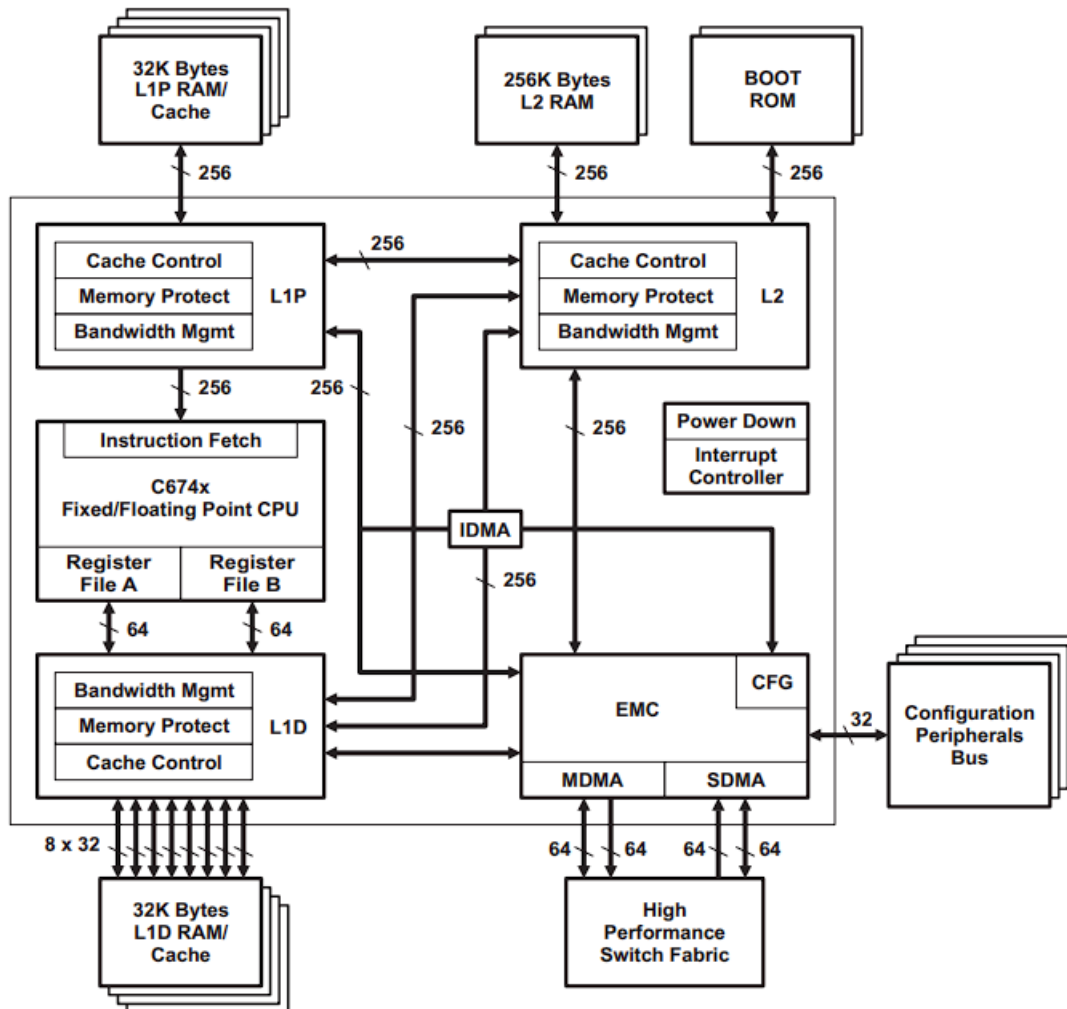


Figure 3-1. C674x Megamodule Block Diagram

6. Software Support
 - TI DSP BIOS™
 - Chip Support Library and DSP Library
7. 128KB of RAM Shared Memory
8. 1.8-V or 3.3-V LVCMOS I/O (Except for USB and DDR2 Interfaces)
9. Two Serial Peripheral Interfaces (SPIs) Each With Multiple Chip selects
10. Three Configurable 16550-Type UART Modules:
 - With Modem Control Signals
 - 16-Byte FIFO
 - 16x or 13x Oversampling Option
11. Two External Memory Interfaces:
 - **EMIFA**
 - NOR (8- or 16-Bit-Wide Data)
 - NAND (8- or 16-Bit-Wide Data)
 - 16-Bit SDRAM With 128-MB Address Space
 - DDR2/Mobile DD Memory Controller with one of the Following
 - 16-Bit DDR2 SDRAM With 256-MB Address Space
 - 16-Bit mDDR SDRAM With 256-MB Address Space
12. Serial ATA (**SATA**) Controller
 - Supports SATA I (1.5 Gbps) and SATA II (3.0 Gbps)
 - Supports All SATA Power-Management Features
 - Hardware-Assisted Native Command Queueing (NCQ) for up to 32 Entries
 - Supports Port Multiplier and Command-Based Switching

Result

Familiarised with the TMS320C6748 DSP Processor