# Scoreboard Example

nstruction stream

Instruction status:

Issue Oprand Comp Result Instruction k LD **F6** 34+**R2** LD **F2** 45+ **R3 MULTD** F0 **F4 SUBD F8 F6** F2 **DIVD** F10 **F6** 

Busy: 用于描述功能部件硬

件资源的占用情况

Op: 说明运行时所用的是哪 一个功能部件

Fi: 目标寄存器

源操作数或寄存器

是否有某个功能单

元占用源寄存器Fj或Fk。

Rj, Rk: 用于标说源寄存器

是否准备好。

Function Unit Statous:

**F6** 

des

Fi

**O**p

Read

SI

Fj

S2

Fk

Exec Write

RS

Qj

RS

Qk

Rj Rk

Clock cycle Mult1 counter

Intege No No Mult2 No

Add

F8

Time Name Busy

No

**F2** 

Divide No

Register result status:

Clock

0

**ADDD** 

FU

F0

**F2 F4**  **F6** 

F8

F10

F12

F3t

•38

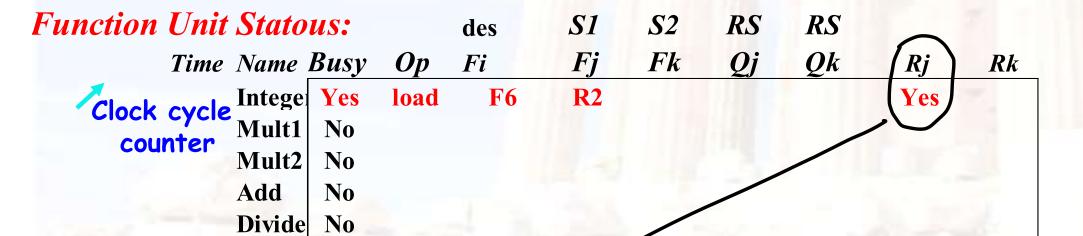
nstruction stream

n sta	tus:		Read Exec Write
n	$\boldsymbol{j}$	k	Issue Oprand Comp Result
<b>F6</b>	34+	<b>R2</b>	✓
<b>F2</b>	45+	<b>R3</b>	
<b>F0</b>	<b>F2</b>	<b>F4</b>	
<b>F8</b>	<b>F6</b>	<b>F2</b>	
F10	$\mathbf{F0}$	<b>F6</b>	440 1110
	F6 F2 F0 F8	F6 34+ F2 45+ F0 F2 F8 F6	on j k F6 34+ R2 F2 45+ R3 F0 F2 F4 F8 F6 F2

**F2** 

**F8** 

**F6** 





Clock

**ADDD** 

0





F10 F12

nstruction stream

V = 0 0 d = 0 = 0 d =	-	~4~	4
NUSTRII			
Instructi			
		~ • • • •	

Instruction	$\boldsymbol{j}$	k	
LD	<b>F6</b>	34+	<b>R2</b>
LD	<b>F2</b>	45+	<b>R3</b>
<b>MULTD</b>	F <sub>0</sub>	<b>F2</b>	<b>F4</b>
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>
DIVD	F10	$\mathbf{F0}$	<b>F6</b>
ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>

Read	Exec	Write
------	------	-------

	Read	Exec	Write
Issue	Opran	d <i>Comp</i>	Result
	✓		
			- I

看ld F2, 45, R3能否issue 由于上一条 ld F6,34,R2在使用Integer unit,结构恢
得等Integer不再busy

in-order

#### Function Unit Statous:

Time	Name	Bus
Clock cycle counter	Intege	Yes
CIOCK CYCIE	Mult1	No
counter	Mult2	No
	Add	No
	Divide	No

Qk

Rk

### Register result status:

Clock 0

F0

FU

load

**F2** 

des

Fi

**F6** 

**F4** 

SI

Fj

R2

**F6** F8 F10

F12

F30

Int

*S2* 

Fk

RS

Qj

nstruction stream

Instructio	n sta	tus:		Read Exec Write	
Instructi	ion	$oldsymbol{j}$	k	Issue Oprand Comp Resul	<u>'t</u>
LD	<b>F6</b>	34+	<b>R2</b>	✓	<b>Calculate Address</b>
LD	<b>F2</b>	45+	<b>R3</b>		
MULTD	<b>F0</b>	<b>F2</b>	<b>F4</b>		
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>		CARS. In
DIVD	<b>F10</b>	$\mathbf{F0}$	<b>F6</b>	1100 11:14	
ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>	7110 1 11	

Function Unit Statous:		des	S1	<i>S2</i>	RS	RS		
Time Name Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Clock cycle Intege Yes	load	<b>F6</b>	R2				No	
Clock cycle Intege Yes  Counter Mult1 No								
Courier National Nation								

Mult2 No Add No Divide No

### Register result status:

nstruction stream

I	structio	n sta	tus:			Read Ex	ec V	Vrite	
	Instruction	on	$oldsymbol{j}$	k	Issue	Oprand Co	mp K	Result	
	LD	<b>F6</b>	34+	R2		✓			Access Data Cache
	LD	<b>F2</b>	45+	<b>R3</b>					
	<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>					
	<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>					
	DIVD	F10	$\mathbf{F0}$	<b>F6</b>					
	ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>					

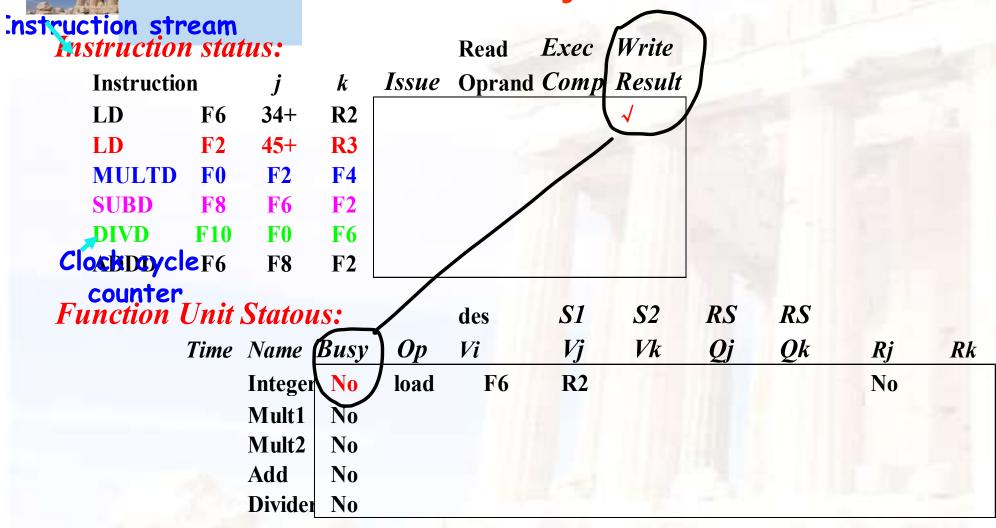
Function Unit Sta	atous:		des	S1	<i>S2</i>	RS	RS		
Time Na	ne Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Clock cycle Mu counter Mu	ege Yes	load	<b>F6</b>	R2				No	
Mu	lt1 No								
counter <sub>Mu</sub>	lt2 No								

Register result status:

Add

Divide No

No



#### Register result status:

nstruction stream

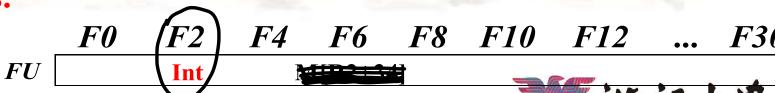
X	nstruction	n sta	tus:			Read	Exec	Write
	Instruction	on	$oldsymbol{j}$	k	Issue	Oprand	Comp	Result
	LD	<b>F6</b>	34+	<b>R2</b>				
	LD	<b>F2</b>	45+	<b>R3</b>	✓			
	<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>				
	<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>				
	DIVD	F10	F0	<b>F6</b>				
	<b>ADDD</b>	<b>F6</b>	<b>F8</b>	<b>F2</b>			77.0	

Function	Unit Statous:
	Citt Diatons.

nction	Unit	Stato	us:		des	S1	<i>S2</i>	RS	RS		
<b>7</b> 01 1.	Time	Name	Busy	Op	Vi	Vj	Vk	Qj	Qk	Rj	Rk
Clock	cycle nter	Intege Mult1	Yes No	load	F2	R3	7/1			Yes	×.
		Mult2 Add	No No								
		Divide	110								

### Register result status:

Clock



ZHEJIANG UNIVERSITY



Read

nstructio	n s	tream
instruct	ion	status:

Instruction	on	$oldsymbol{j}$	$\boldsymbol{k}$	Issue	Oprand Comp Resul
LD	<b>F6</b>	34+	<b>R2</b>		
LD	<b>F2</b>	45+	<b>R3</b>		✓
<b>MULTD</b>	<b>F0</b>	<b>F2</b>	<b>F4</b>	✓	
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>		
DIVD	F10	$\mathbf{F0}$	<b>F6</b>		
ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>		

MUITD无 Structural hazard 和WAW,故可以Issue

### Function Eynie Statous:

countene	Name	Busy	Op
	Intege	Yes	loa
	Mult1	Yes	Mu
	Mult2	No	

Divide No

Add

	des	S1
<b>)</b> p	Fi	Fj
ad	F2	R3
<b>Iul</b>	F0	<b>F2</b>

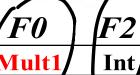
S2



Register result status:

Clock

No



**F4** 

**F6** 

Exec Write

**F8** 

RS

F10

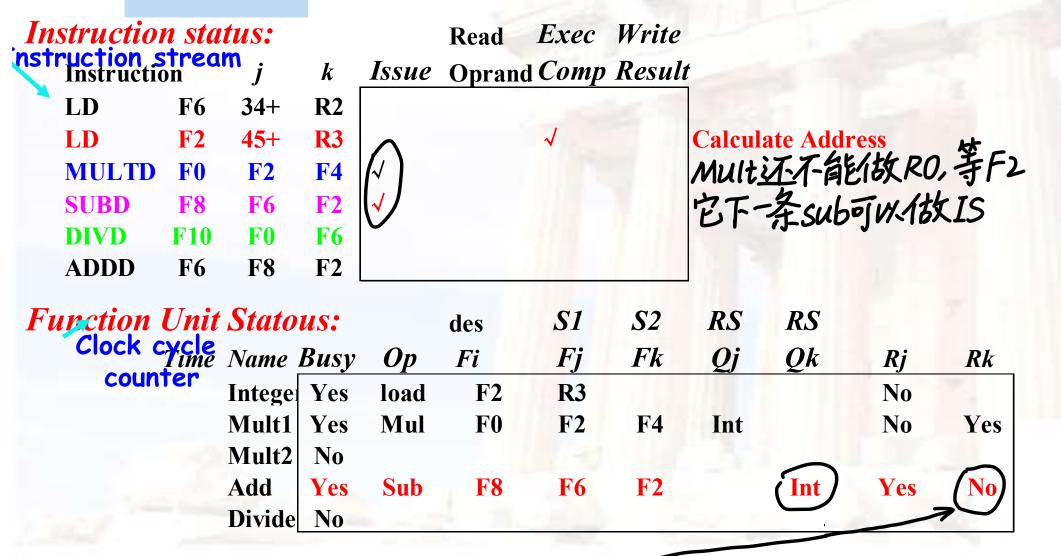
RS

F12

ZHEJIANG UNIVERSITY

•45







Clock 0 F

IJ [

F0 F2 Mult1 Int.46

F4 F6

F8

F10 F12

nstruction stream **Instruction status:** 

Exec Write Read

Issue Oprand Comp Result

Instruction LD **R2 F6** 34+ LD 45+ **R3 F4 MULTD** F<sub>0</sub> F2 **F2 SUBD F6 DIVD** F10  $\mathbf{F0}$ **F6 ADDD F6 F8 F2** 



**Access Data Cache** 

F10

F12

Function Weit Statous:

countiene

<b>&amp;</b> Statou	is:		des	S1	<i>S2</i>	RS	RS		
e Name <u>B</u>	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Intege	Yes	load	F2	R3				No	
Mult1	Yes	Mul	F0	F2	F4	Int		No	Yes
Mult2	No								
Add	Yes	Sub	<b>F8</b>	<b>F6</b>	F2		Int	Yes	No
Divide	Yes	Div	F10	$(\mathbf{F0})$	<b>F6</b>	Mult1		No	Yes

Register result status:

Clock

0

*F8* F0 *F2* **F4 F6** FUMult1 Int Add

ZHEJIANG UNIVERSITY

F30

nstruction stream **Instruction status:** 

Read Exec Write

Instruction	on	$oldsymbol{j}$	k	Issue Oprand Comp Result
LD	<b>F6</b>	34+	<b>R2</b>	
LD	<b>F2</b>	45+	<b>R3</b>	<b>√</b>
<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>	✓
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>	√
DIVD	F10	F0	<b>F6</b>	√
ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>	- FF (10) (1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

F2WB

Function Excie Statous:		des	S1	<i>S2</i>	RS	RS
countieme Name Busy	<b>O</b> p	Fi	Fj	Fk	Qj	Qk

r Name	Busy	<b>U</b> p	Fl	FJ	PK	Qj	QK	KJ	RK
Intege	No	load	F2	R3				No	
Mult1	Yes	Mul	F0	F2	F4	Int		(Yes)	Yes
Mult2	No								
Add	Yes	Sub	F8	<b>F6</b>	F2		Int	Yes	(Yes)
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock

0

FU

**F4** 

**F6** 

**F8** 

F10

F12

F30

M[R2+34] Add

Div,



nstruction stream instruction status:

Read Exec Write

Instruction	on	$\boldsymbol{j}$	k	Issue Oprand Comp Result
LD	<b>F6</b>	34+	<b>R2</b>	
LD	<b>F2</b>	45+	<b>R3</b>	
<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>	
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>	
DIVD	F10	$\mathbf{F0}$	<b>F6</b>	
ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>	100 0 11

Function Unit Statous:

t Statous:		des	S1	<i>S2</i>	RS	RS		
e Name <mark>Busy</mark>	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Intege No	load	<b>F2</b>	R3			bolk	No	
Mult1 Yes	Mul	F0	F2	F4		RO(故	No	No
Mult2 No						完		
Add Yes	Sub	<b>F8</b>	<b>F6</b>	F2			No	No
Divide Yes	Div	F10	F0	F6	Mult1		No	Yes

### Register result status:

Clock

**FU** 

**F4** 

*F6* 

F8 F1

F10 F12

12 ... F30

Add Div

Instruction status:

Read Exec Write

Instruction i k Issue Opend Comp Result

Instruction j k Issue Oprand Comp Result
LD F6 34+ R2

LD F2 45+ R3

MULTD F0 F2 F4

SUBD F8 F6 F2

DIVD F10 F6 F8 F2

Clock cycle

Function Verit Statous: des S1 S2 RS RS

Fi Fi Fk Qk Time Name Busy **O**p Qj Rk Rj Intege No load **F2 R3** No Mult1 Yes Mul F<sub>0</sub> F2 F4No No Mult2 No Add **F8 F6** F2 Yes Sub No No Divide Yes Div F10 F0 **F6** Mult1 No Yes

### Register result status:

Clock 0

**FU** 

F0 F2
Mult1

F4 F6

**F8 F10** Add Div

**Assume Mul takes 7 cycles** 

**Assume Sub takes 3 cycles** 

F12 ... F30 ZHEJIANG UNIVERSITY

nstructio	n stream
instructi	on status

Read	Exec	Write
------	------	-------

Instruction	n	j	k	Issue Oprand Comp Result
LD	<b>F6</b>	34+	<b>R2</b>	
LD	<b>F2</b>	45+	<b>R3</b>	
<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>	✓ Assume Mul takes 7 cycles
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>	✓ Assume Sub takes 3 cycles
DIVD	F10	F0	<b>F6</b>	✓
ADDD	F6	F8	<b>F2</b>	

Function	mit	State	ous:
I WITCHWOOD THE			

urtienit	Stato	us:		des	S1	<i>S2</i>	RS	RS		
Time	Name	Busy	<b>O</b> p	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Intege	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	No	Sub	<b>F8</b>	F6	F2			No	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

**S**2

S1

### Register result status:

Clock 0

FU

F0

Mult1

*F2* **F4** 

**F6** 

**F8** 

RS

F10 *F12* 

Div,

F30

nstructio	n stream
	on status:

Read	Exec	Write
Keaa	Exec	yy riie

Instruction	on	j	$\boldsymbol{k}$	Issue Oprand Comp Resul	t
LD	<b>F6</b>	34+	<b>R2</b>		The same of the sa
LD	<b>F2</b>	45+	<b>R3</b>		
<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>	<b>√</b>	<b>Assume Mul takes 7 cycles</b>
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>		
DIVD	<b>F10</b>	$\mathbf{F0}$	<b>F6</b>	✓	
<b>ADDD</b>	<b>F6</b>	<b>F8</b>	<b>F2</b>	✓	Sub用完加法FU

Function	Unit Statous:	des
----------	---------------	-----

Unit State	ous:		des	S1	<b>S</b> 2	RS	RS		
Time Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Intege	No	load	F2	R3				No	
Mult1	Yes	Mul	F0	F2	F4			No	No
Mult2	No								
Add	Yes	<b>ADD</b>	<b>F6</b>	<b>F8</b>	<b>F2</b>			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

ZHEJIANG UNIVERSITY

### Register result status:

Clock F0 *F2* **F4 F6 F8** F10 F12 F30 Mult1 FU0 Add Div

nstruction stream instruction status:

cec Write

Instruction	on	j	k	Issue Oprand Comp Result	
LD	<b>F6</b>	34+	<b>R2</b>		The state of the s
LD	<b>F2</b>	45+	<b>R3</b>		
MULTD	F0	<b>F2</b>	<b>F4</b>	✓	Assume Mul takes 7 cycles
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>		
DIVD	F10	$\mathbf{F0}$	<b>F6</b>	✓	
ADDD	<b>F6</b>	<b>F8</b>	<b>F2</b>	✓	

Function Unit Statous:	des	S1	<i>S2</i>	RS	RS
------------------------	-----	----	-----------	----	----

Time Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Intege	No	load	F2	R3				No	
Mult1	Yes	Mul	F0	F2	F4			No	No
Mult2	No								
Add	Yes	ADD	<b>F6</b>	F8	F2			No	No
Divide	Yes	Div	F10	F0	<b>F6</b>	Mult1		No	Yes

ZHEJIANG UNIVERSITY

### Register result status:

nstruction stream instruction status:

Instructi	on	j	$\boldsymbol{k}$	Issue Oprand Comp Result	
LD	<b>F6</b>	34+	<b>R2</b>		
LD	<b>F2</b>	45+	<b>R3</b>		The State of the S
<b>MULTD</b>	<b>F0</b>	<b>F2</b>	<b>F4</b>	<b>√</b>	Last cycle of Mul
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>		
DIVD	F10	F0	<b>F6</b>	√	
ADDD	<b>F6</b>	F8	<b>F2</b>	<b>√</b>	1

Function U	nit Statous:	des	S1	S2	RS	
	III DIMIUMS.	ucs		02		

Time Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Intege	No	load	F2	R3				No	
Mult1	Yes	Mul	F0	F2	F4			No	No
Mult2	No								
Add	Yes	<b>ADD</b>	<b>F6</b>	F8	F2			No	No
Divide	Yes	Div		F0	<b>F6</b>	Mult1		No	Yes

RS

ZHEJIANG UNIVERSITY

### Register result status:

Clock F0 F2 F4 F6 F8 F10 F12 ... F30

nstruction stream instruction status:

Read	Exec	Write
------	------	-------

Instruction	on	$oldsymbol{j}$	$\boldsymbol{k}$	Issue	Oprand Comp	Result
LD	<b>F6</b>	34+	<b>R2</b>			
LD	<b>F2</b>	45+	<b>R3</b>			
<b>MULTD</b>	F0	<b>F2</b>	<b>F4</b>			<b>√</b>
<b>SUBD</b>	<b>F8</b>	<b>F6</b>	<b>F2</b>			
DIVD	F10	F0	<b>F6</b>	√		7
ADDD	<b>F6</b>	F8	<b>F2</b>		<b>√</b>	7.10

Function Unit Statous:	dec	S1	<b>S</b> 2	RS	R
Function Onli Statous.	aes	31	32	AS	A

Time Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Intege	No	load	F2	R3				No	
Mult1	No	Mul	F0	F2	<b>F4</b>			No	No
Mult2	No								
Add	Yes	<b>ADD</b>	<b>F6</b>	F8	F2			No	No
Divide	Yes	Div	F10	F0	F6	Mult1		Yes	Yes

ZHEJIANG UNIVERSITY

### Register result status:

Clock F0 F2 F4 F6 F8 F10 F12 ... F30