Scoreboard Example

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Busy：用于描述功能部件硬件资源的占用情况
Op：说明运行时所用的是哪一个功能部件
Fi：目标寄存器
Fj，Fk：源操作数或寄存器
Qj，Qk：是否有某个功能单元占用源寄存器Fj或Fk。
Rj，Rk：用于标识源寄存器是否准备好。

Function Unit Statous:

Clock cycle counter

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU									

Scoreboard Cycle 1

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2	√			
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Function Unit Statous:

Clock cycle counter

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Integer	Yes	load	F6	R2				Yes	
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Register result status:

Clock	F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU			Int					

Scoreboard Cycle 2

in-order ↑

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2		√		
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

看ld F2,45,R3能否issue
由于上一条ld F6,34,R2在
使用Integer unit，结构冲突
得等Integer不再busy

R0做完

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	Yes	load	F6	R2				No	
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Clock cycle counter

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU				Int					

Scoreboard Cycle 3

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2			√	
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Calculate Address

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	Yes	load	F6	R2				No	
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Clock cycle counter

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU				Int					

Scoreboard Cycle 4

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2			√	
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Access Data Cache

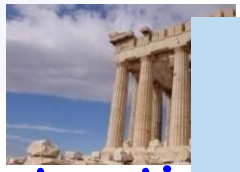
Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	Yes	load	F6	R2				No	
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Clock cycle counter

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU				Int					



Scoreboard Cycle 5

Instruction stream

Clock cycle counter

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				√
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Function Unit Statous:

Time	Name	Busy	Op	des Vi	S1 Vj	S2 Vk	RS Qj	RS Qk	Rj	Rk
	Integer	No	load	F6	R2				No	
	Mult1	No								
	Mult2	No								
	Add	No								
	Divider	No								

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU				[redacted]					

Scoreboard Cycle 6

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3	√			
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

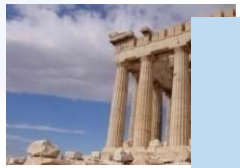
Function Unit Statous:

Clock cycle counter

Time	Name	Busy	Op	des Vi	S1 Vj	S2 Vk	RS Qj	RS Qk	Rj	Rk
	Intege	Yes	load	F2	R3				Yes	
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU		Int		[redacted]					



Scoreboard Cycle 7

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3		√		
MULTD	F0	F2	F4	√			
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

MUITD无structural hazard
和WAW，故可以Issue

Clock Cycle counter

Function Unit Statous:

Time	Name	Busy	Op	Fi	Fj	Fk	RS Qj	RS Qk	Rj	Rk
	Intege	Yes	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4	Int		No	Yes
	Mult2	No								
	Add	No								
	Divide	No								

R0做完

F2要等ld F2,45,R3

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F.
0	FU	Mult1	Int							

Scoreboard Cycle 8

Instruction status:

Instruction stream

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2	√		√	
LD	F2	45+	R3	√			
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Calculate Address

Mult还不能做RO, 等F2

它下一条sub可以做IS

Function Unit Statous:

Clock cycle counter

Time

Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
Integer	Yes	load	F2	R3				No	
Mult1	Yes	Mul	F0	F2	F4	Int		No	Yes
Mult2	No								
Add	Yes	Sub	F8	F6	F2		Int	Yes	No
Divide	No								

Register result status:

Clock	F0	F2	F4	F6	F8	F10	F12	F30
0	FU	Mult1	Int.	[redacted]			Add	

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Scoreboard Cycle 9

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2	√	√	√	
LD	F2	45+	R3	√	√		
MULTD	F0	F2	F4	√			
SUBD	F8	F6	F2	√	√		
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2	√			

都在等R2

Access Data Cache

Function Unit Statous:

Clock cycle counter

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Integer	Yes	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4	Int		No	Yes
	Mult2	No								
	Add	Yes	Sub	F8	F6	F2		Int	Yes	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	Int		[illegible]	Add	Div			

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Scoreboard Cycle 10

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				√
MULTD	F0	F2	F4	√			
SUBD	F8	F6	F2	√			
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2				

F2WB

Clock cycle counter

Functional Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Integer	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4	~~Int~~		Yes	Yes
	Mult2	No								
	Add	Yes	Sub	F8	F6	F2		~~Int~~	Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	~~MUL~~		M[R2+3	Add	Div			

Scoreboard Cycle 11

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3			√	
MULTD	F0	F2	F4			√	
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2	√			

Clock cycle counter

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	Yes	Sub	F8	F6	F2			No	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

RO做完

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	[illegible]		[illegible]	Add	Div			

Scoreboard Cycle 12

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4			√	
SUBD	F8	F6	F2			√	
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2				

Assume Mul takes 7 cycles

Assume Sub takes 3 cycles

Clock cycle counter

Function Unit Statous:

Time	Name	Busy	Op	Fi	Fj	Fk	des Qj	S1 Qk	S2 Rj	RS Rk
	Intege	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	Yes	Sub	F8	F6	F2			No	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	[redacted]		[redacted]	Add	Div			

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Scoreboard Cycle 15

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4			√	
SUBD	F8	F6	F2				√
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2				

Assume Mul takes 7 cycles

Assume Sub takes 3 cycles

Clock cycle counter

Function Unit Statous:

Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	No	Sub	F8	F6	F2			No	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	[redacted]		[redacted]	[redacted]	Div			

Scoreboard Cycle 16

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4			√	
SUBD	F8	F6	F2				
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2	√			

Assume Mul takes 7 cycles

sub用完加法FU

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	Yes	ADD	F6	F8	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	[redacted]		Add	[redacted]	Div			

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Scoreboard Cycle 17

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4			√	
SUBD	F8	F6	F2				
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2		√		

Assume Mul takes 7 cycles

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	Yes	ADD	F6	F8	F2			No	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	[redacted]		Add	[redacted]	Div			

Scoreboard Cycle 18

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4			√	
SUBD	F8	F6	F2				
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2			√	

Last cycle of Mul

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	No	load	F2	R3				No	
	Mult1	Yes	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	Yes	ADD	F6	F8	F2			No	No
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	Mult1	[redacted]		Add	[redacted]	Div			

Scoreboard Cycle 19

nstruction stream

Instruction status:

Instruction		j	k	Issue	Read Oprand	Exec Comp	Write Result
LD	F6	34+	R2				
LD	F2	45+	R3				
MULTD	F0	F2	F4				√
SUBD	F8	F6	F2				
DIVD	F10	F0	F6	√			
ADDD	F6	F8	F2			√	

Function Unit Statous:

Time	Name	Busy	Op	des Fi	S1 Fj	S2 Fk	RS Qj	RS Qk	Rj	Rk
	Intege	No	load	F2	R3				No	
	Mult1	No	Mul	F0	F2	F4			No	No
	Mult2	No								
	Add	Yes	ADD	F6	F8	F2			No	No
	Divide	Yes	Div	F10	F0	F6	~~Mult1~~		Yes	Yes

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
0	FU	[redacted]			Add	[redacted]	Div			