# Homework

Suppose：

Add instruction needs 2 clock cycles. Multiply instruction needs 10 clock cycles. Division instruction needs 40 clock cycles. LD instruction need 1 clock cycles.

```
 FLD        F6, 34（R2）
 FLD        F2, 45（R3）
FMUL.D      F0, F2, F4
FSUB.D      F8, F2, F6
FDIV.D      F10, F0, F6
FADD.D      F6, F8, F2
```

How many cycles does it take to finish each instruction using the following two methods?

(1) Scoreboard algorithm

(2) Tomasulo's approach

# (1) Scoreboard algorithm

| | IS | RO | EX | WB |
|---|---|---|---|---|
| LD | 1 | 1 | 1 | 1 |
| MUL | 1 | 1 | 10 | 1 |
| SUB | 1 | 1 | 2 | 1 |
| DIV | 1 | 1 | 40 | 1 |
| ADD | 1 | 1 | 2 | 1 |

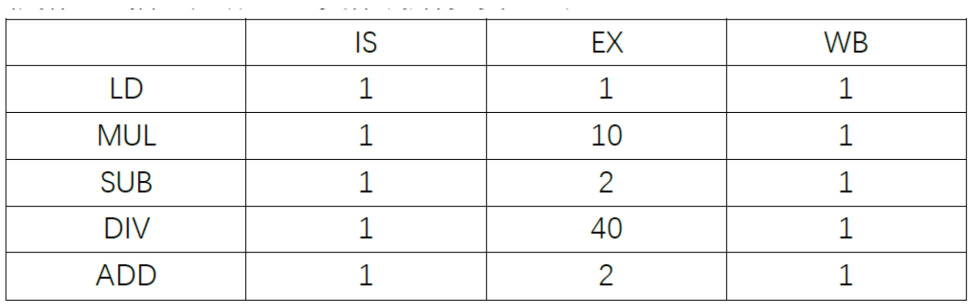
| inst | Fi | Fj | Fk | is | ro | ex | wb |
|---|---|---|---|---|---|---|---|
| L.D | F6 | 34+R2 | | 1 | 2 | 3 | 4 |
| L.D | F2 | 45+R3 | | 5 | 6 | 7 | 8 |
| MUL.D | F0 | F2 | F4 | 6 | 9 | 10~19 | 20 |
| SUB.D | F8 | F2 | F6 | 7 | 9 | 10~11 | 12 |
| DIV.D | F10 | F0 | F6 | 8 | 21 | 22~61 | 62 |
| ADD.D | F6 | F8 | F2 | 13 | 14 | 15~16 | 22 |

| Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| FLD F6, 34(R2) | 🟥 | 🟨 | 🟦 | 🟩 | | | | |
| FLD F2, 45(R3) | | | | | 🟥 | 🟨 | 🟦 | 🟩 |
| FMUL.D F0, F2, F4 | | | | | | 🟥 | | |
| FSUB.D F8, F6, F2 | | | | | | | 🟥 | |
| FDIV.D F10, F0, F6 | | | | | | | | 🟥 |
| FADD.D F6, F8, F2 | | | | | | | | |

| Instruction | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|
| FLD F6, 34(R2) | | | | | | | | |
| FLD F2, 45(R3) | | | | | | | | |
| FMUL.D F0, F2, F4 | 🟨 | 🟦 | 🟦 | 🟦 | 🟦 | 🟦 | 🟦 | 🟦 |
| FSUB.D F8, F6, F2 | 🟨 | 🟦 | 🟦 | 🟩 | | | | |
| FDIV.D F10, F0, F6 | | | | | | | | |
| FADD.D F6, F8, F2 | | | | | 🟥 | 🟨 | 🟦 | 🟦 |

| Instruction | 17 | 18 | 19 | 20 | 21 | 22 | … | … | 61 | 62 |
|---|---|---|---|---|---|---|---|---|---|---|
| FLD F6, 34(R2) | | | | | | | | | | |
| FLD F2, 45(R3) | | | | | | | | | | |
| FMUL.D F0, F2, F4 | 🟦 | 🟦 | 🟦 | 🟩 | | | | | | |
| FSUB.D F8, F6, F2 | | | | | | | | | | |
| FDIV.D F10, F0, F6 | | | | | 🟨 | 🟦 | 🟦 | 🟦 | 🟦 | 🟩 |
| FADD.D F6, F8, F2 | | | | | | 🟩 | | | | |

# (2) Tomasulo's approach



| | IS | EX | WB |
|---|---|---|---|
| LD | 1 | 1 | 1 |
| MUL | 1 | 10 | 1 |
| SUB | 1 | 2 | 1 |
| DIV | 1 | 40 | 1 |
| ADD | 1 | 2 | 1 |

| inst | Fi | Fj | Fk | is | ex | wb |
|---|---|---|---|---|---|---|
| L.D | F6 | 34+R2 | | 1 | 3 | 4 |
| L.D | F2 | 45+R3 | | 2 | 4 | 5 |
| MUL.D | F0 | F2 | F4 | 3 | 6~15 | 16 |
| SUB.D | F8 | F2 | F6 | 4 | 6~7 | 8 |
| DIV.D | F10 | F0 | F6 | 5 | 17~56 | 57 |
| ADD.D | F6 | F8 | F2 | 6 | 9~10 | 11 |

| Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| FLD F6, 34(R2) | 🟥 | | 🟦 | 🟩 | | | | |
| FLD F2, 45(R3) | | 🟥 | | 🟦 | 🟩 | | | |
| FMUL.D F0, F2, F4 | | | 🟥 | | | 🟦 | 🟦 | 🟦 |
| FSUB.D F8, F6, F2 | | | | 🟥 | | 🟦 | 🟦 | 🟩 |
| FDIV.D F10, F0, F6 | | | | | 🟥 | | | |
| FADD.D F6, F8, F2 | | | | | | 🟥 | | |

| Instruction | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17~56 | 57 |
|---|---|---|---|---|---|---|---|---|---|---|
| FLD F6, 34(R2) | | | | | | | | | | |
| FLD F2, 45(R3) | | | | | | | | | | |
| FMUL.D F0, F2, F4 | 🟦 | 🟦 | 🟦 | 🟦 | 🟦 | 🟦 | 🟦 | 🟩 | | |
| FSUB.D F8, F6, F2 | | | | | | | | | 🟦 | 🟩 |
| FDIV.D F10, F0, F6 | | | | | | | | | | |
| FADD.D F6, F8, F2 | 🟦 | 🟦 | 🟩 | | | | | | | |

# Hardware-Based Speculation

Cache for uncommitted instruction results:

3 fields: instruction type, destination address, value

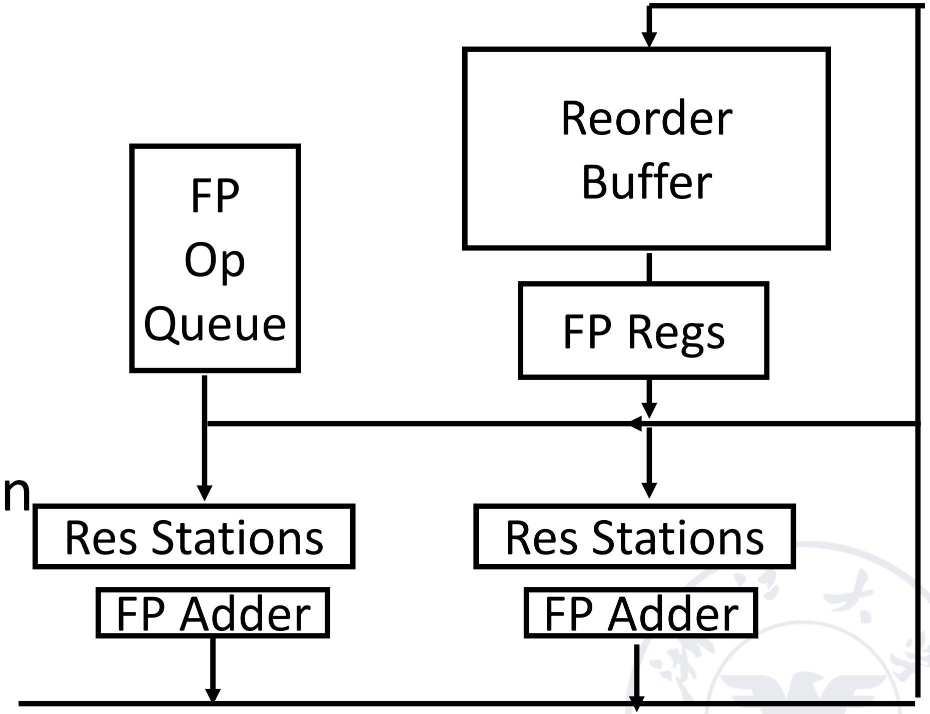
1. When the program execution phase is completed, replace the value in RS with the number of ROB

2. Increase instruction submission stage

3. ROB provides the number of operations in the completion phase and the commit phase

4. Once the operand is submitted, the result is written to the register

5. In this way, when the prediction fails, it is easy to restore the inferred execution instruction, or when an exception occurs, it is easy to restore the state



# Hardware-Based Speculation

Suppose：

- Add instruction needs 2 clock cycles. Multiply instruction needs 10 clock cycles. Division instruction needs 40 clock cycles. LD instruction need 1 clock cycles.

```
FLD       F6, 34(R2)
FLD       F2, 45(R3)
FMUL.D    F0, F2, F4
FSUB.D    F8, F2, F8
FDIV.D    F10, F0, F6
FADD.D    F6, F8, F2
```

- How many cycles does it take to finish each instruction using Hardware-Based Speculation?

# Tomasulo with Reorder Buffer - Cycle 0

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | | | | | | | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | No | | | | | | | |

**Reservation Stations**

| | Busy | Instruction | Status | Object | Value |
|---|---|---|---|---|---|
| 1 | no | | | | |
| 2 | no | | | | |
| 3 | no | | | | |
| 4 | no | | | | |
| 5 | no | | | | |
| 6 | no | | | | |

| | Busy | Instruction |
|---|---|---|
| Load1 | | |
| Load2 | | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | | | | | |
| Busy | no | no | no | no | no | no | … | no |

# Tomasulo with Reorder Buffer - Cycle 1

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | | | | | | | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | No | | | | | | | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | Yes | FLD F6, 34(R2) | Issue | F6 | |
| 2 | no | | | | |
| 3 | no | | | | |
| 4 | no | | | | |
| 5 | no | | | | |
| 6 | no | | | | |

| | Busy | Instruction |
|---|---|---|
| Load1 | Yes | 34 + Regs[R2] |
| Load2 | | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | #1 | | | | |
| Busy | no | no | no | Yes | no | no | … | no |

# Tomasulo with Reorder Buffer - Cycle 2

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | | | | | | | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | No | | | | | | | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | Yes | FLD F6, 34(R2) | Issue | F6 | Mem[load1] |
| 2 | Yes | FLD F2, 45(R3) | Issue | F2 | |
| 3 | no | | | | |
| 4 | no | | | | |
| 5 | no | | | | |
| 6 | no | | | | |

| | Busy | Instruction |
|---|---|---|
| Load1 | Yes | 34 + Regs[R2] |
| Load2 | Yes | 45 + Regs[R3] |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | #2 | | #1 | | | | |
| Busy | no | Yes | no | Yes | no | no | … | no |

# Tomasulo with Reorder Buffer - Cycle 3

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | | | | | | | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | | Regs[F4] | #2 | | #3 | |
| Mult2 | No | | | | | | | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | Yes | FLD F6, 34(R2) | Ex1 | F6 | Mem[load1] |
| 2 | Yes | FLD F2, 45(R3) | Issue | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Issue | F0 | |
| 4 | no | | | | |
| 5 | no | | | | |
| 6 | no | | | | |

| | Busy | Instruction |
|---|---|---|
| Load1 | Yes | 34 + Regs[R2] |
| Load2 | Yes | 45 + Regs[R3] |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | #2 | | #1 | | | | |
| Busy | Yes | Yes | no | Yes | no | no | … | no |

# Tomasulo with Reorder Buffer - Cycle 4

|  | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | Yes | Sub | Regs[F6] | Mem[45+Regs[R3]] |  |  | #4 |  |
| Add2 | No |  |  |  |  |  |  |  |
| Add3 | No |  |  |  |  |  |  |  |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] |  |  | #3 |  |
| Mult2 | No |  |  |  |  |  |  |  |

**Reservation Stations**

|  | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | Yes | FLD F6, 34(R2) | write | F6 | Mem[load1] |
| 2 | Yes | FLD F2, 45(R3) | Ex1 | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Issue | F0 |  |
| 4 | Yes | FSUB.D F8, F6, F2 | Issue | F8 |  |
| 5 | no |  |  |  |  |
| 6 | no |  |  |  |  |

|  | Busy | Instruction |
|---|---|---|
| Load1 | Yes | 34 + Regs[R2] |
| Load2 | Yes | 45 + Regs[R3] |
| Load3 |  |  |

**Reorder Buffer**

|  | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | #2 |  | #1 | #4 |  |  |  |
| Busy | Yes | Yes | no | Yes | Yes | no | … | no |

# Tomasulo with Reorder Buffer - Cycle 5

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | Yes | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | No | | | | | | | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | Yes | FLD F2, 45(R3) | write | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Issue | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | Issue | F8 | |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | no | | | | |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | #2 | | | #4 | #5 | | |
| Busy | Yes | Yes | no | no | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 6

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | Yes | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | Yes | Add | | Regs[F2] | #4 | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex1 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | Ex1 | F8 | |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | Issue | F6 | |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 7

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | Yes | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex2 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | Ex2 | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | Issue | F6 | |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 8

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | Yes | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

## Reservation Stations

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex3 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | Issue | F6 | |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

## Reorder Buffer

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 9

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | Yes | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

Reservation Stations

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex4 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | Ex1 | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

Reorder Buffer

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 10

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | Yes | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex5 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | Ex2 | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 11

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex6 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 12

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | | Regs[F6] | #3 | | #5 | |

## Reservation Stations

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex7 | F0 | |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

## Reorder Buffer

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 13

|  | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] |  |  | #4 |  |
| Add2 | No | Add | #4 | Regs[F2] |  |  | #6 |  |
| Add3 | No |  |  |  |  |  |  |  |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] |  |  | #3 |  |
| Mult2 | Yes | Div |  | Regs[F6] | #3 |  | #5 |  |

**Reservation Stations**

|  | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex8 | F0 |  |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 |  |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

|  | Busy | Instruction |
|---|---|---|
| Load1 | no |  |
| Load2 | no |  |
| Load3 |  |  |

**Reorder Buffer**

|  | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 |  |  | #6 | #4 | #5 |  |  |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 14

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | #2 * Regs[F4] | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex9 | F0 | #2 * Regs[F4] |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 15

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | Yes | Mul | Mem(45+Regs[R3]) | Regs[F4] | | | #3 | |
| Mult2 | Yes | Div | #2 * Regs[F4] | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | Ex10 | F0 | #2 * Regs[F4] |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 | | | #6 | #4 | #5 | | |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 16

|  | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] |  |  | #4 |  |
| Add2 | No | Add | #4 | Regs[F2] |  |  | #6 |  |
| Add3 | No |  |  |  |  |  |  |  |
| Mult1 | No | Mul | Mem(45+Regs[R3]) | Regs[F4] |  |  | #3 |  |
| Mult2 | Yes | Div | #2 * Regs[F4] | Regs[F6] | #3 |  | #5 |  |

**Reservation Stations**

|  | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | Yes | FMUL.D F0, F2, F4 | write | F0 | #2 * Regs[F4] |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Issue | F10 |  |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

|  | Busy | Instruction |
|---|---|---|
| Load1 | no |  |
| Load2 | no |  |
| Load3 |  |  |

**Reorder Buffer**

|  | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | #3 |  |  | #6 | #4 | #5 |  |  |
| Busy | Yes | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 17

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | Sub | Regs[F6] | Mem[45+Regs[R3]] | | | #4 | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | Yes | Div | #2 * Regs[F4] | Regs[F6] | #3 | | #5 | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | no | FMUL.D F0, F2, F4 | commit | F0 | #2 * Regs[F4] |
| 4 | Yes | FSUB.D F8, F6, F2 | write | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Ex1 | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

Need 39 more EX cycles for DIV to finish

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | #6 | #4 | #5 | | |
| Busy | no | no | no | Yes | Yes | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 18

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | Yes | Div | #2 * Regs[F4] | Regs[F6] | #3 | | #5 | |

Reservation Stations

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | no | FMUL.D F0, F2, F4 | commit | F0 | #2 * Regs[F4] |
| 4 | no | FSUB.D F8, F6, F2 | commit | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Ex2 | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

Reorder Buffer

Need 38 more EX cycles for DIV to finish

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | #6 | | #5 | | |
| Busy | no | no | no | Yes | no | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 56

Reservation Stations

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | Yes | Div | #2 * Regs[F4] | Regs[F6] | #3 | | #5 | |

Reorder Buffer

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | no | FMUL.D F0, F2, F4 | commit | F0 | #2 * Regs[F4] |
| 4 | no | FSUB.D F8, F6, F2 | commit | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | Ex40 | F10 | |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | #6 | | #5 | | |
| Busy | no | no | no | Yes | no | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 57

Reservation Stations

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | No | Div | #2 * Regs[F4] | Regs[F6] | #3 | | #5 | |

Reorder Buffer

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | no | FMUL.D F0, F2, F4 | commit | F0 | #2 * Regs[F4] |
| 4 | no | FSUB.D F8, F6, F2 | commit | F8 | F6 - #2 |
| 5 | Yes | FDIV.D F10, F0, F6 | write | F10 | #3/F6 |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | #6 | | #5 | | |
| Busy | no | no | no | Yes | no | Yes | … | no |

# Tomasulo with Reorder Buffer - Cycle 58

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | Add | #4 | Regs[F2] | | | #6 | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | No | | | | | | | |

**Reservation Stations**

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | no | FMUL.D F0, F2, F4 | commit | F0 | #2 * Regs[F4] |
| 4 | no | FSUB.D F8, F6, F2 | commit | F8 | F6 - #2 |
| 5 | no | FDIV.D F10, F0, F6 | commit | F10 | #3/F6 |
| 6 | Yes | FADD.D F6, F8, F2 | write | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

**Reorder Buffer**

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | #6 | | | | |
| Busy | no | no | no | Yes | no | no | … | no |

# Tomasulo with Reorder Buffer - Cycle 59

| | Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
|---|---|---|---|---|---|---|---|---|
| Add1 | No | | | | | | | |
| Add2 | No | | | | | | | |
| Add3 | No | | | | | | | |
| Mult1 | No | | | | | | | |
| Mult2 | No | | | | | | | |

Reservation Stations

| | Busy | Instruction | Status | Dest | Value |
|---|---|---|---|---|---|
| 1 | no | FLD F6, 34(R2) | commit | F6 | Mem[load1] |
| 2 | no | FLD F2, 45(R3) | commit | F2 | Mem[load2] |
| 3 | no | FMUL.D F0, F2, F4 | commit | F0 | #2 * Regs[F4] |
| 4 | no | FSUB.D F8, F6, F2 | commit | F8 | F6 - #2 |
| 5 | no | FDIV.D F10, F0, F6 | commit | F10 | #3/F6 |
| 6 | no | FADD.D F6, F8, F2 | commit | F6 | #4 + F2 |

| | Busy | Instruction |
|---|---|---|
| Load1 | no | |
| Load2 | no | |
| Load3 | | |

Reorder Buffer

| | F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
|---|---|---|---|---|---|---|---|---|
| ROB | | | | | | | | |
| Busy | no | no | no | no | no | no | … | no |

# Tomasulo with Reorder Buffer - Summary

| Instruction | Issue | Exec Comp | Writeback | Commit |
|---|---|---|---|---|
| FLD F6, 34(R2) | 1 | 3 | 4 | 5 |
| FLD F2, 45(R3) | 2 | 4 | 5 | 6 |
| FMUL.D F0, F2, F4 | 3 | 6-15 | 16 | 17 |
| FSUB.D F8, F6, F2 | 4 | 6-7 | 8 | 18 |
| FDIV.D F10, F0, F6 | 5 | 17-56 | 57 | 58 |
| FADD.D F6, F8, F2 | 6 | 9-10 | 11 | 59 |

- In-order Issue/Commit, Out-of-Order Execution/Writeback

# Hardware-Based Speculation

- Instructions are finished in order according to ROB
- It can be precise exception.
- It is easily extended to integer register and integer function unit.
- But the hardware is too complex.