

Tomasulo Loop Example

Loop:	LD	FO	0	R1
4	MULTD	F4	FO	F2
	SD	F4	0	R1
	SUBI	R1	R1	#8
	BNEZ	R1	Loop	

- ☐ Assume Multiply takes 4 clocks
- ☐ Assume first load takes 8 clocks (cache miss), second load takes 1 clock (hit)
- ☐ To be clear, will show clocks for SUBI, BNEZ
- Reality: integer instructions ahead



Loop Example

Instruction	on statu	is:				Exec	Write				
ITER	Instruct	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1				Load1	No	1,015	
1	MULTD	F4	F0	F2				Load2	No		
1	SD	F4	0	R1				Load3	No		
2	LD	F0	0	R1			10.0	Store1	No		
2	MULTD	F4	F0	F2				Store2	No		
2	SD	F4	0	R1				Store3	No		
Reservat	ion Stat	tions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No					1111	MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	No						SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result s	tatus									
Clock	R1	-	F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	•••	F30
0	80	Fu							-		



80

Fu

Load1

Instructi	on statu	s:				Exec	Write				
ITER	Instruct	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R 1	1			Load1	Yes	80	
1	MULTD	F4	F0	F2				Load2	No		
1	SD	F4	0	R1				Load3	No		
2	LD	F0	0	R1			11.0	Store1	No		
2	MULTD	F4	F0	F2				Store2	No		
2	SD	F4	0	R1				Store3	No		
Reservat	ion Stat	tions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No					7 11	MULTD	F4	F0	F2
	Add3	No					-	SD	F4	0	R1
	Mult1	No						SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result s	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	<i>F12</i>	•••	<i>F30</i>



Instructi	on statu	s:				Exec	Write				
ITER	Instruct	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	4-1		Load1	Yes	80	1-01
1	MULTD	F4	F0	F2	2		Real Property	Load2	No		
1	SD	F4	0	R1				Load3	No		
2	LD	F0	0	R1				Store1	No		
2	MULTD	F4	F0	F2				Store2	No		
2	SD	F4	0	R1		1/10		Store3	No		
Reservat	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load1		SUBI	R1	R1	#8
	Mult2	No				- 6		BNEZ	R1	Loop	
Register	result s	tatus									
Clock	R1		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	<i>F12</i>	•••	F30
2	80	Fu	Load1		Mult1					OF AUTO	Printer tree and

Instruction status:				Exec	Write				
ITER Instruction	j	k	Issue	Comp	Result		Busy	Addr	Fu
1 LD F	0 0	R1	1			Load1	Yes	80	
1 MULTD F	4 F0	F2	2		9	Load2	No		
1 SD F	4 0	R1	3			Load3	N/o		
2 LD F	0 0	R1				Store 1	Yes	80	Mult 1
2 MULTD F	4 F0	F2			- () ()	Store2	No		
2 SD F	4 0	R1		11/100		S.ore3	No		
Reservation Station	es:		SI	<i>S2</i>	RS				7
Time Name <u>Bu</u>	sy Op	Vj	Vk	Qj	Qk	Code			
Add1 N	0					LD	F0	0	R 1
Add2 N	O					MULTD	F4	F0	F2
Add3 N	0					SD	F4	0	R 1
Mult1 Y	es Multd		R(F2)	Load1		SUBI	R1	R1	#8
Mult2 N	0			H.		BNEZ	R1	Loop	
Register result stati	lS								
Clock R1	F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	•••	F30
3 80 F	u Load1		Mult1						
□Implicit re	nami	ng s		up '	'Dat	aFlov	v" g	raph	拼言



Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	4-10		Load1	Yes	80	
1	MULTD	F4	F0	F2	2		9	Load2	No		
1	SD	F4	0	R1	3			Load3	No		
2	LD	F0	0	R1				Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2				Store2	No		
2	SD	F4	0	R1				Store3	No		
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
	Add1	No				7/10		LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load1		SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result si	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	•••	F30
4	80	Fu	Load1		Mult1						







Instruction sta	tus:				Exec	Write				
ITER Instru	ction	\dot{J}	\boldsymbol{k}	Issue	Comp	Result		Busy	Addr	Fu
1 LD	F0	0	R1	1			Load1	Yes	80	
1 MULT	TD F4	F0	F2	2			Load2	No		
1 SD	F4	0	R 1	3			Load3	No		
2 LD	F0	0	R1				Store 1	Yes	80	Mult1
2 MULT	TD F4	FO	F2			11.	Store2	No		
2 SD	F4	0	R1				Store3	No		
Reservation St	tations:			S1	<i>S2</i>	RS				
Time Name	e Busy	Ор	Vj	Vk	Qj	Qk	Code:			
Add	l No				1/4	15-13	LD	F0	0	R1
Add	2 No						MULTD	F4	F0	F2
Add	3 No						SD	F4	0	R1
Mult	1 Yes	Multd		R(F2)	Load1		SUBI	R1	R1	#8
Mult	2 No						BNEZ	R1	Loop	
Register result	tstatus									
Clock R1		F0	<i>F2</i>	F4	<i>F6</i>	F8	F10	F12		F30
5 72	Fu	Load1		Mult1						





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Loop Example Cycle 6

Instruction	n statu	s:				Exec	Write				
ITER In	nstructi	ion	\dot{J}	k	Issue	Comp	Result		Busy	Addr	Fu
1 L	D	F0	0	R1	1			Load1	Yes	80	
1 N	IULTD	F4	F0	F2	2			Load2	Yes	72	
1 SI	D	F4	0	R 1	3			Load3	No		
2 L	D	F0	0	R 1	6		77	Store1	Yes	80	Mult1
2 N	IULTD	F4	F0	F2			0.71	Store2	No		
2 SI	D	F4	0	R1				Store3	No		
Reservatio	on Stat	ions:			S1	<i>S2</i>	RS				
Time I	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No					0 1	LD	F0	0	R 1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
]	Mult1	Yes	Multd		R(F2)	Load1	,	SUBI	R1	R1	#8
]	Mult2	No						BNEZ	R1	Loop	
Register re	esult st	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	• • •	F30
6	72	Fu	Load2		Mult1						

□Notice that F0 never sees Load from location, 80

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Loop Example Cycle 7

Instruction stati	is:				Exec	Write				
ITER Instruct	ion	\dot{J}	k	Issue	Comp	Result		Busy	Addr	Fu
1 LD	F0	0	R1	1			Load1	Yes	80	
1 MULTD	F4	F0	F2	2			Load2	Yes	72	
1 SD	F4	0	R1	3			Load3	No		
2 LD	F0	0	R1	6			Store 1	Yes	80	Mult1
2 MULTD	F4	F0	F2	7		11.0	Store2	No		
2 SD	F4	0	R1				Store3	No		
Reservation Sta	tions:			S1	<i>S2</i>	RS				
Time Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
Add1	No						LD	F0	0	R1
Add2	No						MULTD	F4	F0	F2
Add3	No						SD	F4	0	R1
Mult1	Yes	Multd		R(F2)	Load1		SUBI	R1	R1	#8
Mult2	Yes	Multd		R(F2)	Load2		BNEZ	R1	Loop	
Register result s	tatus									
Clock R1		F0	<i>F2</i>	<i>F4</i>	F6	F8	F10	F12	•••	F30
7 72	Fu	Load2		Mult2			Pour			

☐ First and Second iteration completely overlapped

Register file completely detached from computation



Instruction	on statu	s:				Exec	Write				
ITER	Instructi	ion	\dot{J}	k	Issue	Comp	Result	-	Busy	Addr	Fu
1	LD	F0	0	R1	1	4-0		Load1	Yes	80	
1	MULTD	F4	F0	F2	2			Load2	Yes	72	
1	SD	F4	0	R1	3			Load3	No		
2	LD	F0	0	R1	6			Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7			Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load1		SUBI	R1	R1	#8
	Mult2	Yes	Multd		R(F2)	Load2		BNEZ	R1	Loop	
Register	result st	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	<i>F12</i>	•••	F30
8	72	Fu	Load2		Mult2				,		in to a

Instructi	on statu	s:				Exec	Write				
ITER	Instruct	ion	\dot{J}	k	Issue	Comp	Result	1	Busy	Addr	Fu
1	LD	F0	0	R1	1	9		Load1	Yes	80	
1	MULTD	F4	F0	F2	2			Load2	Yes	72	
1	SD	F4	0	R1	3			Load3	No		
2	LD	FO	0	R1	6			Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7		11	Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load1		SUBI	R1	R1	#8
	Mult2	Yes	Multd		R(F2)	Load2		BNEZ	R1	Loop	
Register	result si	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	F6	F8	F10	F12	• • •	F30
9	72	Fu	Load2		Mult2						

□Load1 completing: who is waiting? □Note: Dispatching SUBI



Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	\dot{J}	k	Issue	Comp	Result	1	Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2			Load2	Yes	72	
1	SD	F4	0	R1	3			Load3	No		
2	LD	FO	0	R1	6	10		Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7		11	Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
	Add1	No					11	LD	F0	0	R 1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R 1
4	Mult1	Yes	Multd	M[80]	R(F2)		7 11	SUBI	R1	R1	#8
	Mult2	Yes	Multd		R(F2)	Load2		BNEZ	R1	Loop	
Register	result si	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	F6	F8	F10	F12	•••	F30
10	64	Fu	Load2		Mult2						

□Load2 completing: who is waiting? □Note: Dispatching BNEZ





Instructi	ion statu	s:				Exec	Write				
ITER	Instruct	ion	\dot{J}	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2			Load2	No		
1	SD	F4	0	R1	3		4	Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7			Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reserva	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No					11.0	LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
3	Mult1	Yes	Multd	M[80]	R(F2)		200	SUBI	R1	R1	#8
4	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop	
Register	result si	tatus									
Clock	R1		F0	<i>F2</i>	F4	<i>F6</i>	F8	F10	<i>F12</i>	•••	F30
11	64	Fu	Load3		Mult2						

□Next load in sequence





Instruction	on statu	s:				Exec	Write				
ITER	Instructi	ion	\dot{J}	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2			Load2	No		
1	SD	F4	0	R1	3			Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	Mult1
2	MULTD	F4	FO	F2	7		11.0	Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No					111-13	LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No					77.77	SD	F4	0	R 1
2	Mult1	Yes	Multd	M[80]	R(F2)			SUBI	R1	R1	#8
3	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop	
Register	result st	atus									
Clock	R1		F0	<i>F2</i>	F4	<i>F6</i>	F8	F10	F12		F30
12	64	Fu	Load3		Mult2						

□ Why not issue third multiply?





Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2			Load2	No		
1	SD	F4	0	R1	3			Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store 1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7			Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reserva	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
	Add1	No					11	LD	F0	0	R1
	Add2	No					V - // I	MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
1	Mult1	Yes	Multd	M[80]	R(F2)		1	SUBI	R1	R1	#8
2	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop	
Register	result si	atus									
Clock	R1		F0	F2	<i>F4</i>	<i>F6</i>	F8	F10	F12	• • •	F30
13	64	Fu	Load3		Mult2						



Instructi	on statu	s:				Exec	Write				
ITER	Instructi	on	j	k	Issue	Comp	Result	-	Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No	100	
1	MULTD	F4	F0	F2	2	14	-	Load2	No		
1	SD	F4	0	R1	3			Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7			Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reservat	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No					11/1/17	LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No					77.77	SD	F4	0	R 1
0	Mult1	Yes	Multd	M[80]	R(F2)			SUBI	R1	R1	#8
1	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop	
Register	result st	atus									
Clock	R1		F0	<i>F2</i>	F4	<i>F6</i>	F8	F10	F12	•••	F30
14	64	Fu	Load3		Mult2						

□Mult1 completing. Who is waiting?





Instructi	on statu	s:				Exec	Write				
ITER	Instructi	on	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3			Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	[80]*R2
2	MULTD	F4	F0	F2	7	15		Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No					7 7	SD	F4	0	R1
	Mult1	No						SUBI	R1	R1	#8
0	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop	
Register	result st	atus									
Clock	R1		F0	F2	F4	<i>F6</i>	F8	F10	F12	•••	F30
15	64	Fu	Load3		Mult2						

■Mult2 completing. Who is waiting?





Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Compl	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3			Load3	Yes	64	
2	LD	F0	0	R 1	6	10	11	Store1	Yes	80	[80]*R2
2	MULTD	F4	F0	F2	7	15	16	Store2	Yes	72	[72]*R2
2	SD	F4	0	R1	8			Store3	No		
Reservat	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load3		SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result si	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	•••	F30
16	64	Fu	Load3		Mult1				-		12x 11x 12x 11



Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Compl	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No	100	
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3			Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	[80]*R2
2	MULTD	F4	F0	F2	7	15	16	Store2	Yes	72	[72]*R2
2	SD	F4	0	R1	8			Store3	Yes	64	Mult1
Reservat	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load3		SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result st	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	<i>F12</i>	•••	F30
17	64	Fu	Load3		Mult1				5		

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64

18

Fu

Load3

Loop Example Cycle 18

Instructi	on statu	<i>s</i> :				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No	- 38	
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3	18		Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store 1	Yes	80	[80]*R2
2	MULTD	F4	F0	F2	7	15	16	Store2	Yes	72	[72]*R2
2	SD	F4	0	R1	8			Store3	Yes	64	Mult1
Reservat	tion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No					31.77	MULTD	F4	F0	F2
	Add3	No					3 1	SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load3	4	SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result st	atus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	•••	<i>F30</i>

Mult1

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Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3	18	19	Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	No		
2	MULTD	F4	F0	F2	7	15	16	Store2	Yes	72	[72]*R2
2	SD	F4	0	R1	8	19		Store3	Yes	64	Mult1
Reservat	ion Stat	ions:			S1	<i>S2</i>	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No						LD	F0	0	R1
	Add2	No					11	MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load3		SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result st	atus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	<i>F12</i>	•••	F30
19	64	Fu	Load3		Mult1				7		5 ag 2 m

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Instructi	on statu	s:				Exec	Write				
ITER	Instructi	ion	j	k	Issue	Compl	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3	18	19	Load3	Yes	64	
2	LD	F0	0	R1	6	10	11	Store1	No		
2	MULTD	F4	F0	F2	7	15	16	Store2	No		
2	SD	F4	0	R1	8	19	20	Store3	Yes	64	Mult1
Reservat	tion Stat	ions:			S1	S2	RS				
Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	Add1	No				145		LD	F0	0	R1
	Add2	No						MULTD	F4	F0	F2
	Add3	No						SD	F4	0	R1
	Mult1	Yes	Multd		R(F2)	Load3		SUBI	R1	R1	#8
	Mult2	No						BNEZ	R1	Loop	
Register	result st	tatus									
Clock	R1		F0	<i>F2</i>	<i>F4</i>	<i>F6</i>	F8	F10	F12	•••	F30
20	64	Fu	Load3		Mult1				-		



Summary of Tomasulo Algorithm

- Reservations stations: implicit register renaming to larger set of registers + buffering source operands
 - > Prevents registers as bottleneck
 - > Avoids WAR, WAW hazards of Scoreboard
 - > Allows loop unrolling in HW
- □Not limited to basic blocks
 - > (integer units gets ahead, beyond branches)
- □ Lasting Contributions
 - > Dynamic scheduling
 - > Register renaming
 - > Load/store disambiguation
- □360/91 descendants are Pentium III; PowerPC 604; MIPS R10000; HP-PA 8000; Alpha 21264

