1. 选择题

(1) What is the RISC-V assembly code for the binary:

0000 1110 1001 0101 0010 1000 0010 0011

A、sw x10, 240(x9)

B、sw x9, 240(x10)

C、sd x10, 240(x9)

D、sd x9, 240(x10)

(2) In order to put the content of address A(32 bits) to register x11, which one following is correct?

(A) lui x10, A\_upper (B) lui x10, A\_upper

ori x10,x10, A\_lower lw x11, A\_lower(x10)

lw x11, 0(x10)

(C) lui x10, A\_upper (D) lui x10, A\_upper

ori x10,x10, A\_lower or x11, A\_lower(x10)

lw x11, 0(x10)

where A\_upper, A\_lower are the high 20 bits and low 12 bits respectively.

(3) For the addition of 0.12345\*10-2和0.12345\*10+2, the first operation is aligning the exponents. After this operation, the aligned exponent is: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_。

A、both -2 B、both +2

C、one is -2,the other is +2 D、both 0

(4) Which statement is correct?

(A) In virtual memory, the number of entries of a page table is equals to the physical page number.

(B) Increasing associativity can reduce Capacity miss.

(C) asynchronous bus: A bus that uses a handshaking protocol for coordinating usage rather than a clock; can accommodate a wide variety of devices of differing speeds.

(D) 内存结构中耗时最多的是最上层

(5) What is the right presentation of the result of 

A：1011 1111 0100 0000 0000 0000 0000 0000

B：1111 1111 1100 1000 0000 0000 0000 0000

C：1011 0001 0100 1000 0000 0000 0000 0000

D：1010 0001 0100 1000 0000 0000 0000 0000

(6) Single-cycle RISC-V datapath cannot complete which of the following operations in one clock cycle.

A、Reading data from and writing data to data memory

B、ALU computation and writing data to the register file

C、Updating PC and writing data to data memory

D、Reading data from register file, ALU computation and writing data to data memory

(7) (\_\_\_\_) can be reduced by increasing the block size.

A：Compulsory misses

B：Capacity misses

C：Conflict misses

D：All three misses

(8) For a virtual memory with TLB, which of following will be run first during memory access? (\_\_\_\_)

A：test cache hit B：test TLB hit

C：test physical memory hit D：test dirty bit

(9) In RAID, REDUNDANT means that more disks are used for \_\_\_\_\_\_\_\_\_\_\_\_\_.

A. enlarging capacity of disk system

B. improving transfer rate of system

C. finding and correcting the read/write error

D. improving reliability of disk system

(10) Given a direct-mapped cache with 16 blocks and each block has 4 words. What block number does byte address 840 map to?

A：2 B：3 C：4 D：5

(11) Cache’s write-through polity means write operation to main memory \_\_\_\_\_\_\_.

A. as well as to cache B. only when the cache is replaced

C. when the difference between cache and main memory is found

D. only when direct mapping is used

大题：

1.

(1) 把这6个数排序：在原码、补码、符号表示、IEEE754 下的 0xF0000000，在原码、补码下的 0xFFFFFFFF

Or 给出不同格式的数排序：单精度浮点、符号-大小、2补码、1补码、还有一个2的N-1次方 bias notation

(2) 不用别的寄存器，交换 x10 和 x11

(3) 书上IndexOutOfBound 那个例子，判断数组越界



2.

C程序写汇编：

卷首给出了'1'=49

void main(char \*s,int \*n){

char c,ch;

c = '3';

ch = '5';

\*n = replace(\*s,c,ch);

}

int replace(char \*u,char c,char ch){

int i = 0;

while(u[i]!=0){

if(u[i]==c){

u[i]=ch;

break;

}

i++;

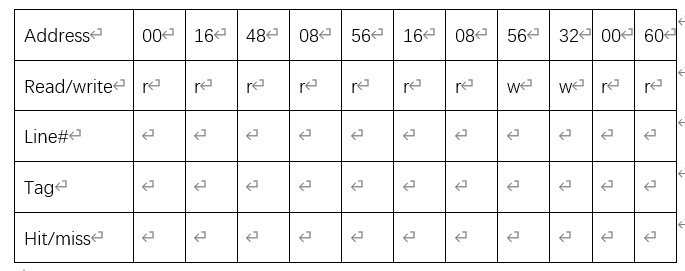
}

return i;

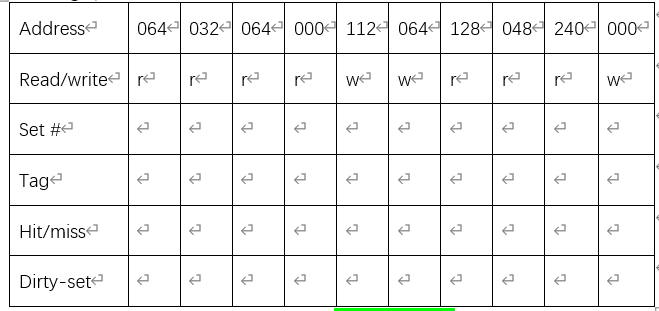
}

3.

(1) Consider a 32 byte direct-mapped write-through & write around cache with 8 byte blocks. Complete the table below for sequence of memory references (occurring from left to right).



(2) Consider a 128byte 2-way set associative write-back with 16 byte blocks, assuming LRU replacement. Complete the table below for a sequence of memory references (occurring from left to right)



Please write down the dirty block number：

4.

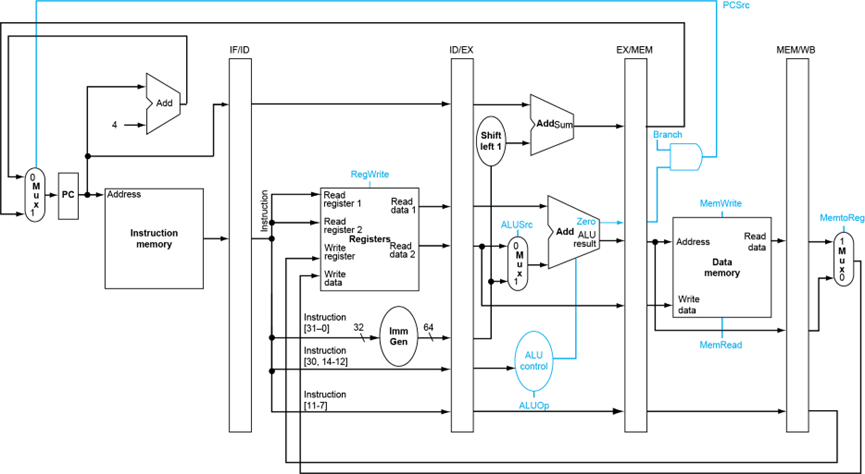
Consider a virtual memory system with the following properties:

40-bit virtual byte address, 16KB pages, 36-bit physical byte address

(1). What is the total size of the page table for each process on this processor, assuming that the valid, protection, dirty, and use bits take a total of 4 bits and that all the virtual pages are in use? ( assuming that disk addresses are not stored in the page table).

(2). Assume that the virtual memory system has implemented a TLB with a total of 64 TLB entries. Could the TLB hold a program if the program accessed at least 8 MB of memory at a time? If you want the TLB to hold the program, how large the page size should be?

5.



For the above single-cycle datapath, answer the questions:

(1) When execute sub instruction, the control signals PCSrc, ALUSrc, MemWrite, RegWrite, and MemtoReg generated by the controller are respectively (\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_).

Assuming that the following codes are executed on the above five-stage pipelined datapath:

sub x5, x7, x11

ld x13, 8(x5)

ld x7, 4(x2)

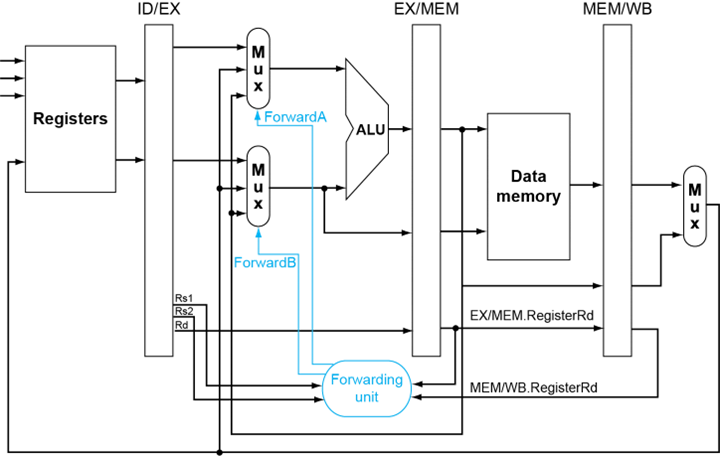
add x13, x5, x13

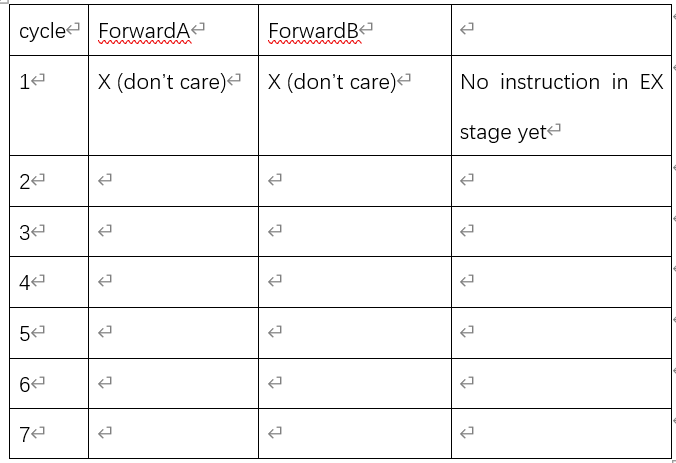
sd x13, 0(x5)

(2) If there is no forwarding or hazard detection, insert NOPs to ensure correct execution.

(3) If the processor has forwarding, but we forgot to implement the hazard detection unit, redo (2)

(4) If there is forwarding (shown in following figure), for the first seven cycles, specify the forwarding signals for each cycle.





答案：

选择：

B A B C A A A B D C A

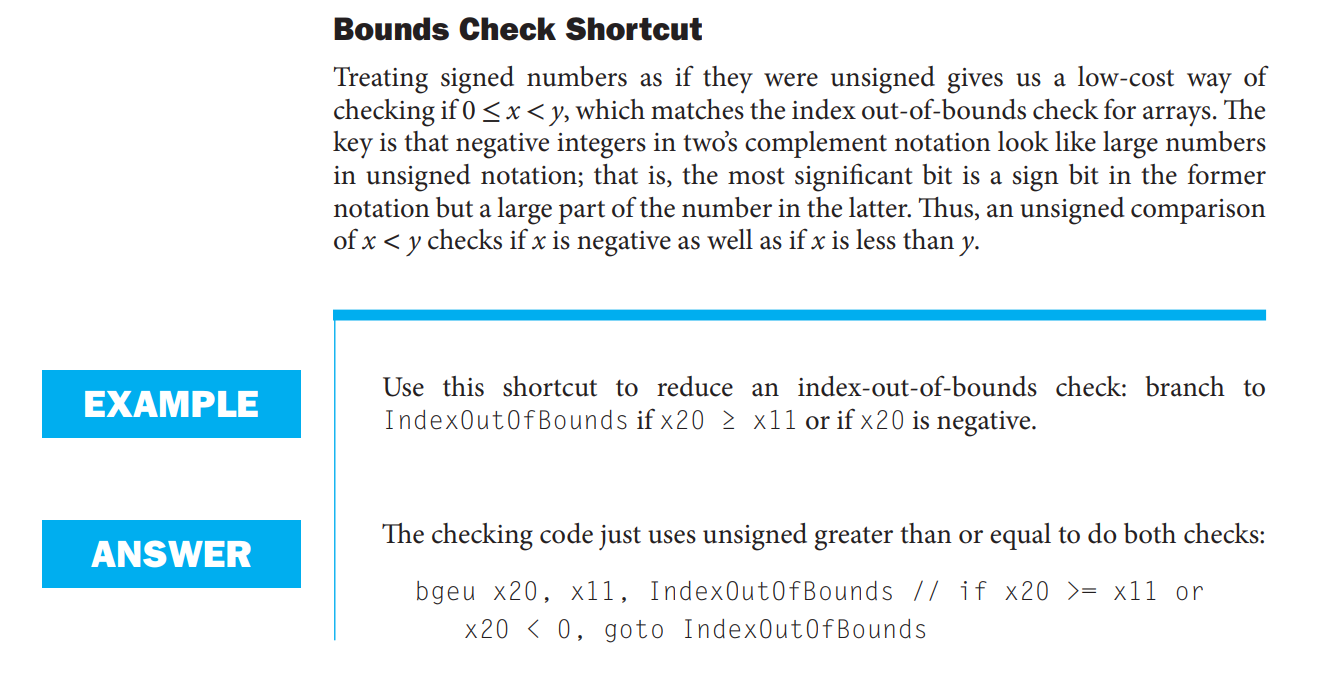
大题：

1.(1) 略

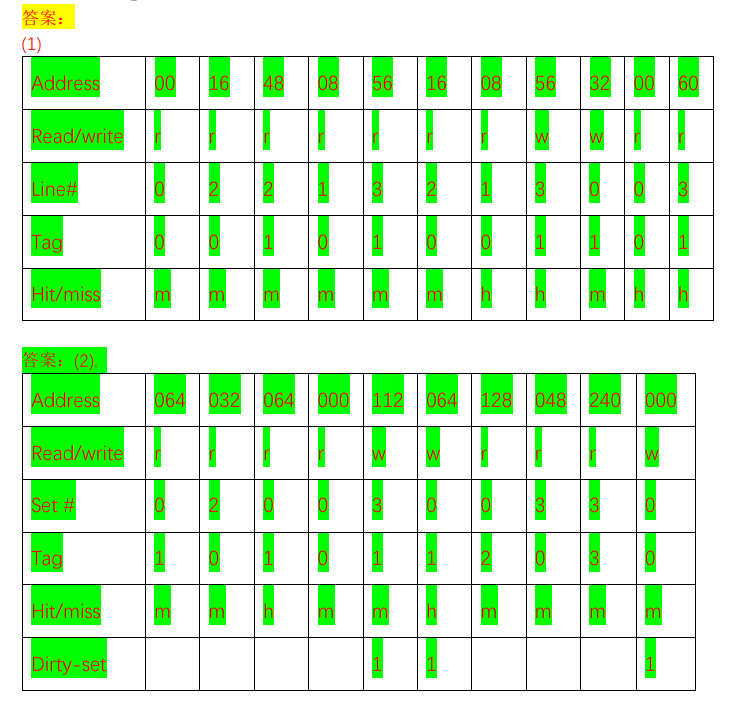
2的N-1次方 bias notation是真实值减去2^(n-1)-1

（2）异或

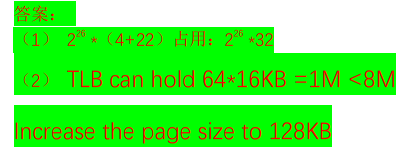
（3）



2.

3. 

4.



5.

