# Chapter1

* 1. Consider two different implementations of the same instruction。。。

**答案：**

* 1. Compilers can have a profound impact on the performance of an。。。

**答案：** 1）1.1、1.25

2）1.37

3）1.67、2.27

# Chapter2

1. Assemble:To convert the RISCV instructions into machine 。。。

**答案：**

|  |  |  |
| --- | --- | --- |
| **Address(Hex)** | **RISCV Assembly Instruction** | **Machine Code(Hex)** |
| 200000 | jal x0, L1 | **0x0700006F** |
| 200004 | Loop: add t3, s3, s4 | **0x01498e33 ‬‬**‬ |
| 200008 | bne t3, t4, Loop | **0xffde1ee3 ‬‬** |
| …… |  | - |
| 200070 | L1： …… | - |

jal x0, L1的解题过程：

**0000 0000 0000 0011 1000-00000-1101111 --🡪**

**0-000 0000 0-0-00 0011 1000-00000-1101111 --🡪**

**0-00 0011 1000-0-000 0000 0-00000-1101111 --🡪**

**0-0000111000-0-00000000-00000-1101111 --🡪**

**0-000 0111 000-0 -0000 0000-0000 0-110 1111 --🡪**

**0700006f**

**0x200000: jal x0, 0x200070**

**0x200004: add t3, s3, s4**

**0x200008: bne t3, t4, 0x200004**

**0x200070: addi x1,x0,1**

**0x200074: addi x2,x1,2**

**0x200078: addi x3,x1,3**

1. To convert the pseudoinstruction(left) into the shortest sequence of 。。。.

**答案：**

|  |  |  |
| --- | --- | --- |
| **Pseudoinstruction** | **Function** | **RISCV instructions** |
| J Lable | goto Lable | **jal x0,Lable;** |
| Seqz rd,rs | Rd = (rs=0)?1:0 | **Sltu rd,x0,rs**  **Xori rd,rd,1** |
| Not rd,rs | rd = ~rs | **xori rd,rs,-1;** |

# Chapter3

* 1. **The data have no inherent meaning, different data format or 。。。.**

**答案：**

|  |  |
| --- | --- |
| 1)a two’s complement integer |  |
| 2)signed and magnitude integer |  |
| 3)A IEEE754 single precision floating-point number | **2-118×(1. 100 0000 0000 0000 0110 1111)2或4.51\*10-36** |
| 4)A RISCV instruction | **Jal x0,76 or jal x0,0x4c** |

* 1. A and B are the floating-point number with IEEE754 single precision。。。。

**答案：**

|  |  |  |
| --- | --- | --- |
| 31 | 30 …… 23 | 22 …… 0 |
| **1** |  | **0 0011 1001 1001 1001 1001 10** |

|  |  |  |
| --- | --- | --- |
| 31 | 30 …… 23 | 22 0 |
| **1** |  | **0 1010 0000 0000 0000 0000 00** |

**计算过程中列出前面部分正确也给部分分数，上表黄底色的不一致也算对。**

# Chapter4

* 1. **Examine the difficulty of adding a proposed swap rs1, rs2 。。。**

**答案：**

Ans.Ans. 1) No new functional blocks are needed.

2) The register fi le needs to be modified so that it can write to two registers in the same cycle. Th e ALU would also need to be modified to allow read data 1 or 2 to be passed through to write data

3) The answer depends on the answer given in 2): whichever input was not allowed to pass through the ALU above must now have a data path to write data 2

4) There would need to be a second RegWrite control wire.

5) Many possible solutions.

* 1. **A new instruction is added to 7-instruction single-cycle CPU of RISC-V:**

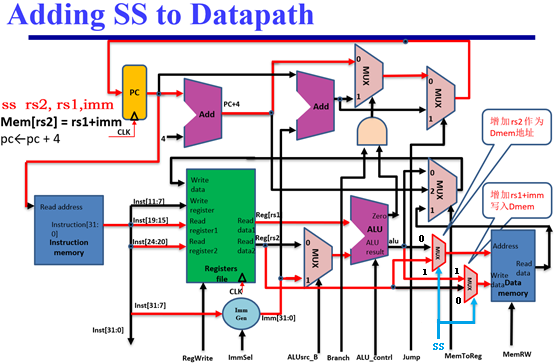
**ss rs2, rs1, imm** (Store Sum)

**答案：**

1) some additional muxes

2) No functional blocks need to be modified, 但RAM的addr和Writedata的来源需要修改。说中这2句任一句都算对。

3) ALU res到RAM的addr之间增加1个mux模块1，寄存器堆的readdata2到RAM的Writedata之间增加1个mux模块2，alures连接到模块1的0口，模块2的1口，readdata2分别连接到模块1的1口，模块2的0口，然后模块1的输出连到RAM的addr，模块2的输出连到RAM的Wtdata，两个模块的控制信号均取自SS（新增）。见下面的图。



4)

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **ALUSrcB** | **Memto-Reg** | **Reg Write** | **Mem Read** | **Mem Write** | **Branch** | **Jump** | **ALUOp1** | **ALUOp0** | **SS-ctr** |
| **SS** | 1 | 0或1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

* 1. **Add NOP instructions to the code below so that it will run correctly 。。。**

**答案：**

* 1. **Consider the fragment of RISC-V assembly below: 。。。。。**

**答案：**