EEC 180 Lab 2

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Objective and Introduction:

The objective of this lab is to synthesize a top-level design including two four-bit adders. This will be achieved by designing lower level modules such as full adders, four-bit adders, and seven-segment display drivers and instantiating the proper amount of modules throughout the hierarchy.

Experiment:

Part II. A Hexadecimal display driver

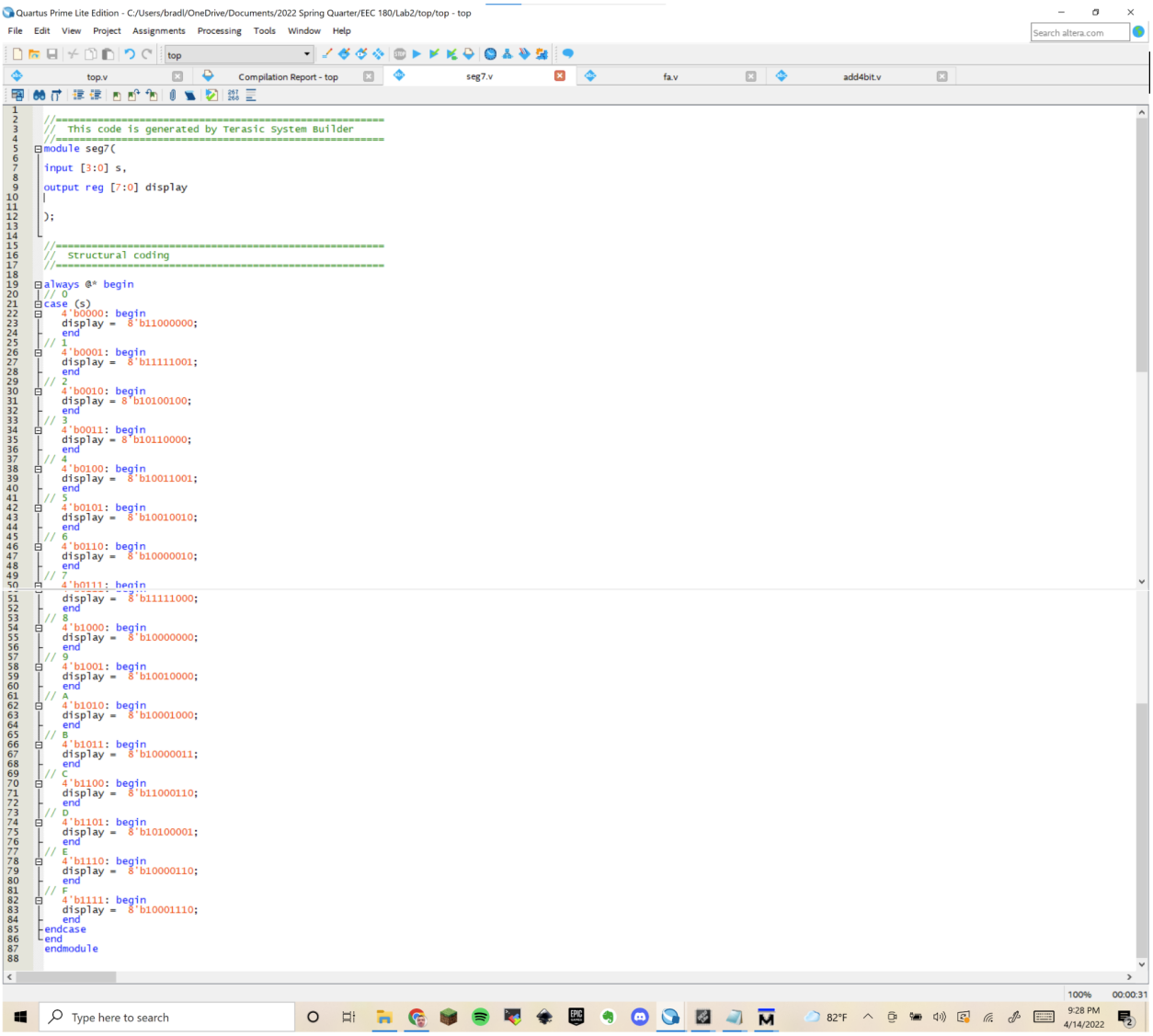

Figure 1: seg7.v

Part III. A Combinational 4-bit Adder

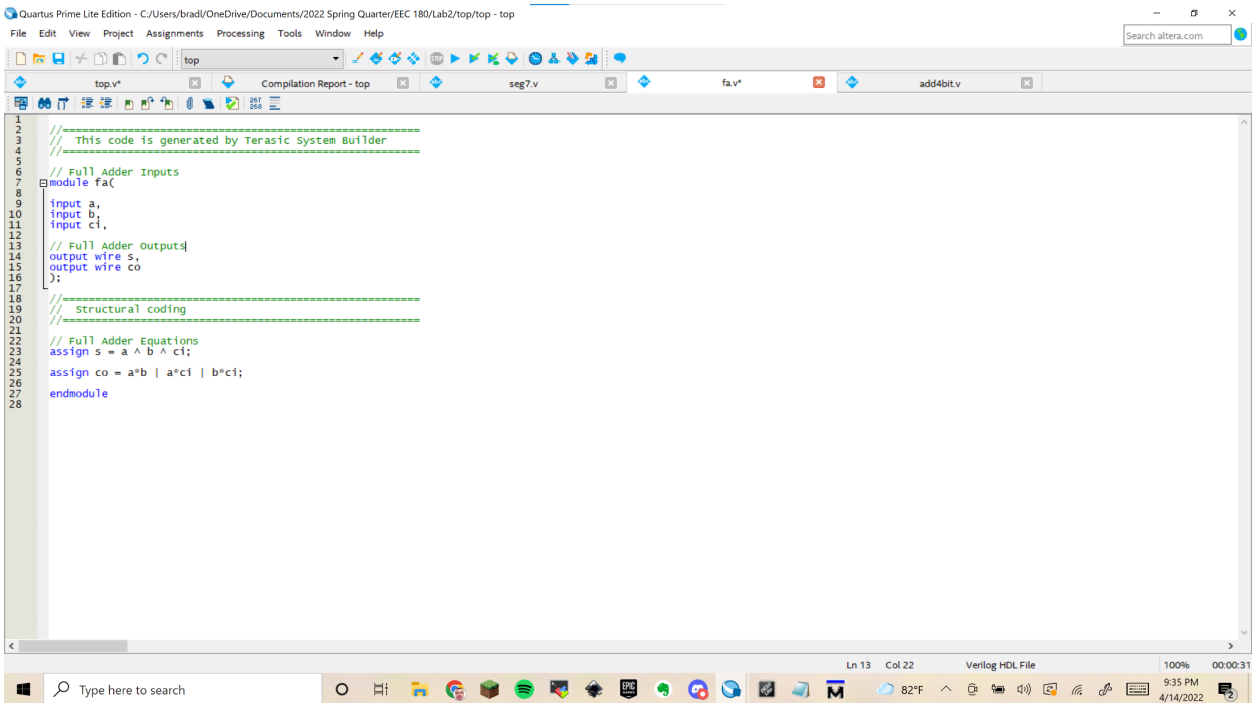

Figure 2: fa.v

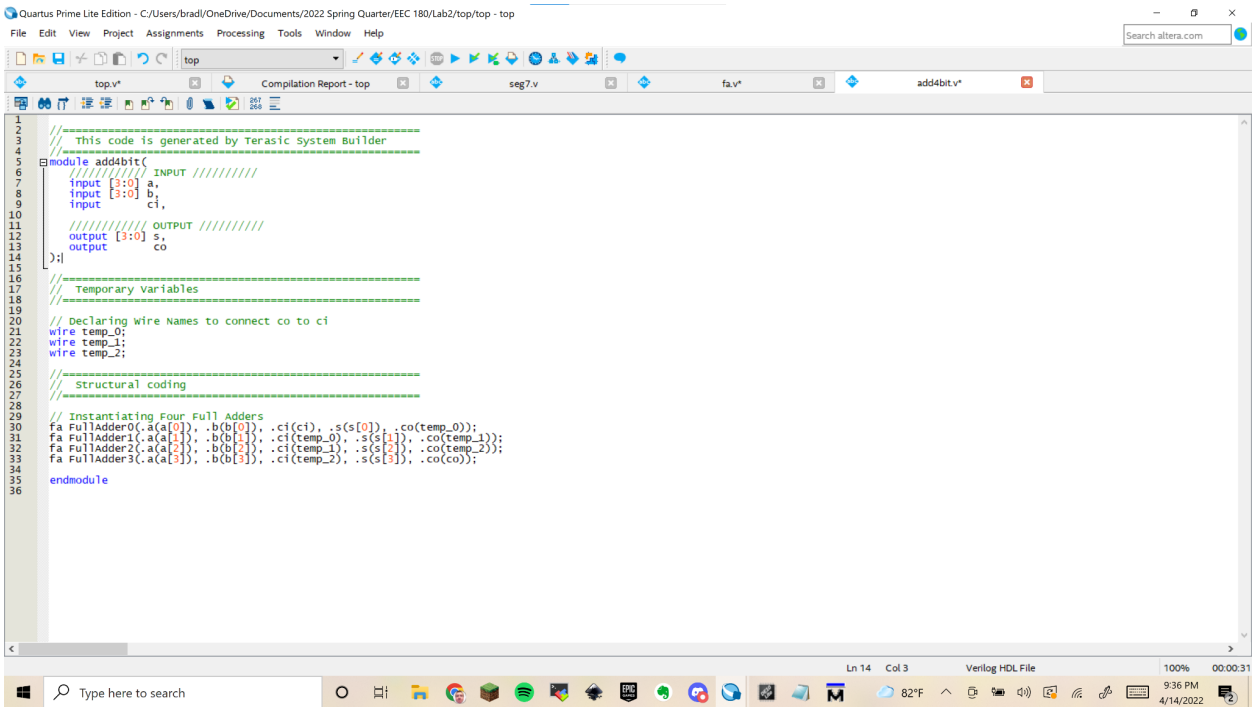

Figure 3: add4bit.v

Part IV. Top-level design

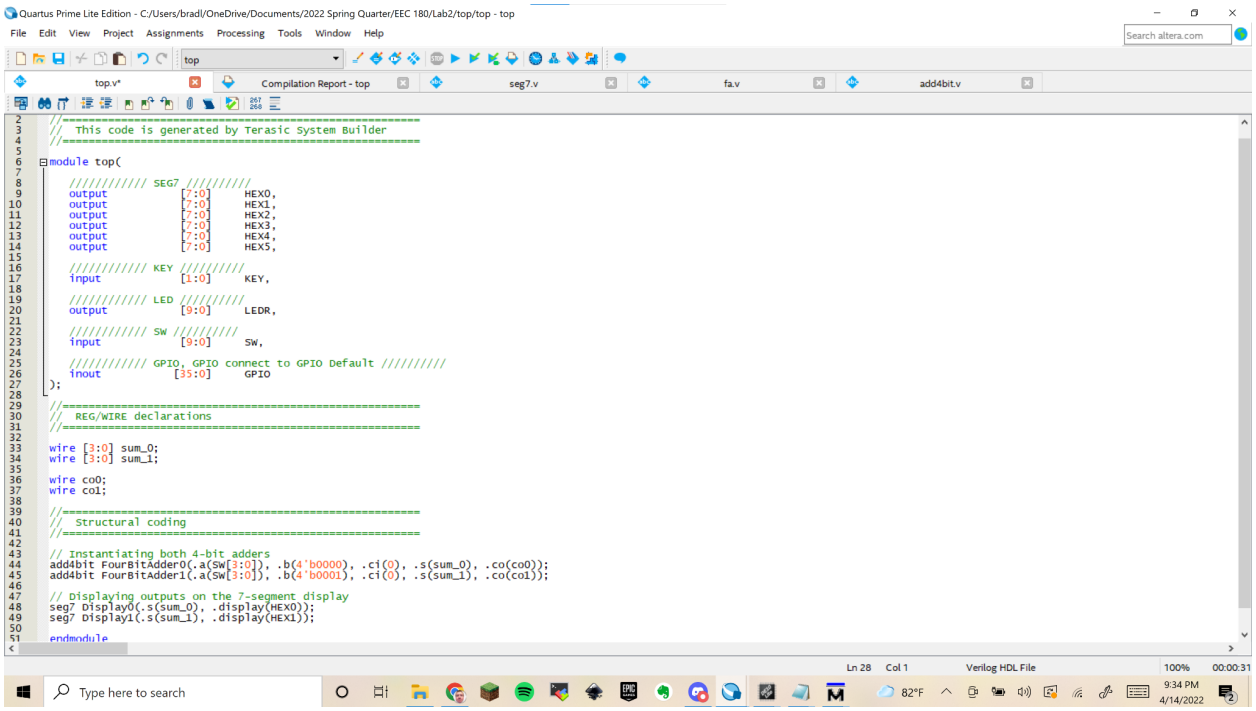

Figure 4: top.v

Part V. Implementation and Verification on the DE10 - Lite

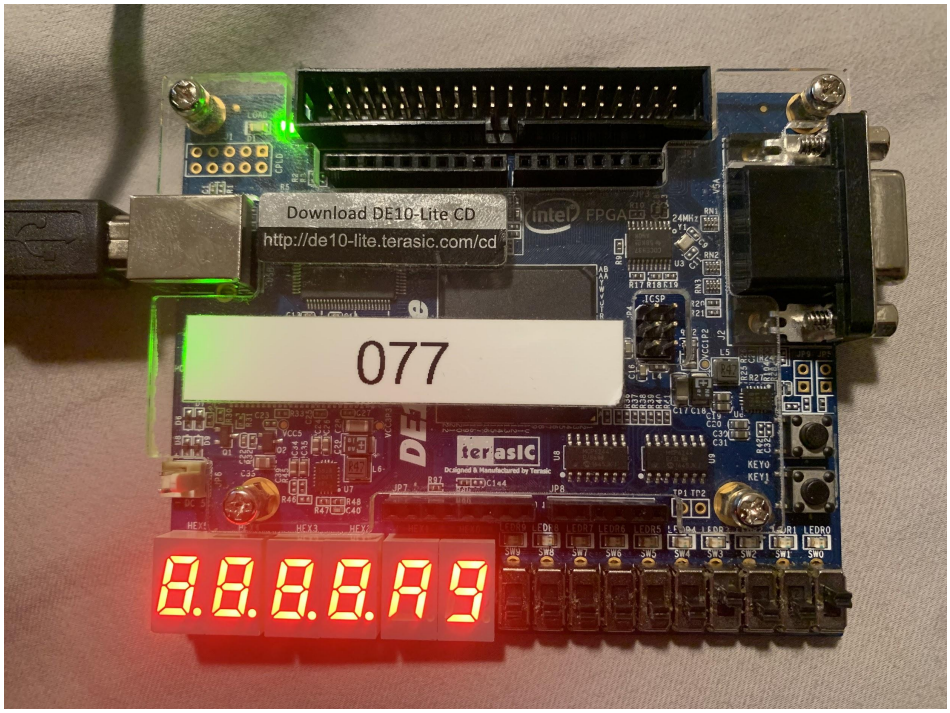

Figure 5: Implementation on DE-10 Lite Board

Part VI. Submitted Work

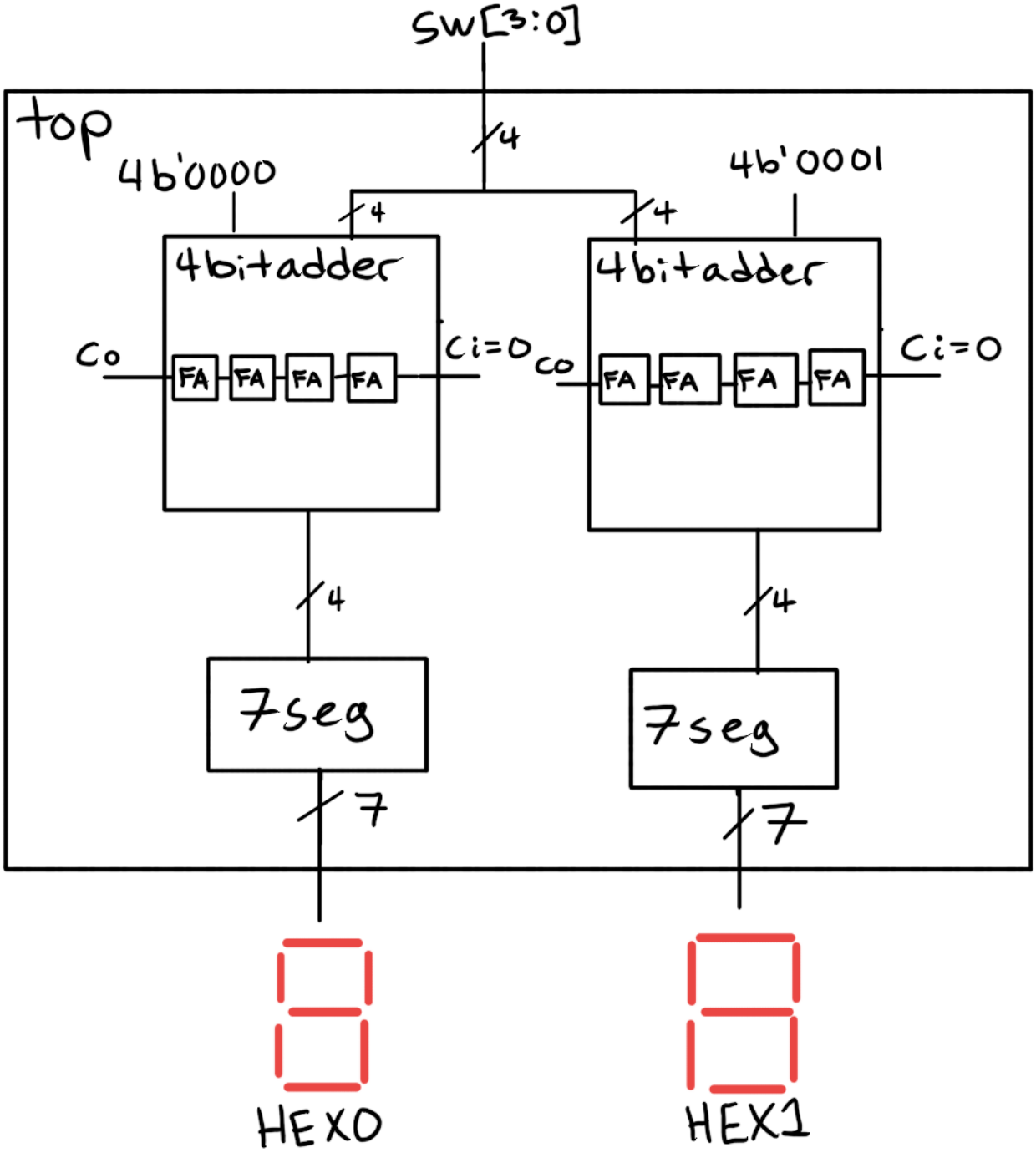

Figure 6: Circuit Diagram

Conclusion: After completing this lab I feel I have gained a greater understanding of how top level designs are created within quartus and programmed in Verilog. I hope to put this knowledge of instantiating and defining modules to use in future labs.