EEC 180 Lab 4

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Objective and Introduction:

The objective of this lab is to implement a 10 bit shift register using D-Flip-Flop modules as an introduction to implementing Finite State Machines in verilog.

Results:

Part III. Circuit Design

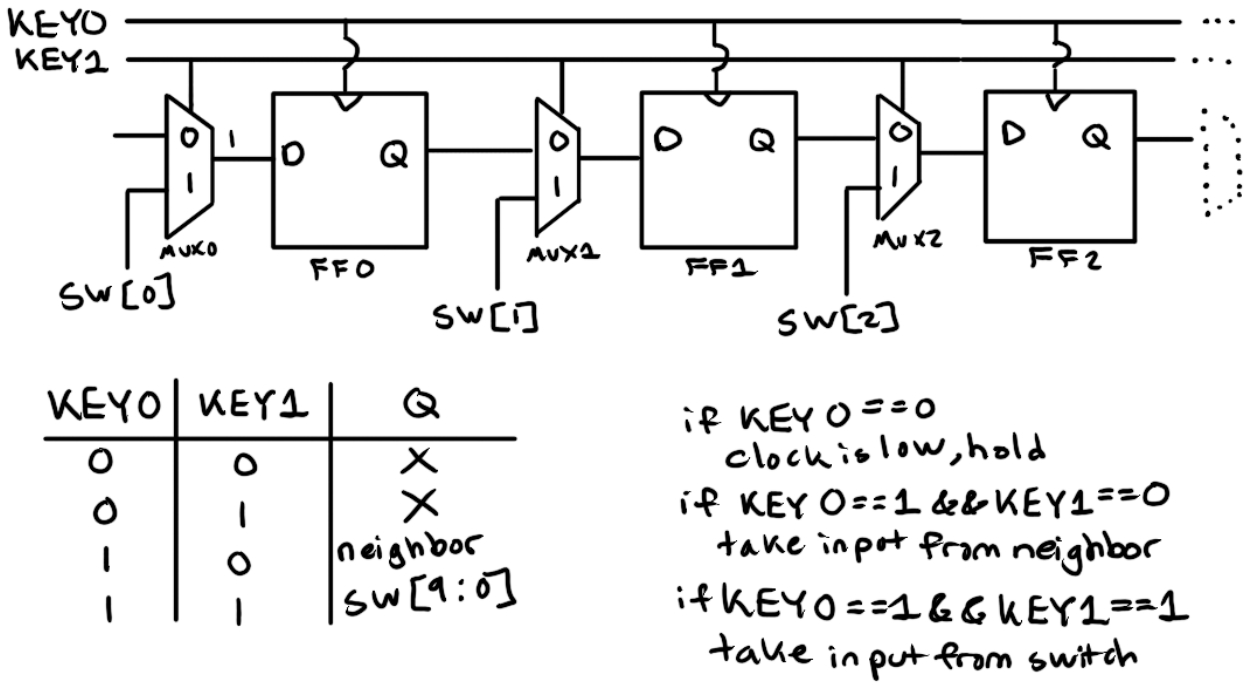

Figure 1: Circuit Design

Part IV. Modelsim Testbench

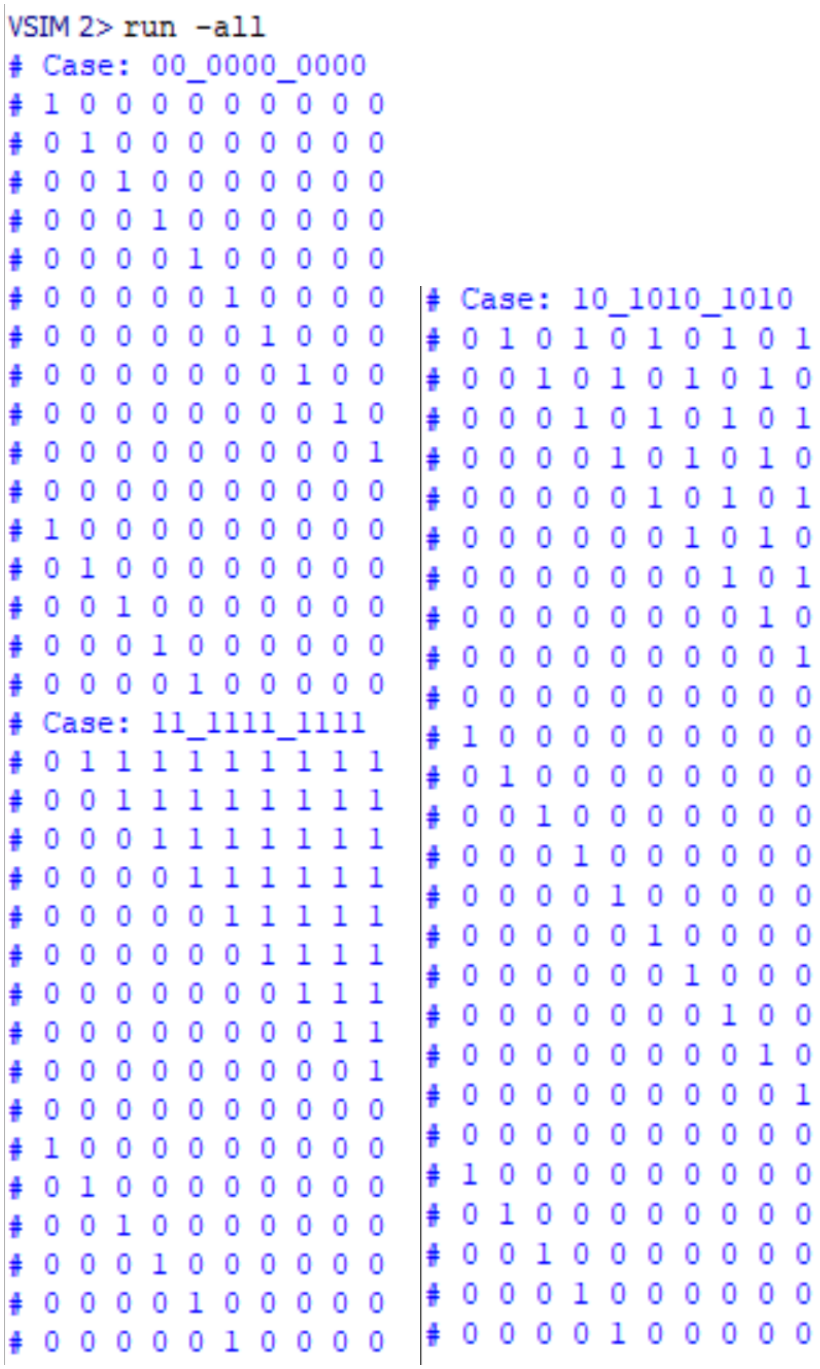

Figure 2: Modelsim Case 1, 2, and 3 Simulations

Conclusion:

After implementing each D-FlipFlop as a register and establishing the next state conditions as described in *Figure 1,* I tested my design on my DE-10 Lite Board and programmed a testbench as well. While I had originally planned on instantiating each flip-flop and MUX as low level modules, it is clear to me that the same circuit can be described as a series of states and non-blocking assignments to determine the next state, and conditional statements instead of multiplexors.