

Bradley Manzo

Santa Cruz, CA 95060

bmanzo@ucsc.edu | Mobile: (951) 314-7983 | <https://brmanzo.github.io>

Education:

University of California, Santa Cruz

September 2024 - Current

- MS in Computer Science and Engineering
- Expected Graduation Spring 2026

GPA: 3.72/4.00

University of California, Davis

September 2019 - December 2023

- BS in Computer Engineering, Minor in Technology Management

GPA: 3.43/4.00

Relevant Coursework: ASIC System Design, Agile Hardware Design, Formal Methods, VLSI, Digital IC

Work Experience:

University of California, Santa Cruz, CA

September 2024 – Current

Teaching Assistant

- Leading students in lab section, hosting office hours, grading and preparing instruction material.
- Instructing subjects including Embedded System Design Lab and Intro to Computer Networks.

Tiami Networks, Elk Grove, CA

January - April 2024

FPGA Engineering Intern

- Implemented 5G NR Stack in hardware for SSB Detection using Intel's DSP Builder in Simulink.
- Designed and pipelined components such as peak detectors, correlational filters, and accumulators.

Hewlett Packard Enterprise, Roseville, CA

June - September 2023

ASIC-SDK Engineering Intern

- Collaborated with HPE Networking Engineers to identify the cause of a faulty wired network link.
 - Developed internal tests using Python and designed an ML model using the TensorFlow library.
 - Designed a deep learning model exhibiting 86% accuracy, while the remaining 14% was within an acceptable margin of error.
-

Projects:

FPGA-based CNN Hardware Acceleration

November 2025 - Current

- Interfacing ESP32-c3 with Arducam via I2C/SPI, image processing with FPGA via UART.
- CDC FIFO for decoupled IO, RLE compressed data transfer, Sobel filtering for edge detection.
- Parameterized modules independently verified using CocoTB before integrating into pipeline.

FPGA-Based Tensor Processing Unit

January - December 2023

- Led a group of four in designing a configurable FPGA-based TPU. Built around a systolic array synthesized in Verilog and communicated with through a custom driver program developed in C.
 - TPU capable of sparse and dense matrix multiplication up to 4096x4096, 4x faster than software.
 - Parameterized data widths and Systolic Array size in Chisel for Agile Hardware Design 2025
-

Leadership Experience:

UC Davis Triathlon Club President

June 2023 – June 2024

- Led a team of 12 officers, oversaw and facilitated all club logistics, meetings and operations.
 - Upheld campus and club policies and maintained an equitable and welcoming environment.
-

Skills:

Digital Design: Hardware acceleration using System Verilog & Chisel, verification using CocoTB.

Programming: C/C++, Python, TensorFlow, Pytesseract, MATLAB, Chisel, Scala, Scripting, UNIX.

General: Effective communicator, written and verbal. Highly collaborative and resourceful leader.