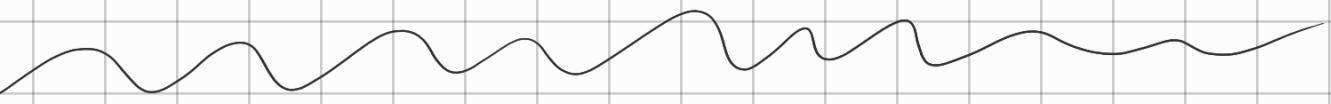
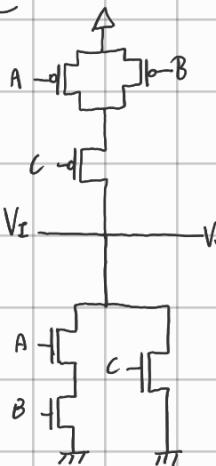


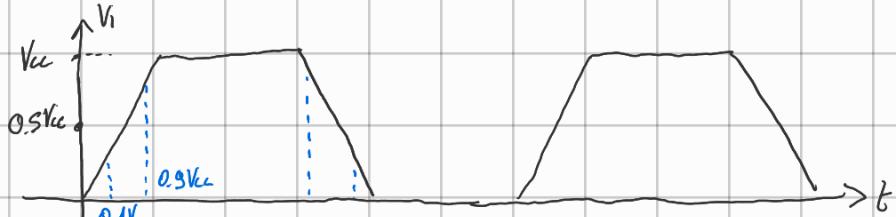
Amd - Or invertor:

$$U = \overline{AB} + C$$



$$V_i \rightarrow V_o$$

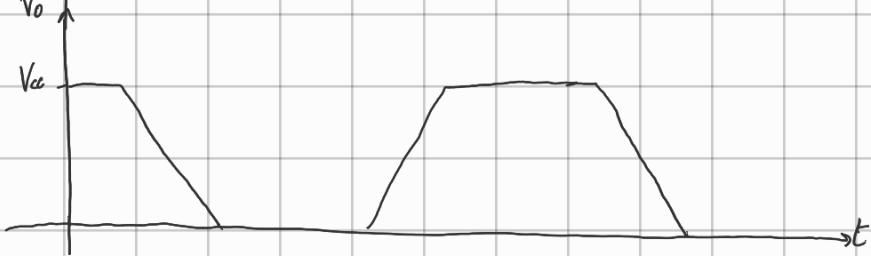
Let's model the input voltage as a trapezoidal waveform and make it periodic.



$t_{rise}$  and  $t_{fall}$  = tempo per passare

dal 10% al 90% dell'escursione

e  $V_i$  inversa.



We can consider  $t_{rise}$  and

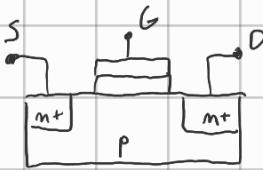
$t_{fall}$  here too.

Per il ritardo di propagazione, si prende la metà dell'escursione di ingresso (immaginando che l'ingresso arriva un fronte verticale all'istante) e si vede quando l'uscita raggiunge il 50% della sua escursione.  $t_{phl}$  o  $t_{phh}$ . Indichiamo come è cambiato l'output.

We define  $t_p = (t_{phh} + t_{phl})/2$

Why does the output take some time to change?

In the RC circuit, there was a dependence from the  $\tau = RC$ . There must be something similar here too. In a very rough approximation, from the  $V_{os}-I_{os}$  relationship of a MOS, we know that we can see the MOS as a resistor. Now we need to find the capacitor. Keep in mind that gates are normally connected together. Let's recall the structure of a NMOS:

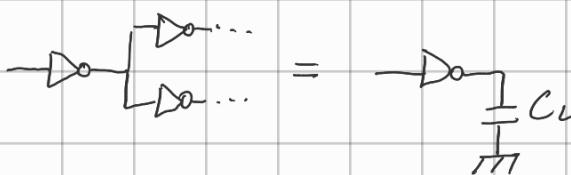


We have conductor, dielectric and semiconductor. It behaves like a capacitor. The input of a CMOS gate behaves like a capacitor.

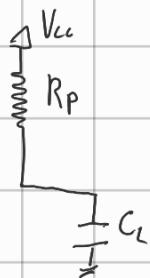
NOTE: Between S,D and gate we have a pn junction, which behaves like a diode that contributes to the capacity seen from the output. So S and D also contribute. A wire also has a series resistance and a parallel capacitor.

We are modeling what is connected to the output of a CMOS gate as a capacitor.

So we can adopt this model:



So if  $V_i = 0$ :



if  $V_i = V_{cc}$

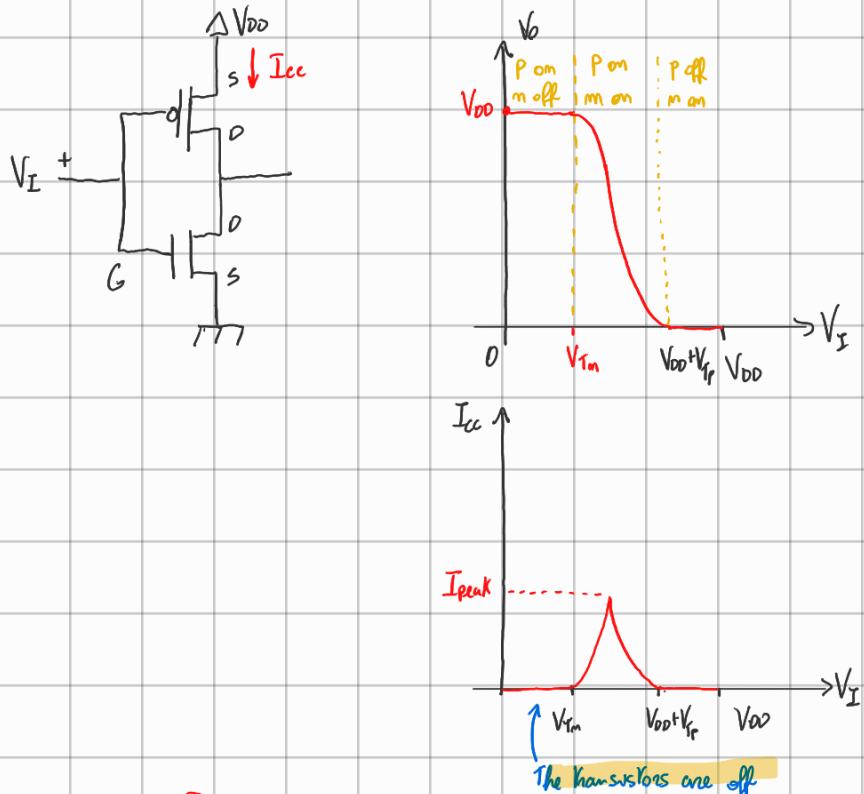


So the  $\tau$  depends on the on resistance of the MOS and on the capacity  $C_L$ . NOTE: making a larger transistor will have a smaller on resistance but bigger capacity,

- C MOS power consumption:  $P = P_{\text{static}} + P_{\text{dynamic}}$ . Two contributions.

$P_{\text{static}}$ : The consumption that's always there, doesn't depend on the activity of the circuit.

- STATIC (we use the inverter because the structure of the gates is always the same)



If transistors are symmetric the  $I_{\text{peak}}$  is around  $\sqrt{V_C}/2$ .

If  $V_I = 0$  or  $V_I = V_{DD}$   $\Rightarrow I_{cc} = 0$  so,  $P_{\text{static}} = 0$ . This is one of the points of dominance of the CMOS (but not 100% true, almost 0, very small). Why? There are leakages, and Sub-threshold current between drain and source. The transistor is never 100% off.

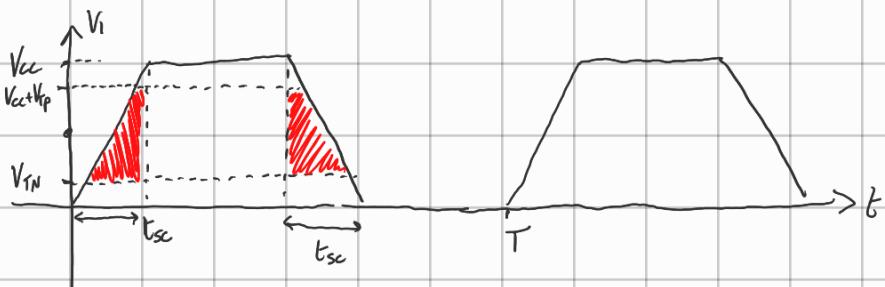
Leakage: the gate is so thin that electrons can move through the gate.

This contribution has worsened over the years, may go up to 20-30% of the total power consumption.

- Dynamic Power: 2 contributions: 1. Short circuit power 2. Switching power.

1. Even if the input changes abruptly, the output takes some time. We are considering the situation in which both transistors are on, so when  $V_I \in [V_{Tm}, V_{DD} + V_F]$ .

So this is due to the simultaneous conduction of the transistors.



Let's consider this:

The red area is the time in which the power is dissipated by the mos.

$$E_{SC} = 2 \int_0^{t_{sc}} V_{CC} \cdot n_{CC}(t) dt$$

(The energy outside it's zero)

$$\text{if } t \in [0, t_{sc}], V_I = \frac{V_{CC}}{t_{sc}} \cdot t$$

$$\frac{dV_I}{dt} = \frac{V_{CC}}{t_{sc}}$$

$$E_{SC} = 2 \cdot V_{CC} \int_0^{V_{CC}} n_{CC}(V_I) \frac{t_{sc}}{V_{CC}} dV_I = 2 t_{sc} \int_0^{V_{CC}} n_{CC}(V_I) dV_I$$

Let's remind that:

$\downarrow$   
integral is this. Area is Power

$$E_{SC} = 2 \cdot t_{sc} \cdot P_0$$

depends on the transistor size and on the technology



Now, if we assume the input is periodic, we can evaluate the average power consumption:

$$P_{SC} = \frac{E_{SC}}{T} = 2 \cdot \frac{t_{sc}}{T} \cdot P_0$$

This equation tells us that the power consum. is proportional

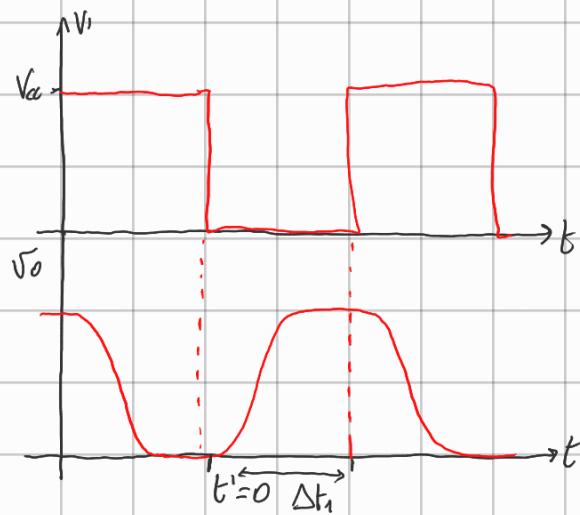
to the falling and rising time of the input. The power depends on the slope of the input.

We have to make the input change as fast as possible. If  $t_{sc} = 0$ ,  $P_{SC} = 0$ . BUT



BUT; We also have a switching power contributing to the consumption. Assume we have this input:





Assume a sharp rise and fall:

$$\frac{1}{C_L} \frac{dV}{dt} \quad [Models what is connected]$$

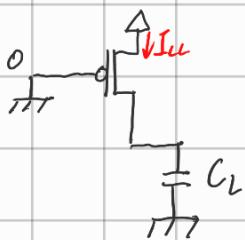
is the output

We waste energy in the charge and discharge of capacitor:

For a capacitor  $Q = C V_c$  and  $E_C = \frac{1}{2} C V_c^2$ . Let's say we start from  $t=0$ .

stored in capacitor

In  $\Delta t_1$  the capacitor is charged:



We assume that the period of the  $V_{cc}$  is large enough so that it reaches a steady value

$$E_{\text{switching}}^{(1)} = \int_0^{+\infty} V_{cc} \cdot I_{cc}(t) dt = V_{cc} \int_0^{+\infty} I_{cc}(t) dt = C_L V_{cc}^2$$

energy consumed to charge the capacitor

is equal to the charge stored in the capacitor, which is total is  $V_{cc} \cdot C \cdot V_{cc}$ .

NOTE: half of the power is stored in the capacitor. The other half is dissipated on the PMOS transistor.

② Now during the discharge we have that the energy stored in the capacitor is dissipated on the NMOS.

So, in a cycle,  $E_{sw} = C_L V_{cc}^2$  which is dissipated on both transistors in the form of heat.

switching frequency.

$$P_{sw} = \frac{E_{sw}}{T} = C_L f V_{cc}^2$$

Though in a real circuit the inputs are not periodic, but there's a dominant signal, which is the clock (synchronous digital circuit). The output of all the gates changes in correspondence of one edge of the clock, which is a periodic signal. Usually a square wave. In general not on every edge, so we consider this with an "a" factor:  
 $\hookrightarrow$  out doesn't change on every edge

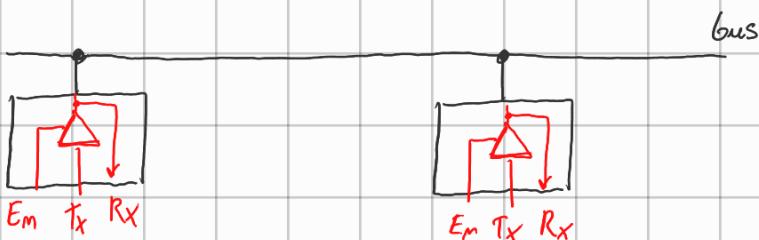
$$P_{sw} = a \cdot C_2 f_{ck} V_{cc}^2, a \in [0,1],$$

as called switching activity.  $f_{ck}$  = clock frequency.

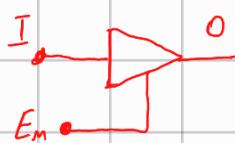
How to reduce? Reduce  $V_{cc}$ , frequency. If a portion of the circuit isn't been used we can switch the clock off (clock gating).

NOTE: Power is related to what the function does. Looking at the power supply we can try to understand what the processor is doing. Different instructions may use different circuits so the switching power can be different.

### • TRI-STATE BUFFER:



We have two blocks that want to communicate.

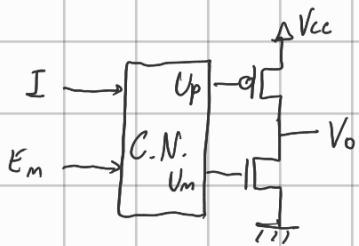


I	Em	O
-	0	Z
0	1	0
1	1	1

→ high impedance: like the buffer didn't exist.

We want to avoid undefined values on the bus, otherwise stuff.

Let's start from the inverter and independently control the two gates; with buffer as disabled both transistors off. We want a combinatory network that receives  $I$  and  $E_m$ , that define the Gate potentials of NMOS and PMOS.



So:

$E_m$	$I$	$U_m$	$U_p$	$Out$
0	0	0	1	z
0	1	0	1	z
<hr/>		the out is $z \uparrow$		
1	0	1	1	0
1	1	0	0	1

