Electronics Systems (938II)

Lecture 3.5

Semiconductor Memories – SRAM

Introduction to Random Access Memory (RAM)

- With the term **RAM** (Random Access Memory), typically we indicate memories that are:
  - **RWM** (Read and Write Memory)
  - **Volatile**

- Note
  - EPROM or EEPROM (or Flash memory) could be seen as a sort of RWM, but…
    - … for those devices, 'writing' (= erasing + reprogramming) is disruptive
    - **In RAMs (or better, RWM) writing is not disruptive**

Introduction to Random Access Memory (RAM)

- RAM classification

  - **Static** RAM (**SRAM**)
    - The memory content is hold over the time, as long as the memory is powered

  - **Dynamic** RAM (**DRAM**)
    - Even if the memory is powered, the memory content needs to be refreshed over the time, otherwise it is lost

Introduction to Random Access Memory (RAM)

- RAM classification

  - **Static** RAM (**SRAM**)
    - The memory content is hold over the time, as long as the memory is powered

  - **Dynamic** RAM (**DRAM**)
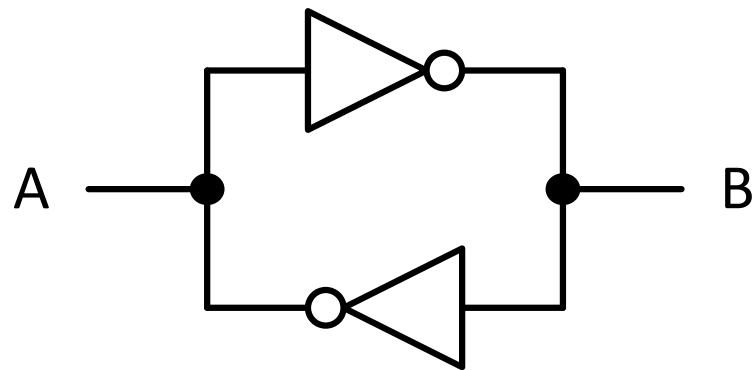   - Even if the memory is powered, the memory content needs to be refreshed over the time, otherwise it is lost

SRAM – Memory cell

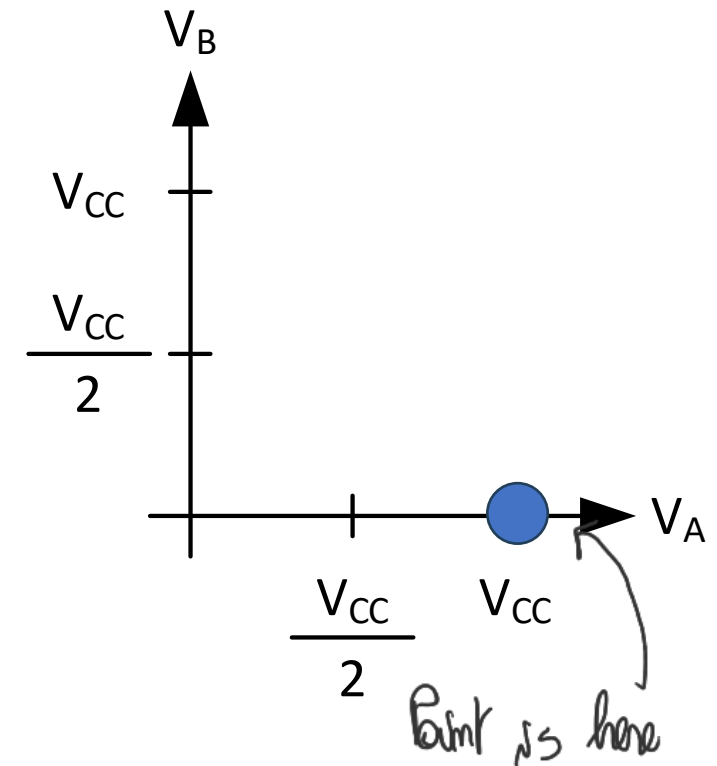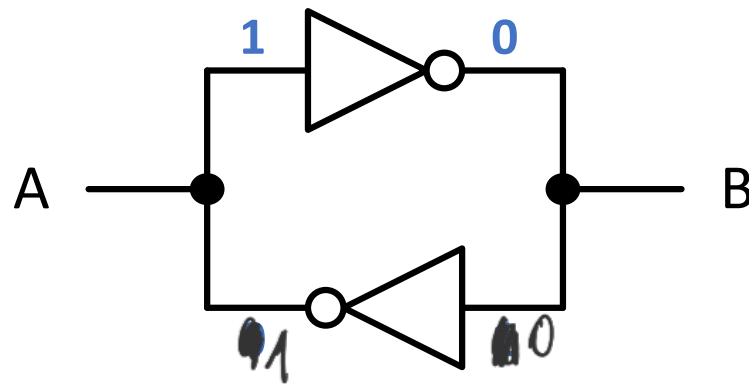- **Bistable** = two closed-loop inverters
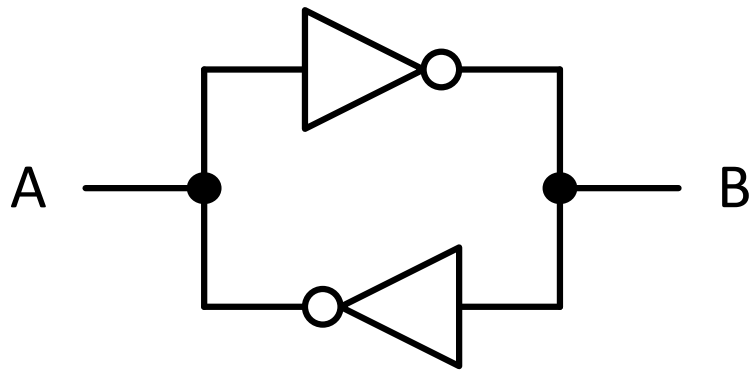
SRAM – Memory cell

- Bistable = two closed-loop inverters
  - Two stable states
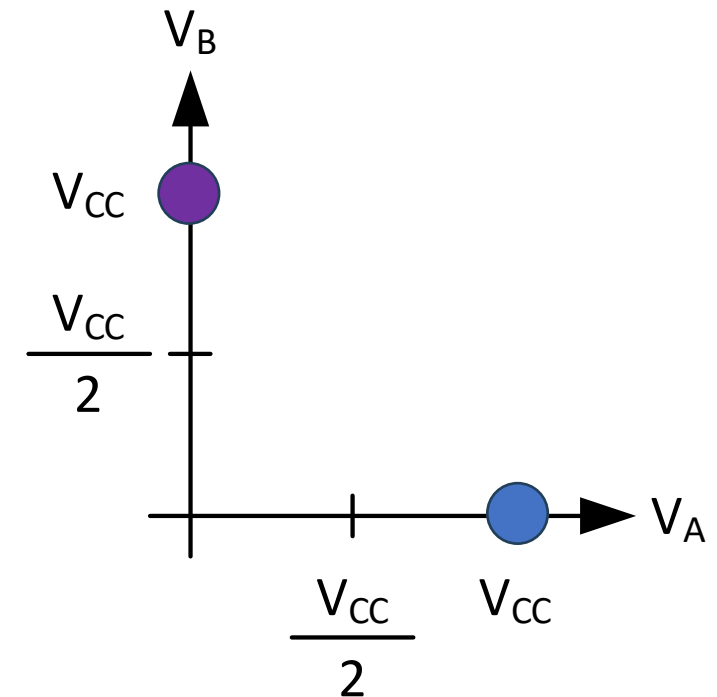 - Stable = the state is not changed (unless external stimuli)

SRAM – Memory cell

- Bistable = two closed-loop inverters
  - Two stable states
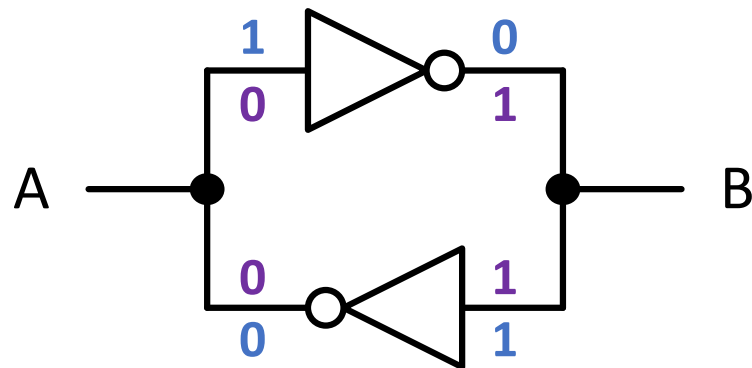 - Stable = the state is not changed (unless external stimuli)
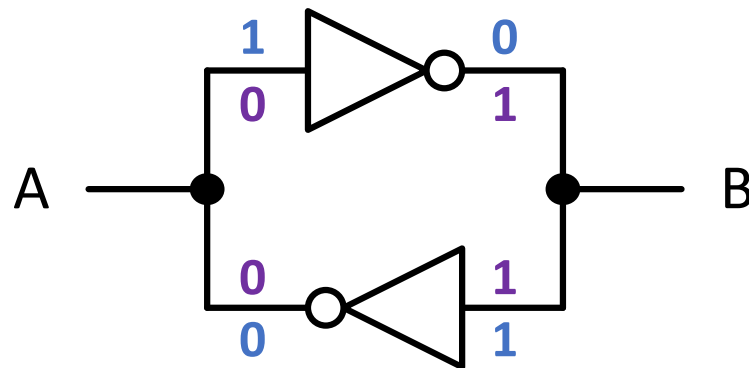   - **State 1**

SRAM – Memory cell

- Bistable = two closed-loop inverters
  - Two stable states
  - Stable = the state is not changed (unless external stimuli)
    - **State 1**
    - **State 2**

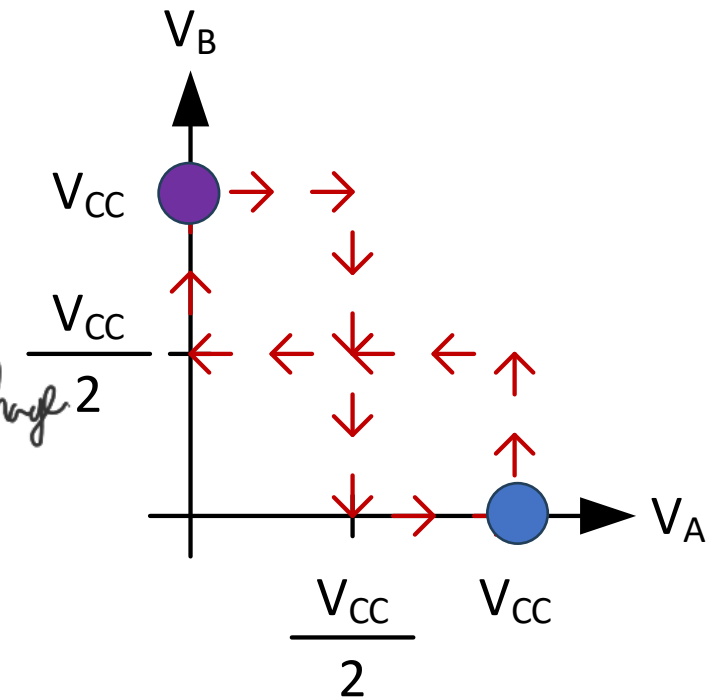Lecture 3.5 - Semiconductor Memories – SRAM
Luca Crocetti

SRAM – Memory cell

- Bistable = two closed-loop inverters
  - Two stable states
  - Stable = the state is not changed (unless external stimuli)
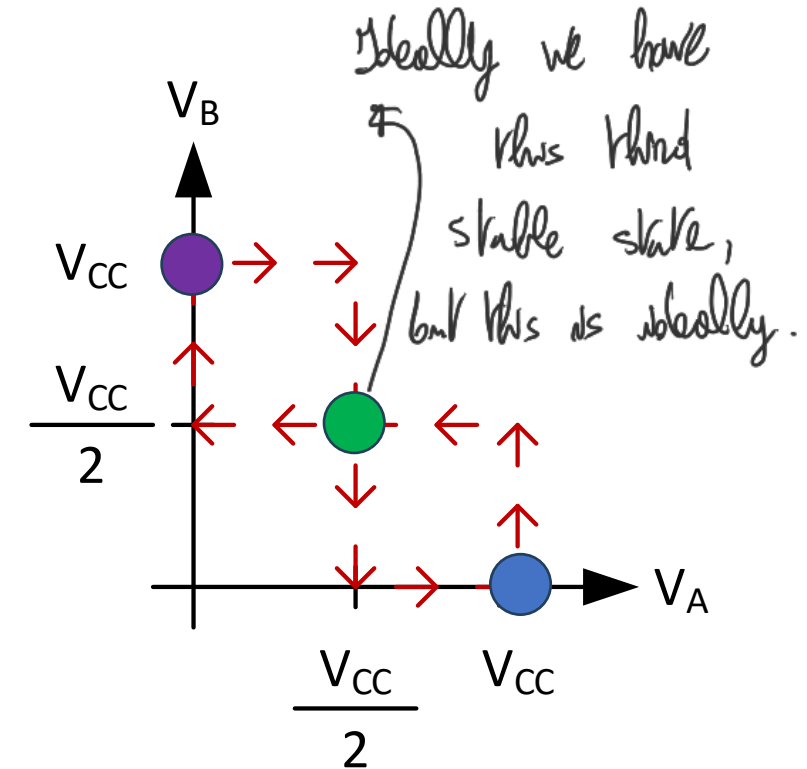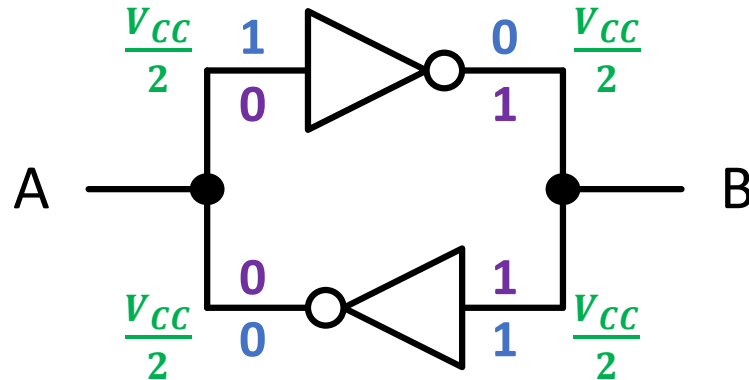   - **State 1**
    - **State 2**

If you apply the external stimuli you have a state change

SRAM – Memory cell

- Bistable = two closed-loop inverters
  - Two stable states
  - Stable = the state is not changed (unless external stimuli)
    - **State 1**
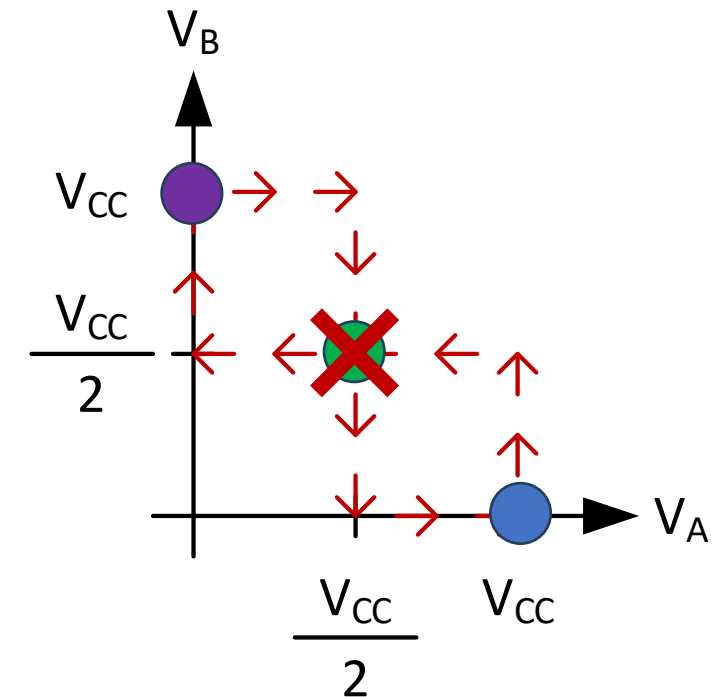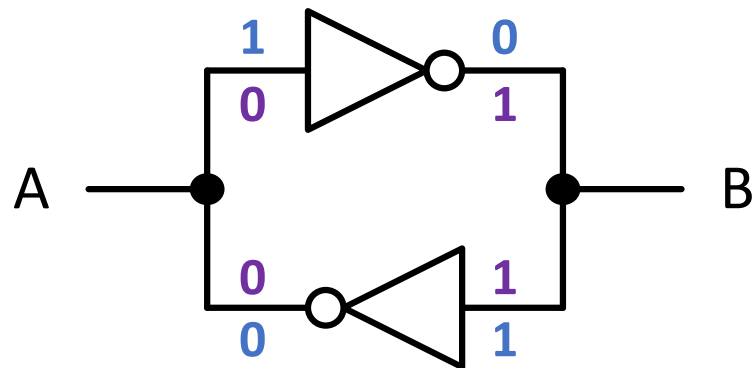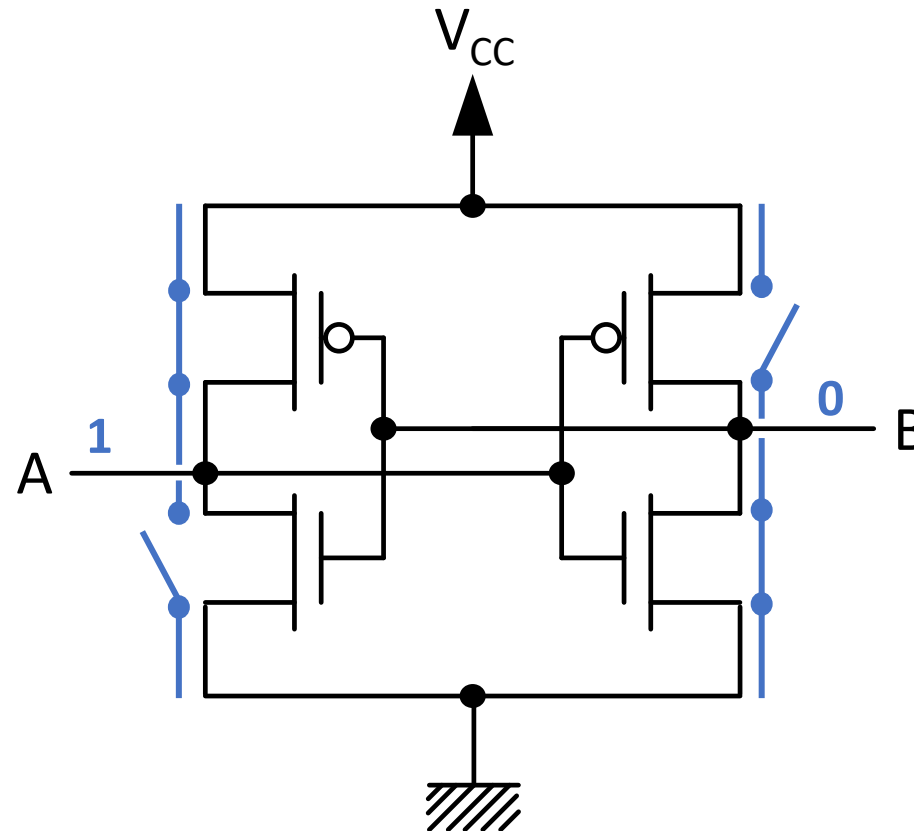   - **State 2**
    - **State 3** ???

SRAM – Memory cell

- Bistable = two closed-loop inverters
  - Two stable states
  - Stable = the state is not changed (unless external stimuli)
    - **State 1**
    - **State 2**
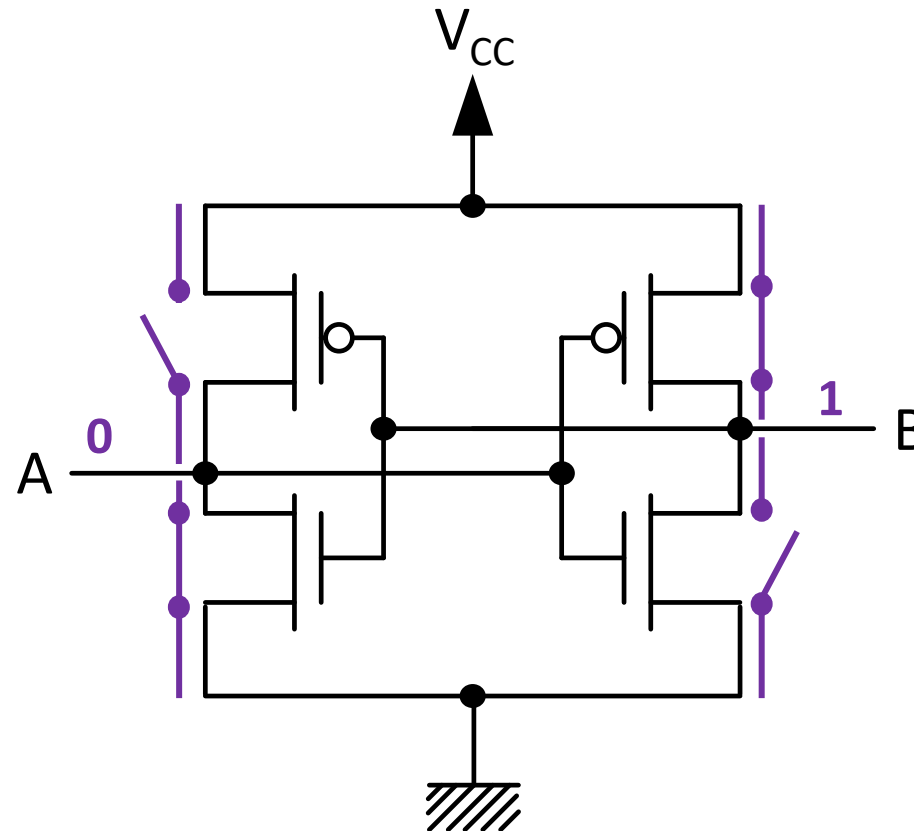   - **State 3** ??? → No! Unstable!!!

Lecture 3.5 - Semiconductor Memories – SRAM
Luca Crocetti

SRAM – Memory cell

- Bistable
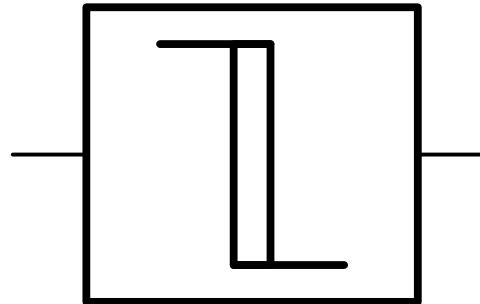 - **CMOS implementation**
    - **State 1**
    - **State 2**

SRAM – Memory cell

- Bistable
  - **CMOS implementation**
    - **State 1**
    - **State 2**

SRAM – Memory cell

- Bistable
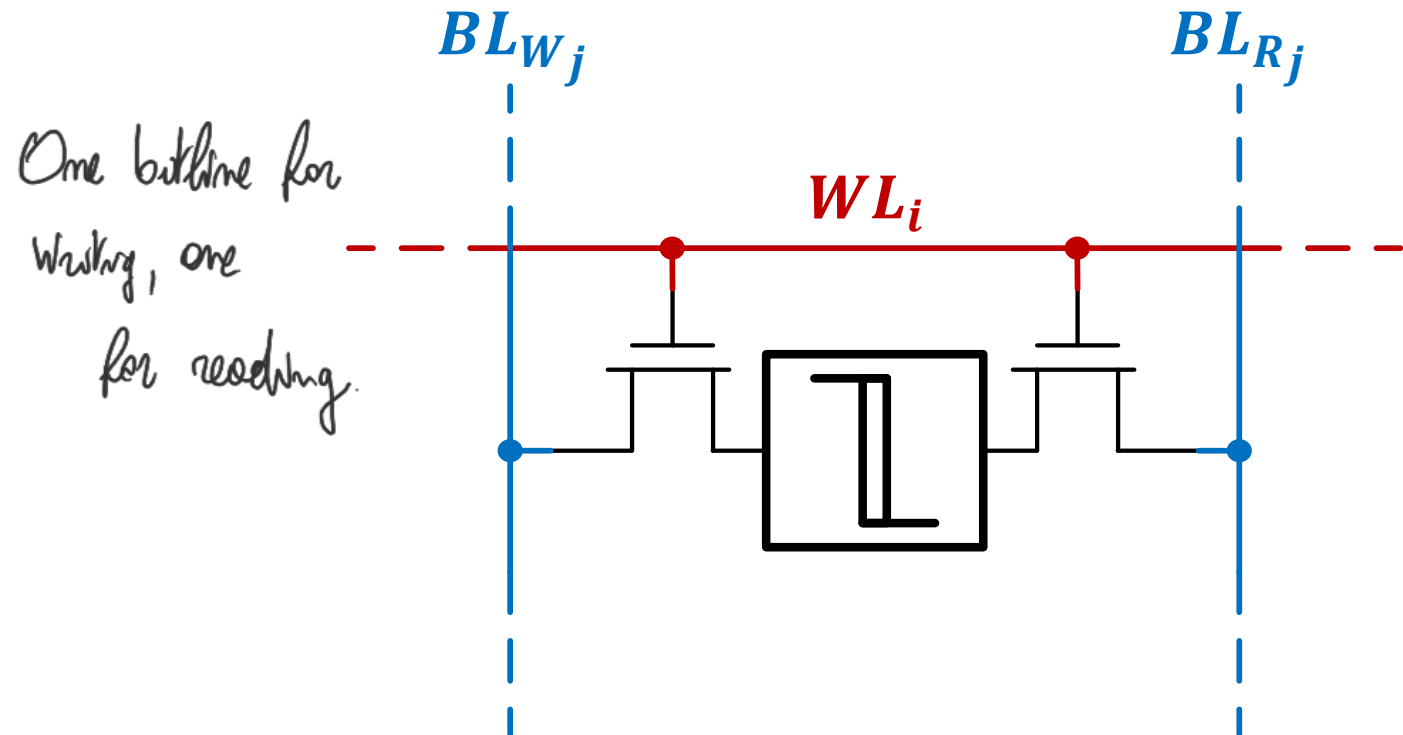 - **Symbol**

Lecture 3.5 - Semiconductor Memories – SRAM
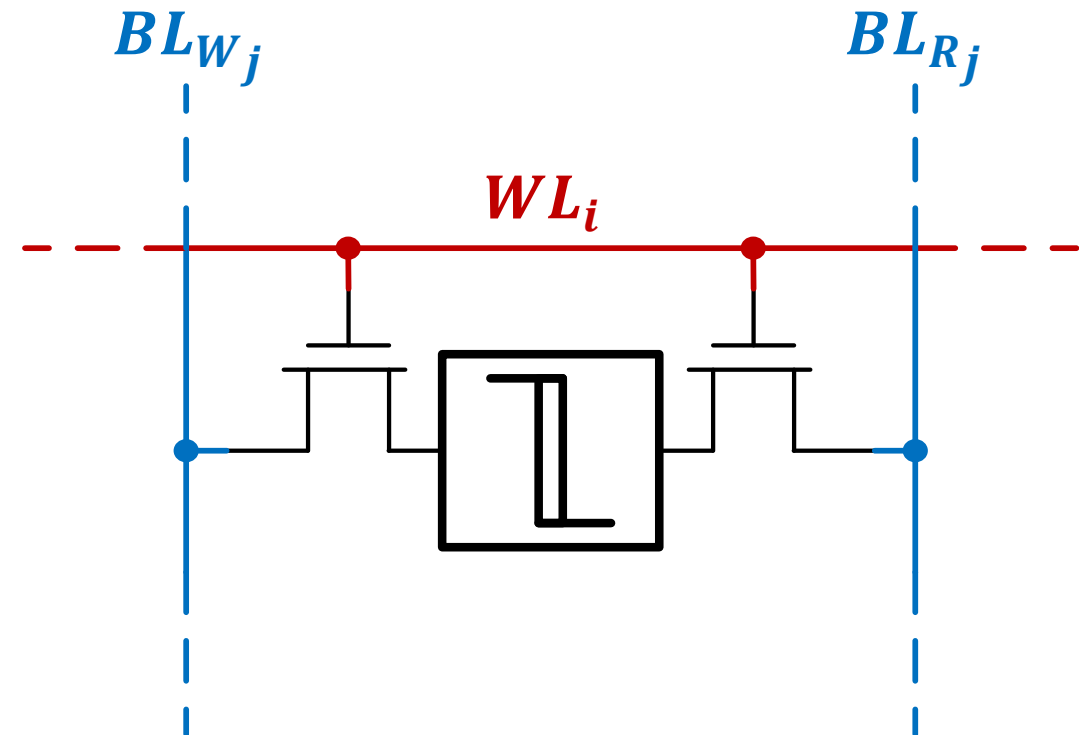Luca Crocetti

SRAM – Memory cell

- Architecture
  - Bistable
  - 2x access transistors

  - WL_i = Word Line
  - BL_{W_j} = Bit Line for Write
  - BL_{R_j} = Bit Line for Read

BL_{W_j} BL_{R_j}

One bitline for writing, one for reading.

WL_i

SRAM – Memory cell

- Architecture
  - Bistable
  - 2x access transistors

  - Also called **6T** (6-Transistors) **SRAM cell**
    - Other architecture exist
    - Example: 4-transistors (4T)

SRAM – Memory cell
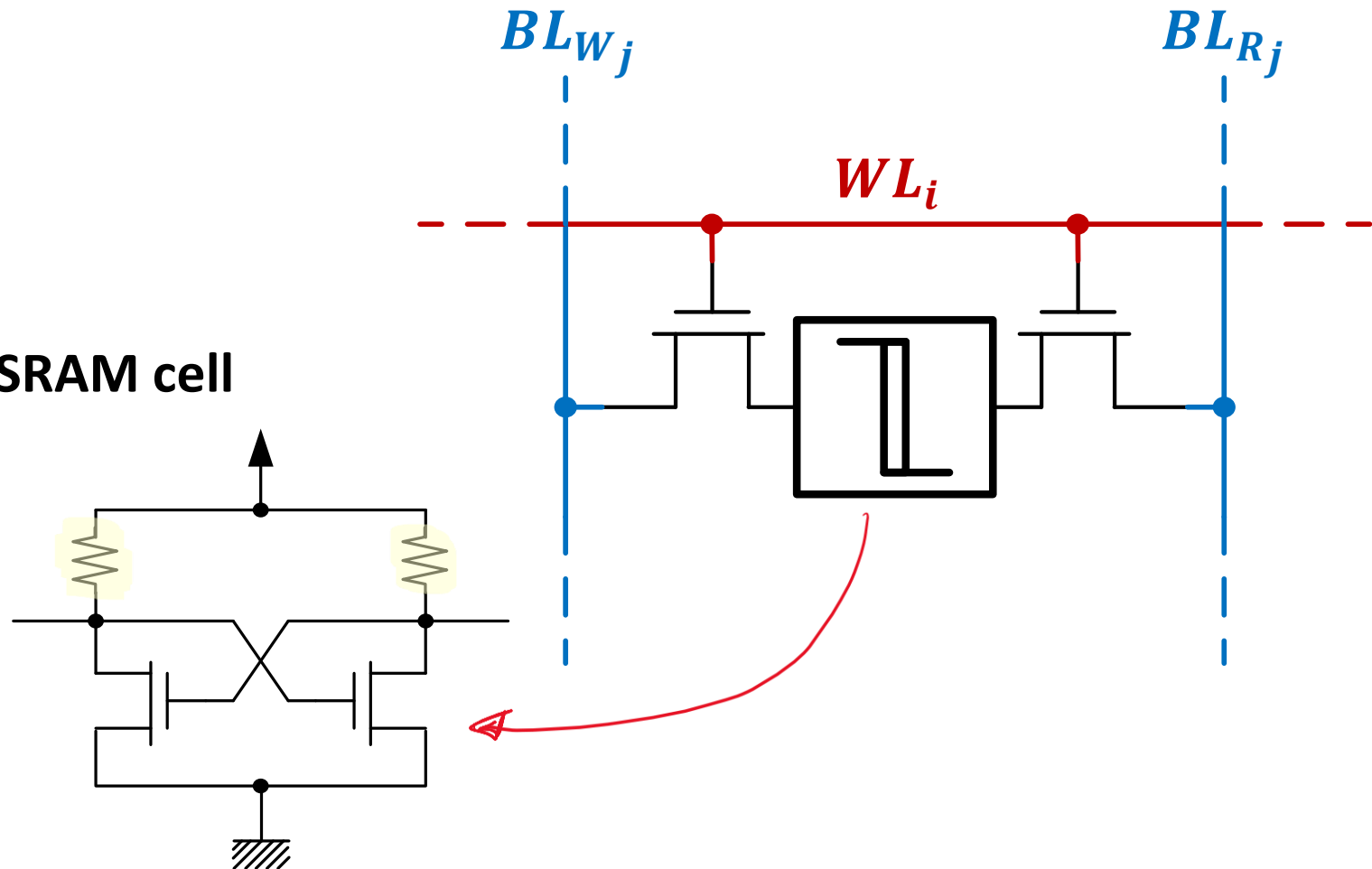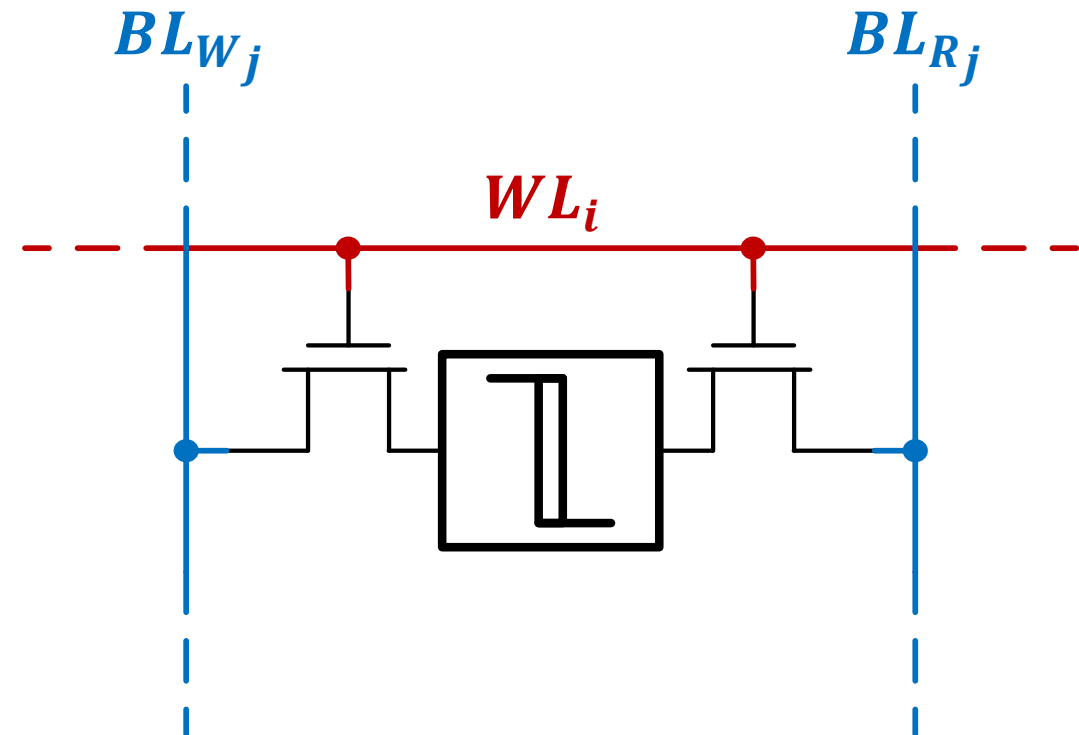
- ## Architecture
  - Bistable
  - 2x access transistors

  - Also called **6T** (6-Transistors) **SRAM cell**
    - Other architecture exist
    - Example: 4-transistors (4T)
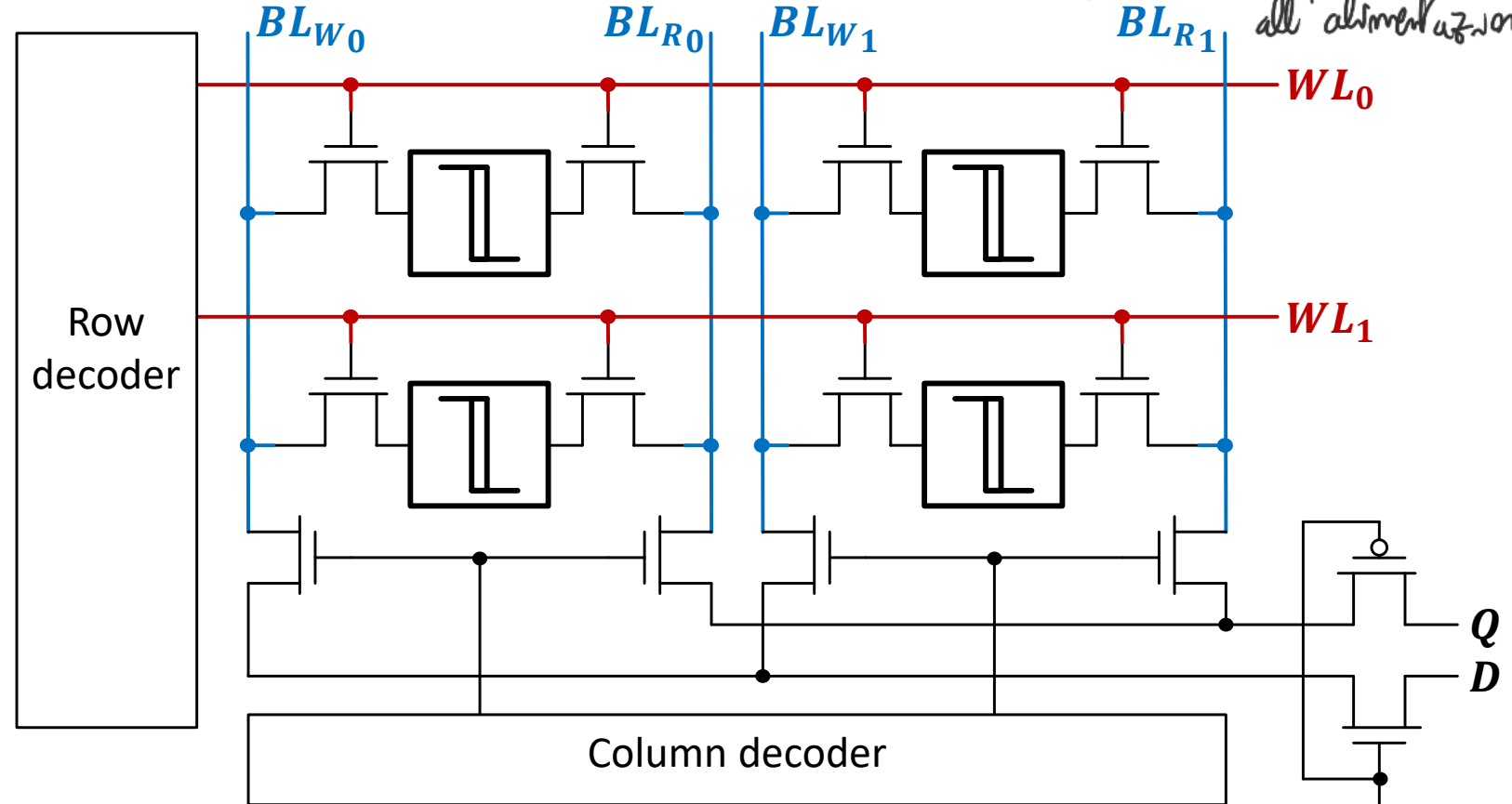   - Resistors instead of pull-up p-MOS in the bistable

BL_{W_j} BL_{R_j}

WL_i

SRAM – Memory cell

- ## Architecture
  - ### Bistable
  - ### 2x access transistors

  - ### Also called **6T** (6-Transistors) **SRAM cell**
    - However, 6T is the most diffused
      - Performance vs. costs

    - If you are interested in other SRAM cell circuits:
      - https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10134887

BL_{W_j} BL_{R_j} WL_i

SRAM – Architecture and working principle

(handwritten: quw le BL mon Sono connesse all' alimentazione)

- Example – 4x4
  - **D** = input (write) data
  - **Q** = output (read) data
  - **W** = write command
    - 1 = write
    - 0 = read

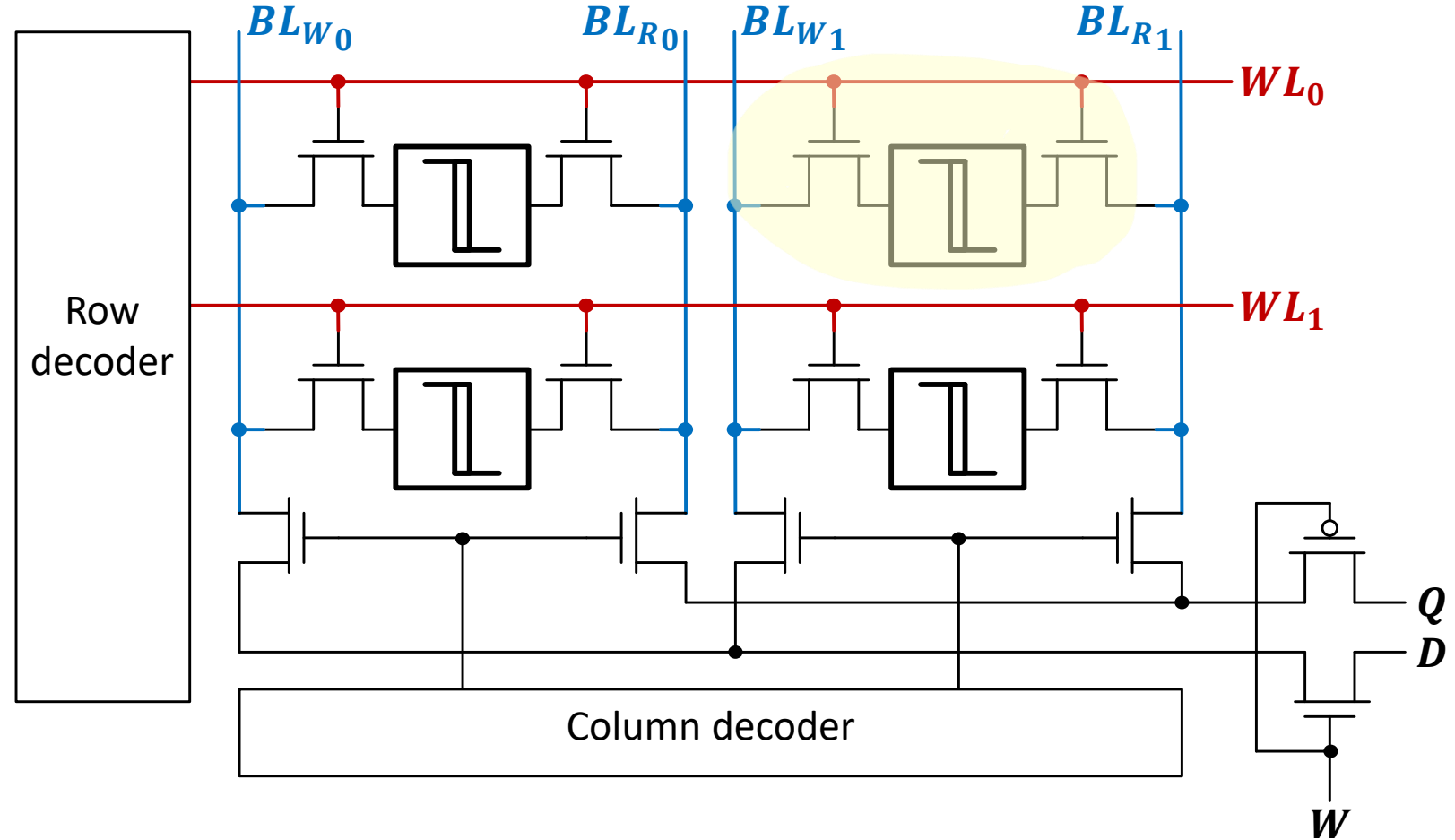*(handwritten below diagram: According to the address, col. dec. is activating the WBL.)*

SRAM – Architecture and working principle

- Example – 4x4
  - **Read**
    - Cell (0,1)

SRAM – Architecture and working principle

- Example – 4x4
  - **Read**
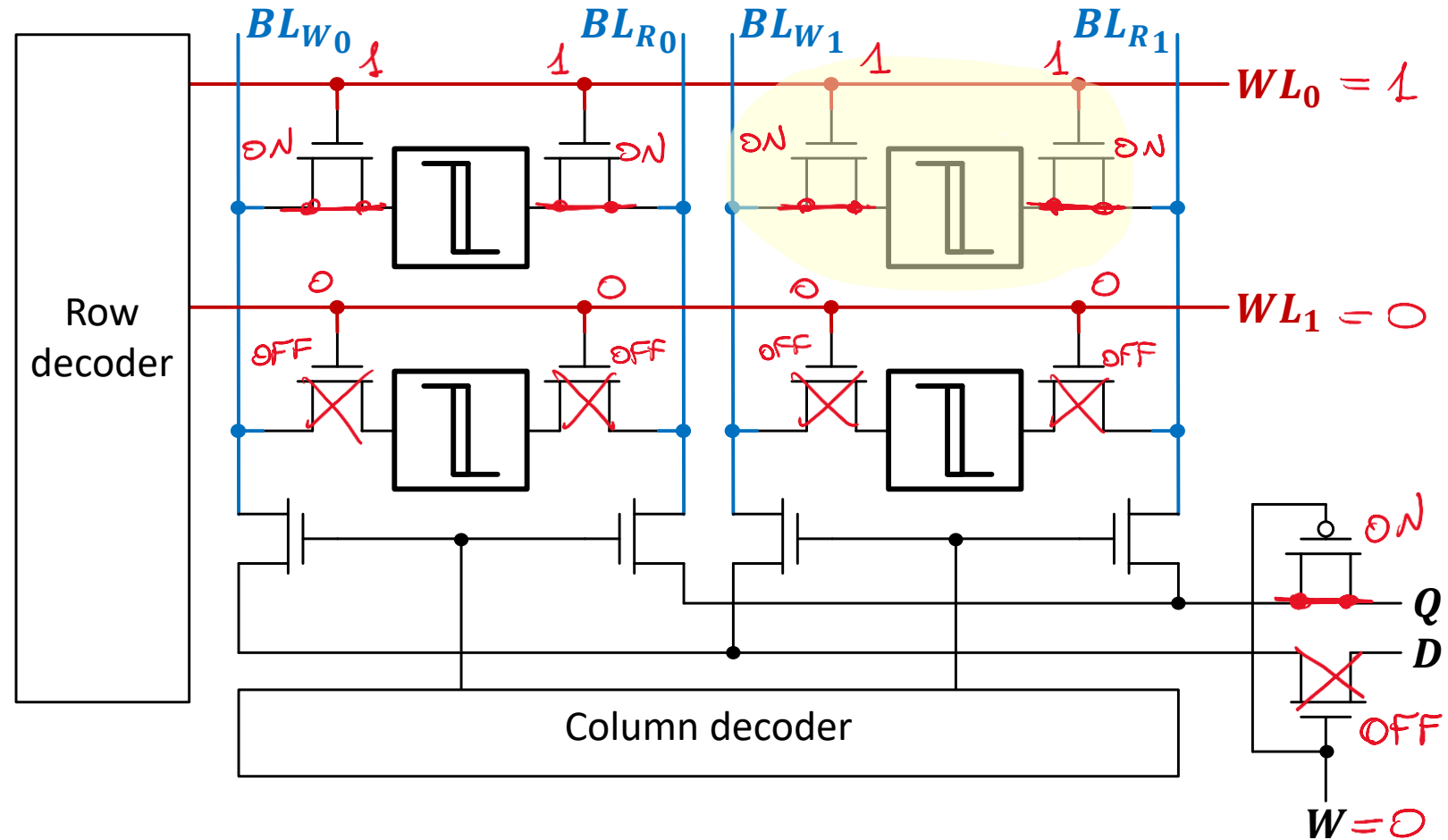   - Cell (0,1)

    - W = 0

SRAM – Architecture and working principle

- Example – 4x4
  - **Read**
    - Cell (0,1)
    - W = 0
    - $WL_0 = 1$
    - $WL_1 = 0$

SRAM – Architecture and working principle

- Example – 4x4
  - **Read**
    - Cell (0,1)
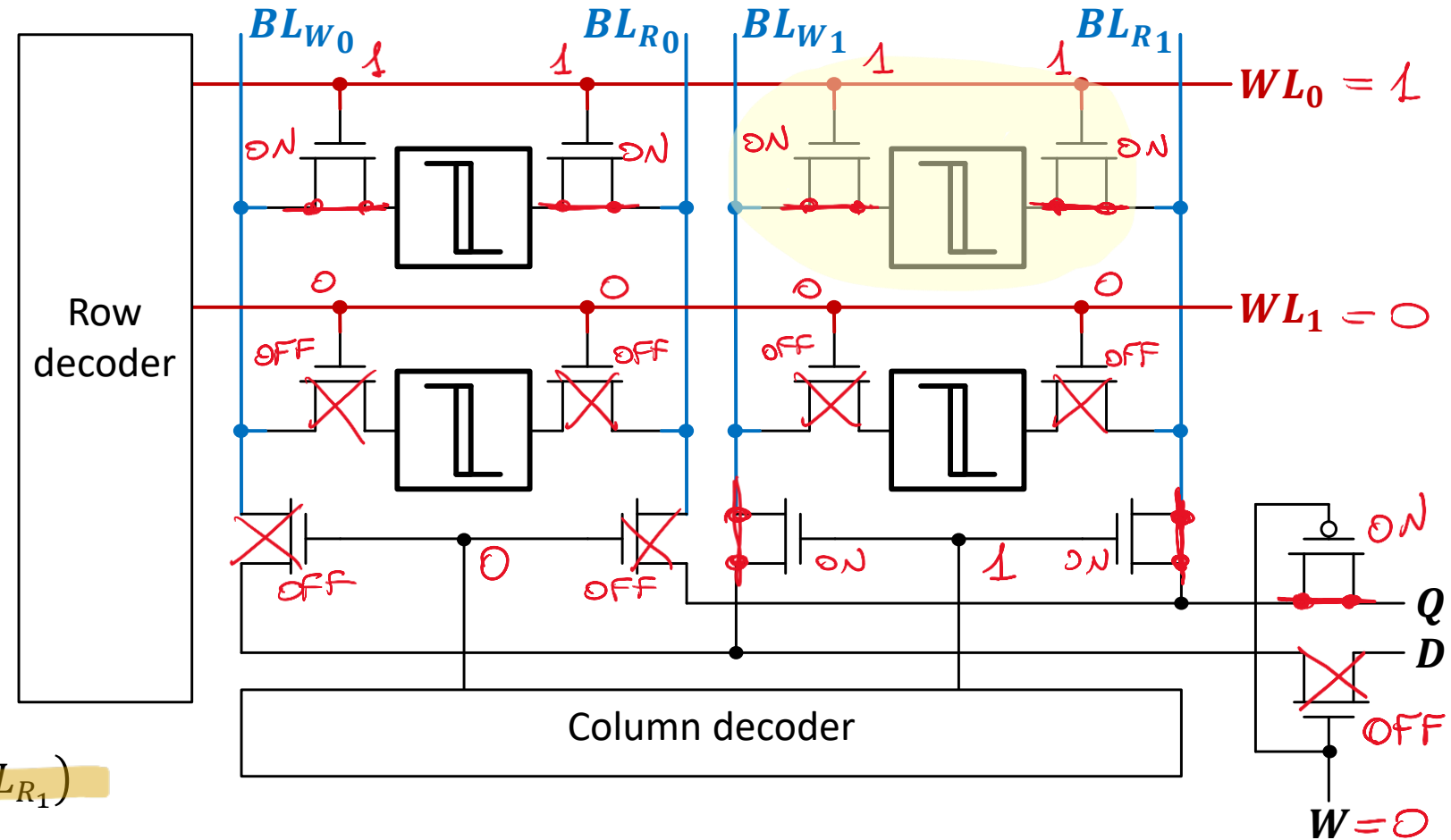   - W = 0
    - $WL_0 = 1$
    - $WL_1 = 0$
    - Column decoder
      - Activating access transistors of (BL_{W_1}, BL_{R_1})
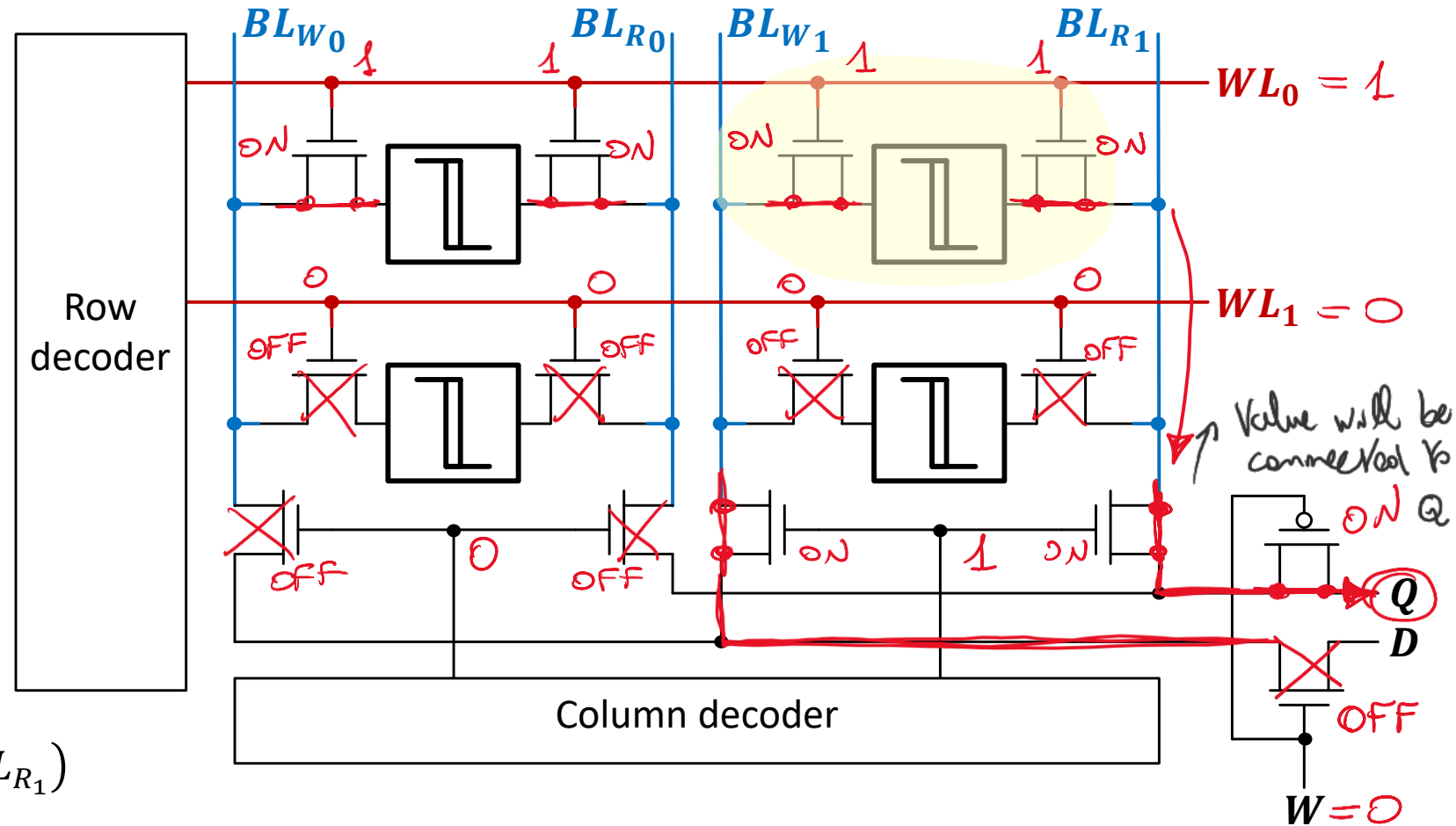
SRAM – Architecture and working principle
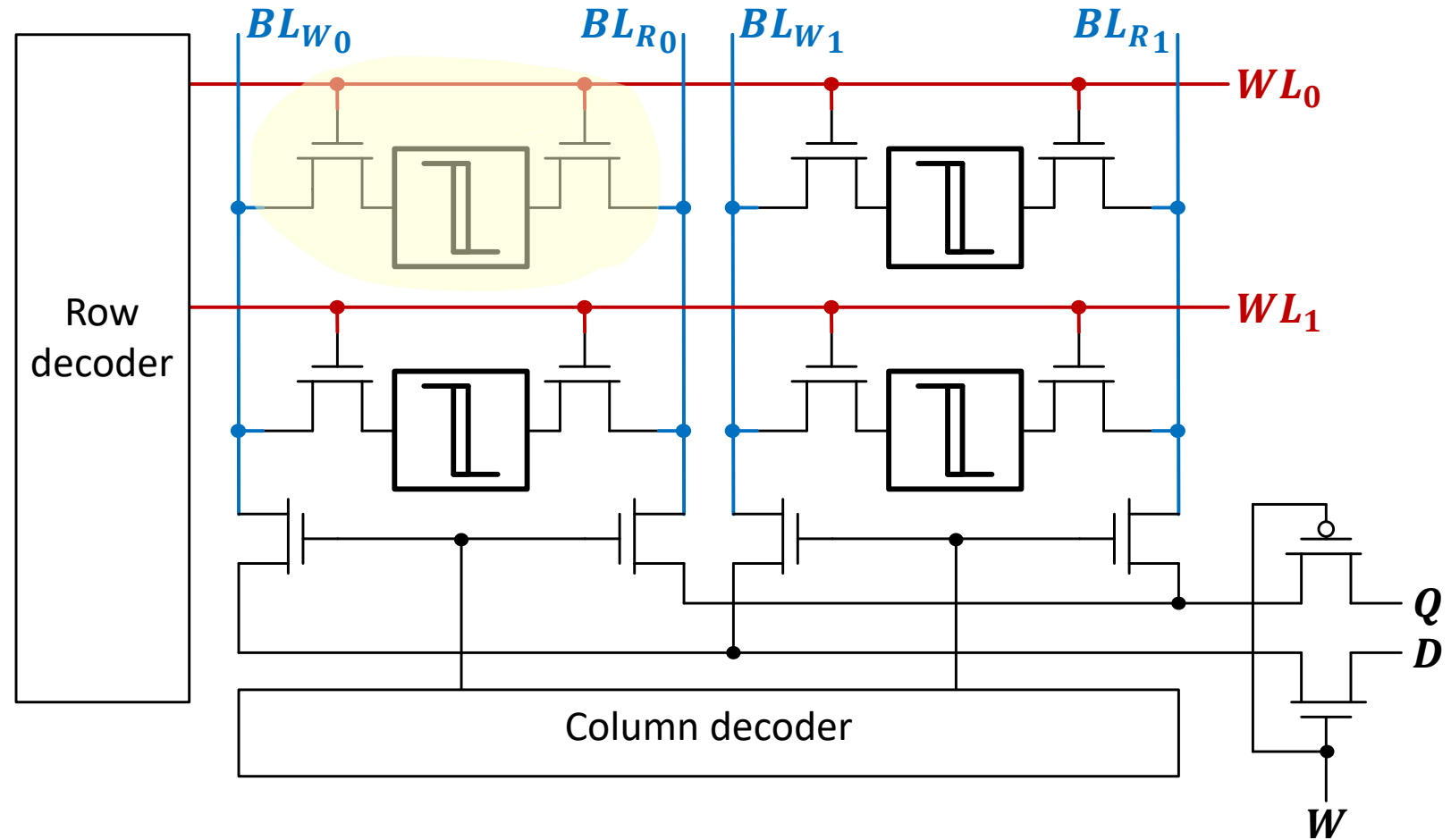
- Example – 4x4
  - **Read**
    - Cell (0,1)

    - W = 0

    - $WL_0 = 1$
    - $WL_1 = 0$

    - Column decoder
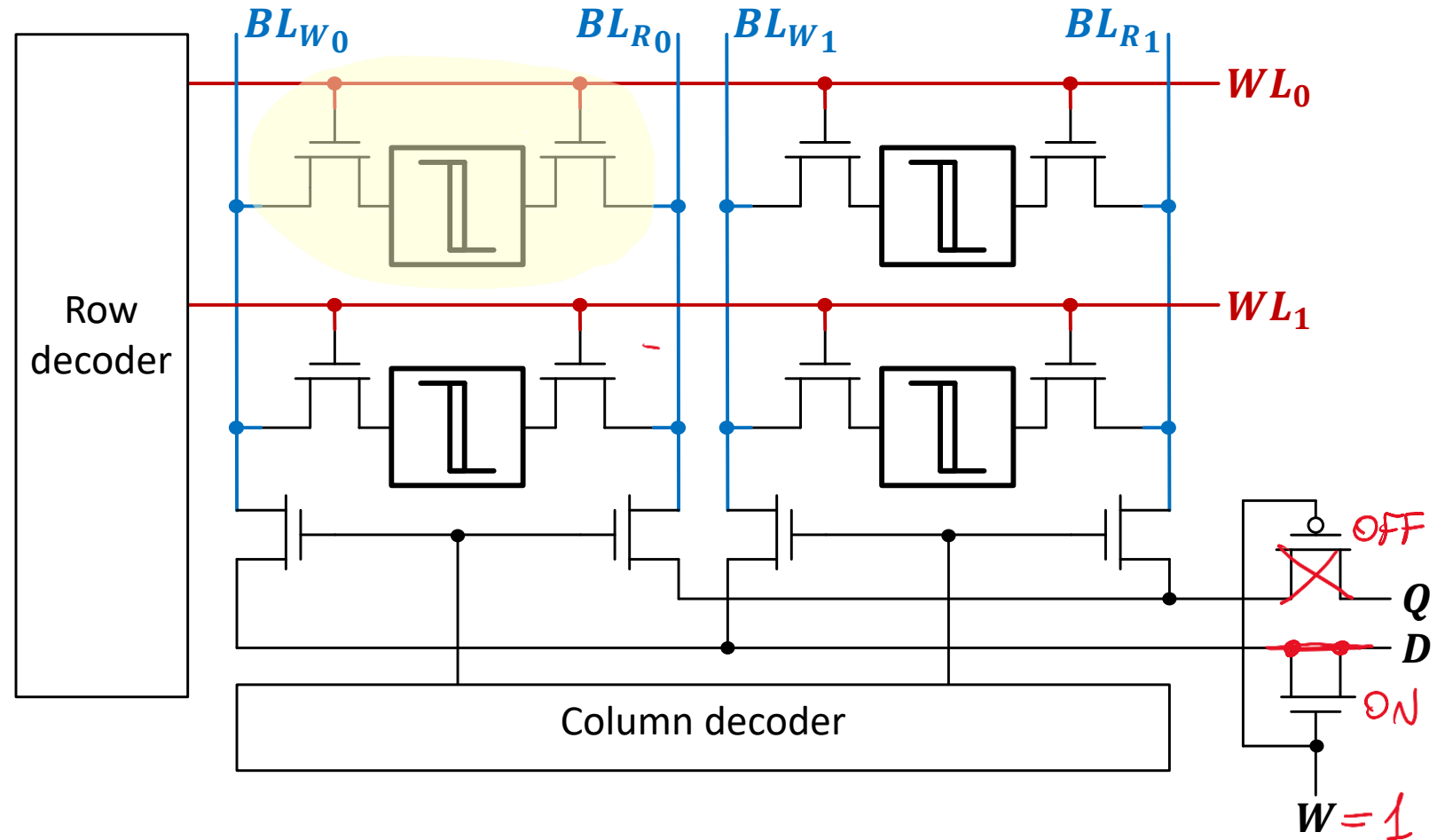   - Activating access transistors of (BL_{W_1}, BL_{R_1})

SRAM – Architecture and working principle

- Example – 4x4
  - **Write**
    - Cell (0,0)

SRAM – Architecture and working principle

- Example – 4x4
  - **Write**
    - Cell (0,0)

    - W = 1

SRAM – Architecture and working principle
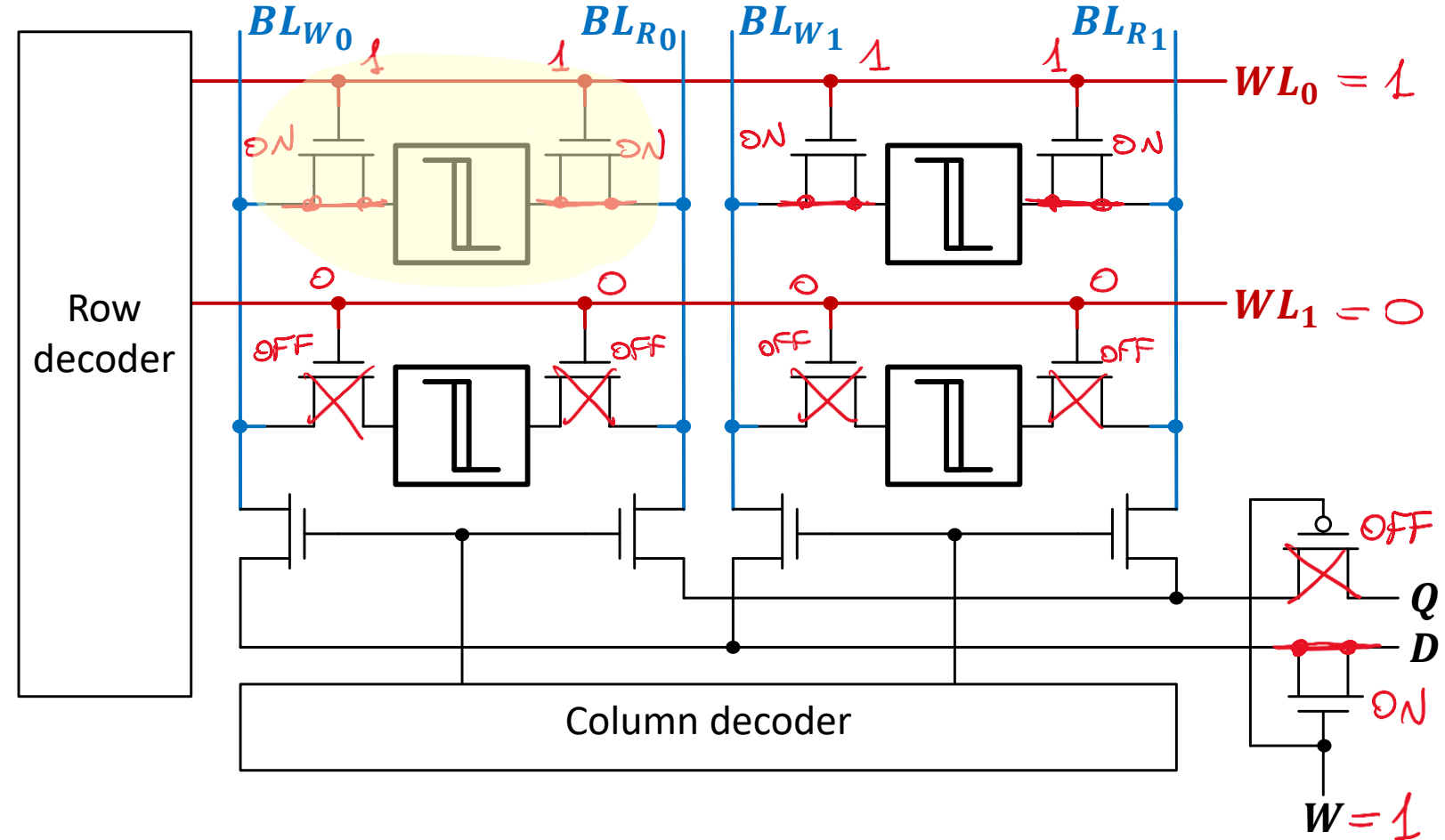
- Example – 4x4
  - **Write**
    - Cell (0,0)
    - W = 1
    - $WL_0 = 1$
    - $WL_1 = 0$

SRAM – Architecture and working principle

- Example – 4x4
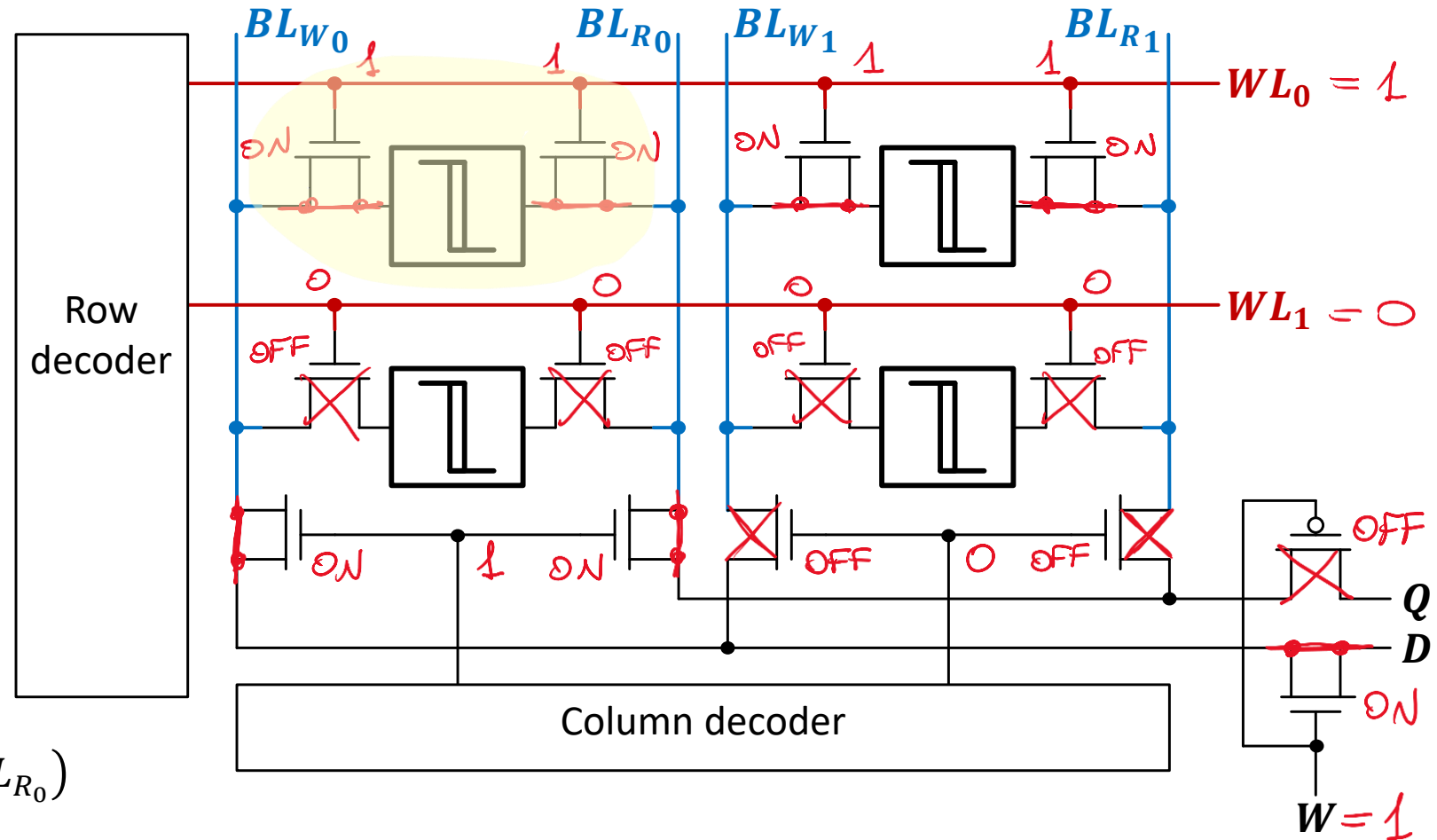 - **Write**
    - Cell (0,0)

    - W = 1

    - $WL_0 = 1$
    - $WL_1 = 0$

    - Column decoder
      - Activating access transistors of (BL_{W_0}, BL_{R_0})

SRAM – Architecture and working principle

- Example – 4x4
  - **Write**
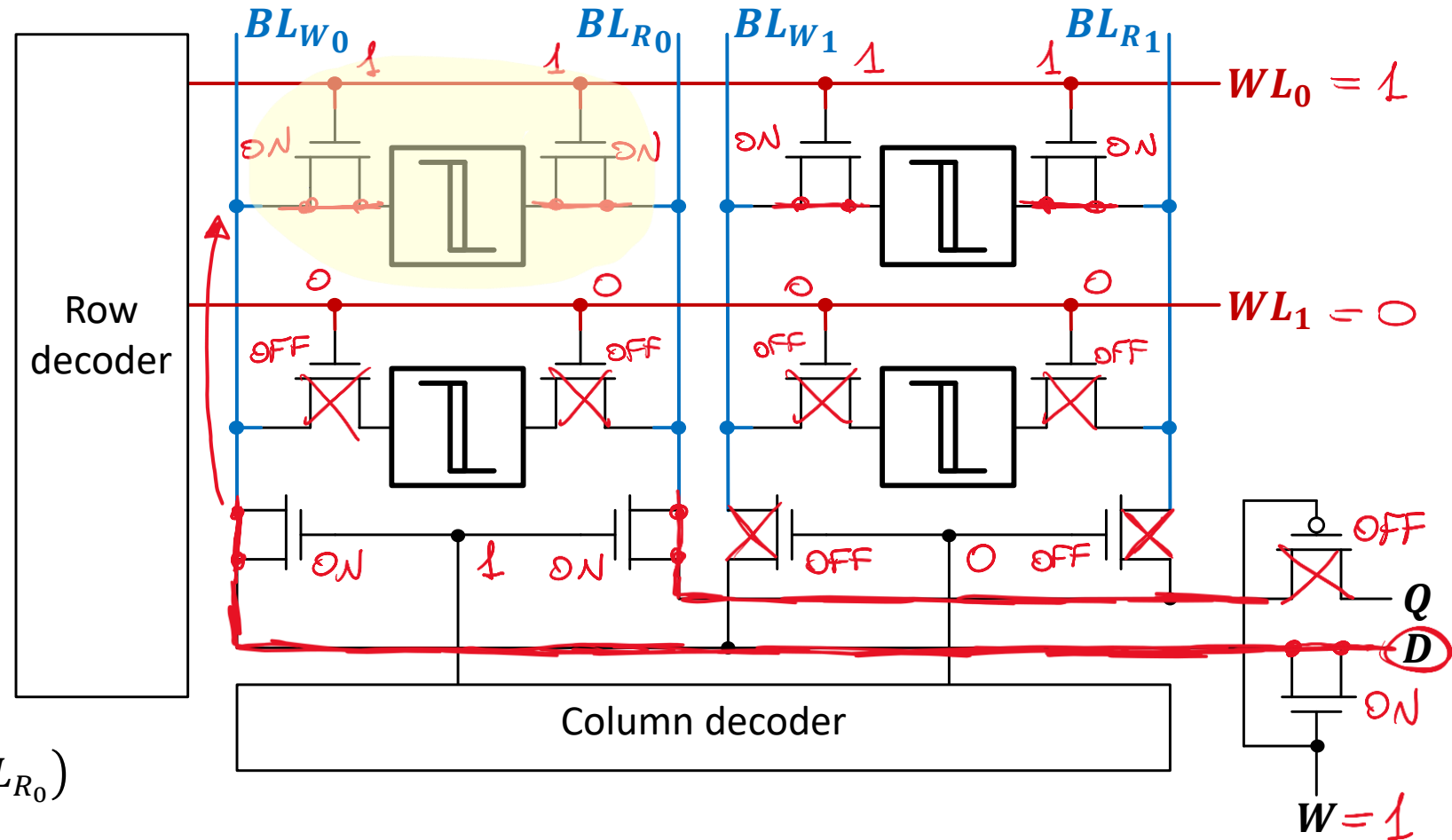   - Cell (0,0)

    - W = 1

    - $WL_0 = 1$
    - $WL_1 = 0$

    - Column decoder
      - Activating access transistors of (BL_{W_0}, BL_{R_0})

Thank you for your attention

Luca Crocetti
(luca.crocetti@unipi.it)