Any questions so far?

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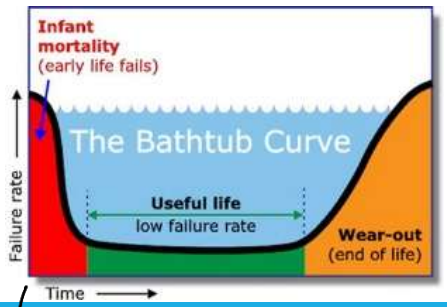
Recycled Components & Aging Phenomena

- **More than 80%** of the counterfeit components are **recycled**
- Most of the recycled parts are at the end of life → damaged considerably due to usage and **aging**



Failure rate as time goes on:
for a short lifetime period we have chips may stop working properly very soon: this is for production defects. Production is complex and we cannot avoid defects

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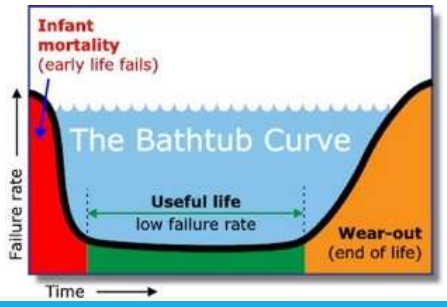
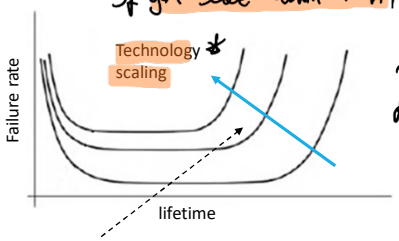
So these chips should be avoided. So we test chips to try to identify as many chips as possible. We can either destroy them or do failure analysis: understand what went wrong. So we now are in the useful life region.
After a bit, though, your system is going to wear out.

Recycled Components & Aging Phenomena

- **More than 80%** of the counterfeit components are **recycled**
- Most of the recycled parts are at the end of life → damaged considerably due to usage and **aging**



If you scale down tech, wearing out starts kicking in earlier and failure rate increases.



New aging mechanisms:
- Negative and Positive Bias temperature instability (NBTI, PBTI) (Mainly negative)
- Hot carrier injection (HCI) ①
- Time dependent dielectric breakdown (TDDB)
- …

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① HBr = highly energetic
② In MOS we have dielectric very thin, that can eventually (not abruptly) break down.
*With scaling, we refer to the size of transistors (the channel): $I_D \propto \frac{W}{L}$

DR0

injected carriers vs trapped carriers; dielectric gets weaker as electric fields are applied over it.

Basics on Transistor Aging Phenomena

- When the chip operates in functional mode, the **transistors age mainly due to NBTI** (**Negative Bias Temperature Instability**), and **HCI** (**Hot Carrier Injection**).
- The aging effects of NBTI and HCI can cause **parametric shifts** and circuit failures
- NBTI occurs when a negative gate-to-source voltage is applied at the pMOS transistors (i.e., when they are ON), which breaks Si-H bonds generating the interface traps → **NBTI is data dependent**!
- These interface traps can get electrically charged and increase the absolute value of the pMOS threshold voltage (V_{th}), resulting in reduced transistor current and increased gate delay
- HCI occurs in nMOS devices caused by the trapped interface charge at $Si=SiO_2$ surface near the drain end during switching that results a non-recoverable Vth degradation

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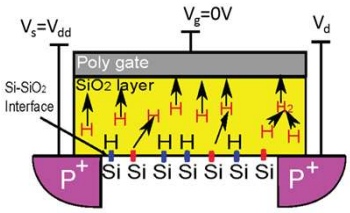
- NBTI, PBTI could really be neglected with larger components. But for tech nodes before 80-60nm, those are limpacking.

- Problem is related

defects we can find for transistors. Related to potential wells that are able to trap electrons (due to impurities you have during production) Because of quantistic phenomena like tunnel effect that makes electrons fall in the well without having potential. So effect is that threshold voltage increases, so I_D smaller.

What happens to MOS transistors as they age? (I)

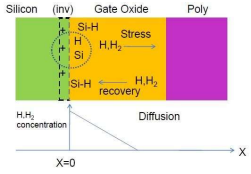
- Aging effects: physical description



$$\Delta V_{th} = \frac{qN_{it,NBTI}(t)}{C_{ox}}$$

$N_{it,NBTI}$: interface traps generated by NBTI

- A similar effect take place for HCI:
  - HCI occurs when the electron or hole in the transistors gains sufficient energy to overcome the silicon dioxide barrier in order to break an interface state → interface traps are generated



$$\Delta V_{th} = \frac{qN_{it,HCI}(t)}{C_{ox}}$$

$N_{it,HCI}$: interface traps generated by HCI

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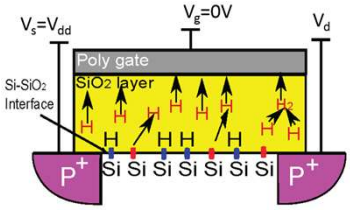
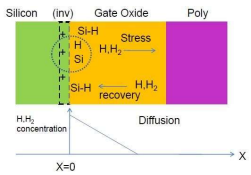
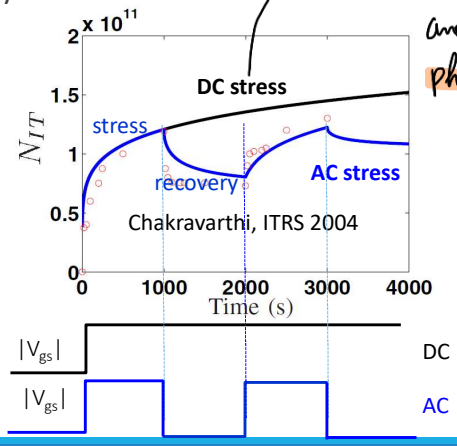
What happens to MOS transistors as they age? (II)

- NBTI: stress and recovery







- Recovery is only partial → net threshold voltage increase over time

deterioration kind of saturates over a while and you have recovery. But main physical driver of degradation is $\Delta V_{th} = \frac{qN_{it,NBTI}(t)}{C_{ox}}$ Temperature and electric fields: you have a recovery, so V_{th} starts decreasing again but does'nt get back to nominal value. So over time, you still have degradation. Transistor degrades when it is on, partially recovers when is off. Degradation of a component is data dependent. (Recovery happens for trapped charges)

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NMOS is on with logic 1 and off with logic 0. Depends on the workload we are going to process. This is bad for designers.

To tackle this problem, designers make systems slower. You lose performance at the very beginning of course.
You can even adjust frequency of circuits overtime. Systems embed performance monitors overtime to look at your degradation rate and slow down clock signals or voltage supply.

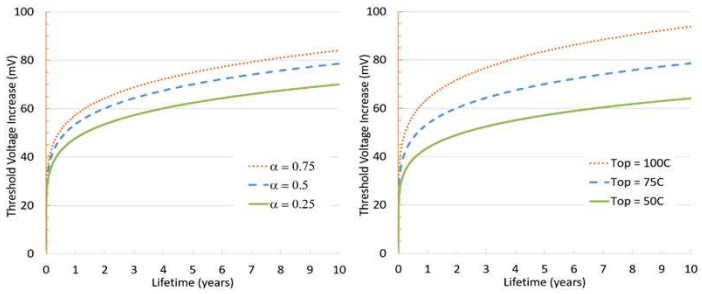
Temperature worsen time degradation; α = stress ratio: components are mostly on: α high.

What happens to MOS transistors as they age? (III)

- NBTI: analytical modelling

$$\Delta V_{th} = \xi K \sqrt{C_{ox}(V_{gs} - V_{th0})} e^{-\frac{E_a}{kT}} (\alpha t)^{\frac{1}{6}}$$

α: stress ratio
T: operating temperature
t: operating time (lifetime)
E_a: activation energy



(32 nm CMOS technology at T ambient)

Stress ratio: ratio between the amount of time during which the device is under stress (ON) and the overall operating time → **Stress ratio accounts for NBTI aging data (workload) dependency**

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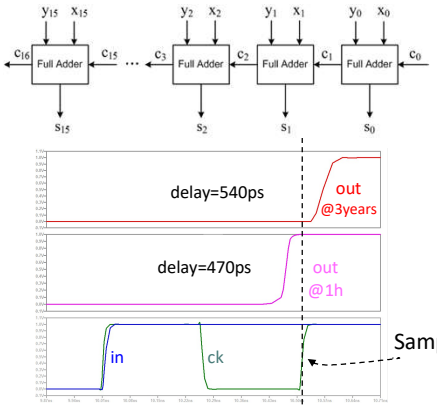
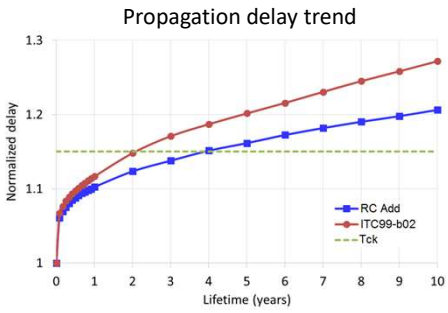
Aging Effects in Electronic Circuits Performance (I)

- The overall (and well characterized) effect is that electronic circuits get slower





- Propagation delay degradation can lead to the sampling of a wrong data → reliability issue → Lifetime (LT) reduction

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You can use the model up there as a model for ΔV_{th} over time.

C_{ox} = oxide capacitance

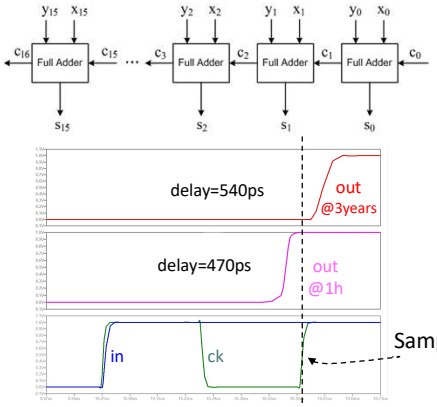
Example of simulation on ripple carry adder. You do a simulation for the worst case propagation delay τ_{pd} → this leads you to the minimum $T_{clk\,min}$ → then you select the real $T_{ck} = T_{ck\,min}(1 + \%)$

↳ percentage of slack

NOTE: What is the signal that is experiencing the worst prop. delay? C_{16} is the one. And after ΔV_{th} estimation, we have a delay of 470 ps in 1h, but in 3 years you get 510 ps. If you want to have an idea of survival time, you can plot propagation delay over time (this is the worst case). So you can increase the slack to get better results.

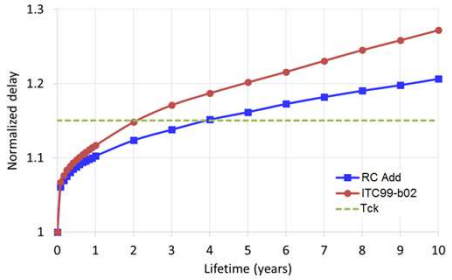
Aging Effects in Electronic Circuits Performance (II)

- The overall (and well characterized) effect is that electronic circuits get slower



Sampling clock edge

Propagation delay trend



- 15% time margin:
  - LT_{itc} = 2.1 years
  - LT_{add} = 4 years

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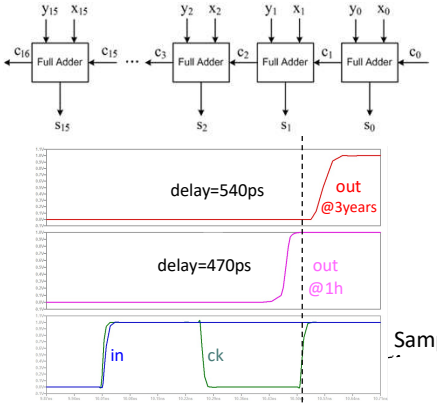
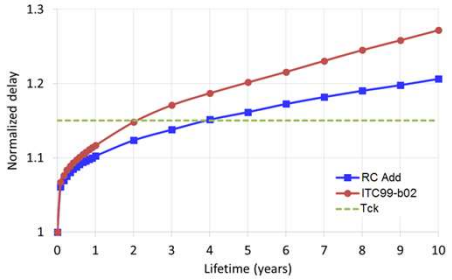
Aging Effects in Electronic Circuits Performance (III)

- The overall (and well characterized) effect is that electronic circuits get slower



Sampling clock edge

Propagation delay trend



- 20% time margin:
  - LT_{itc} = 4.8 years
  - LT_{add} = 9 years

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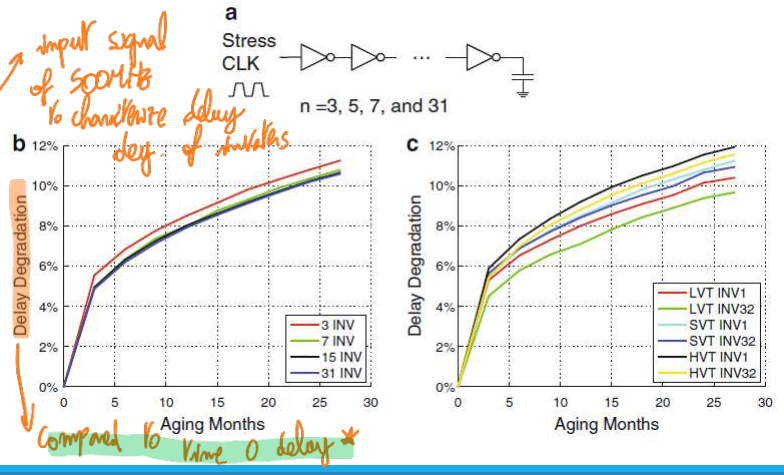
Aging Effects Analysis for Recycled IC Detection (I)

- Example: inverter chain
- Inverter chains with the same capacitive load and the same stress coming from a 500 MHz clock
- These chains are composed of 3, 7, 15, and 31 standard, high, and low threshold voltage (SVT, HVT, and LVT) inverters



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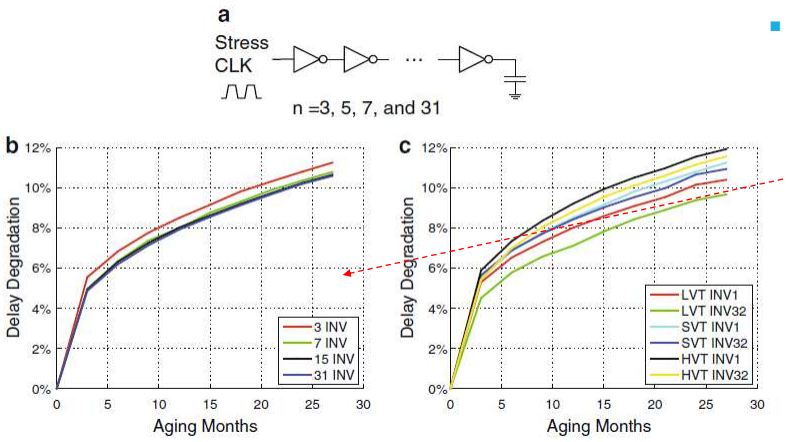
Aging Effects Analysis for Recycled IC Detection (II)



- Delay degradation of inverter chains under clock stress for up to 27 months with no interruption
  - Fig. b: the **number of inverters does not have a significant impact** on the degradation of these chains since they receive the same stress, and each inverter's speed degrades at the same rate

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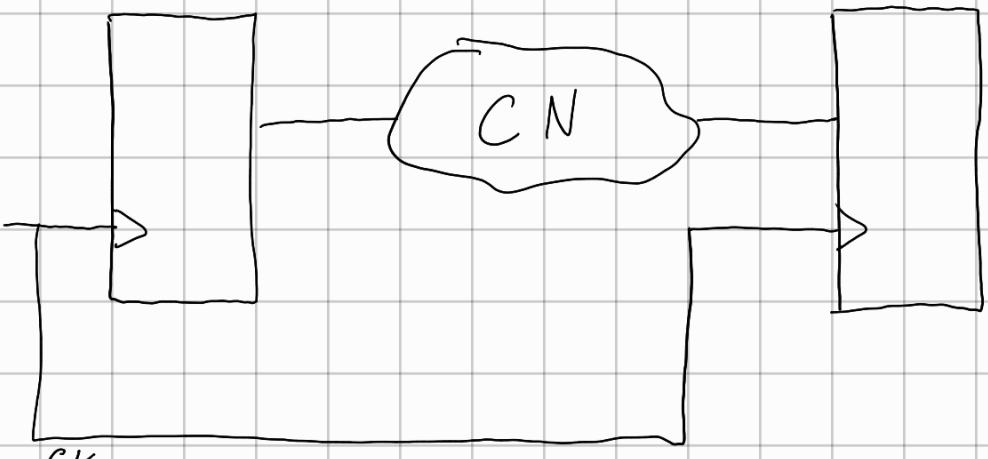
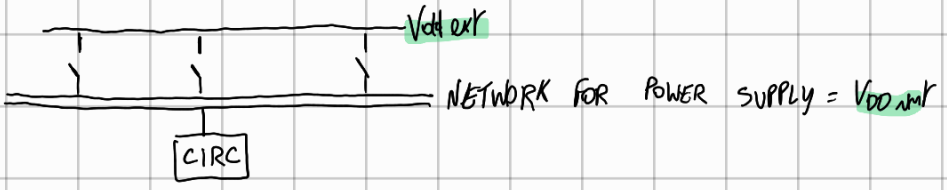
① Components with higher threshold voltage are experiencing highest levels of degradation. This is for construction physical defaults.

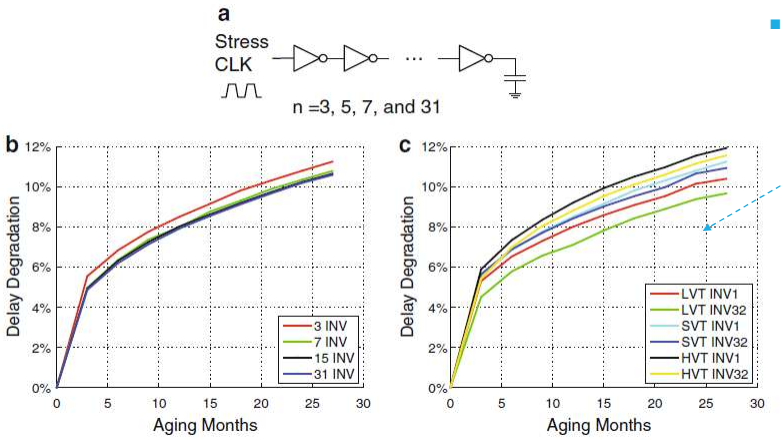


↳ switching from 0 to 1, even if CN doesn't have anything useful for a while. So you can turn off the clock and save power: CK, En

- This is called clock gating. This reduces dynamic power.
- To reduce static power consumption, you can turn off voltage supply! Power gating



Aging Effects Analysis for Recycled IC Detection (III)



- Delay degradation of inverter chains under clock stress for up to 27 months with no interruption
  - Fig. c: the chain with the **HVT inverters** experiences **more degradation** than the chains with the SVT or LVT inverters,
  - the **INVX1** inverter chain has a **larger degradation** than the INVX32 inverter chain

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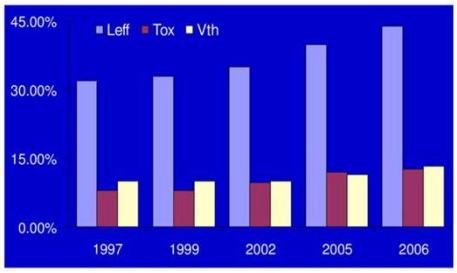
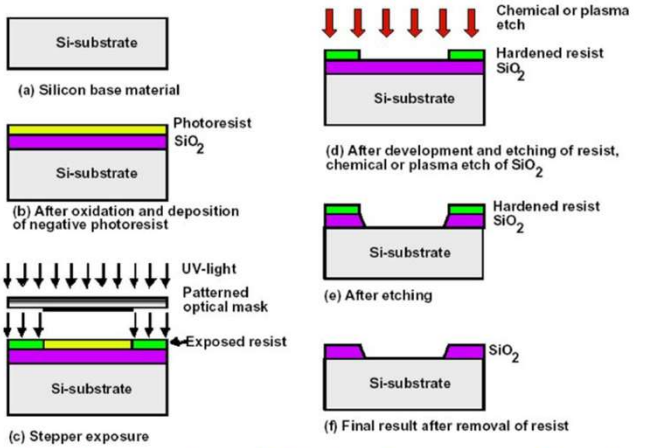
Lithography Manufacturing Process

Process variations trend



Process variations keep increasing as technology scales down



- As technology scales, all kinds of sources of variations
  - Critical dimension (CD) control for minimum feature size
  - Doping density
  - Masking

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Another interesting phenomena: process variations. When you scale down the technology, the manufacturing mechanisms become increasingly complex.
Photolithography is one of the main manufacturing mechanisms that need to be performed, and defining component parameters precisely gets harder.
Components are characterised by W, L, V_{TH}..., that have impact on performance.
Problem is that these parameters cannot be really defined very precisely.
So in complex circuits we will have transistors ideally the same, but upon closer looks, we don't have a specific value.

In reality we have a distribution.

Effect: components that should behave the same, will have different performances.
If we pick a component in A and B, A will be more performing than B.

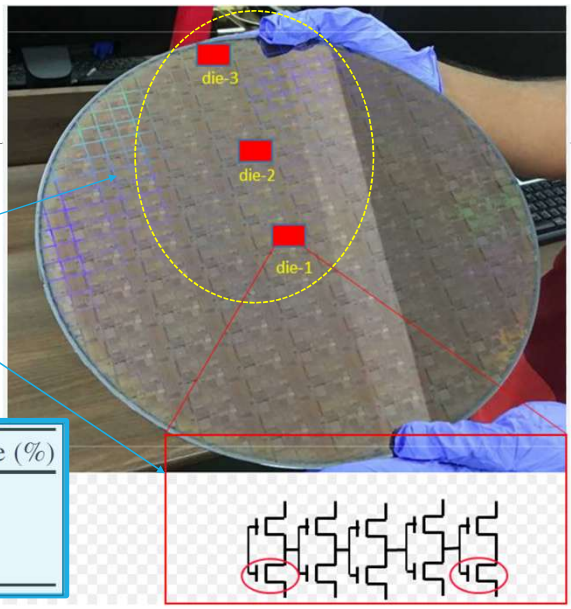
- This is process variation (for one IC, you have one value in this distribution)

IDEA: I can compare component with a new one to see if they are recycled.
But for a new component I don't know precisely the performances!
And as we scale down, this difference is even bigger.
As a reference, assume I am in A with a new component. I take another that falls in B. How can I tell if I was unlucky and component is new or if I have a recycled one?

You have different chips within a wafer and they exhibit different variations

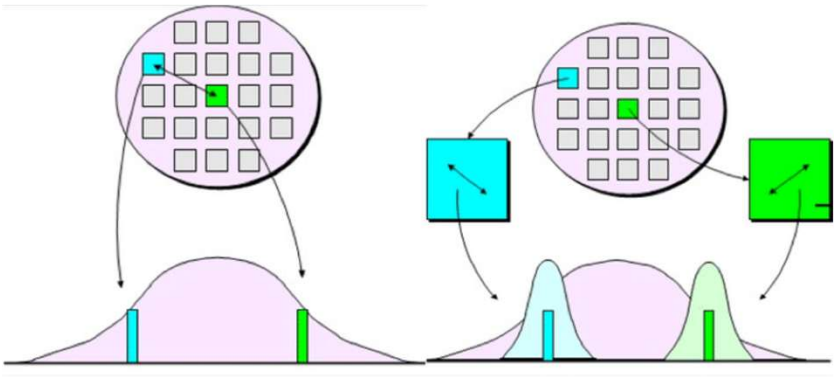
Process Variations

- There can be both
  - Die-to-Die (D2D), or inter-die variations, and
  - Within-Die (WID), or intra-die variations



Parameter	Inter-die (%)	Intra-die (%)
Threshold voltage (V_{th})	20	5
Channel length (L)	8	2
Oxide thickness (T_{ox})	4	1

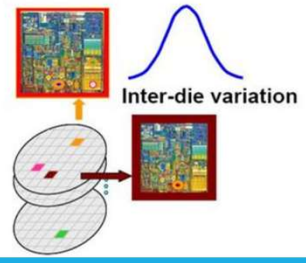
Process Variations

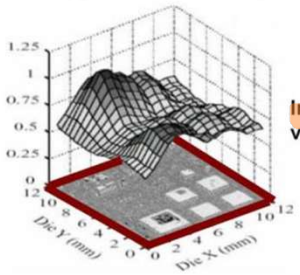


- Die-to-Die (D2D), or inter-die variations
- Within-Die (WID), or intra-die variations

Process Variations

- Inter-die vs intra-die variation
  - Inter-die variation: same devices at different dies are manufactured differently
  - Intra-die (spatial) variation: same devices at different locations of the same die are manufactured differently





It is location dependent

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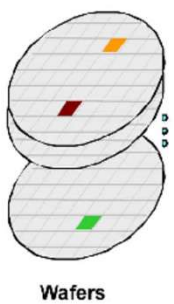
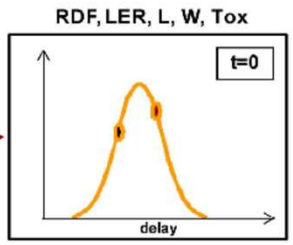
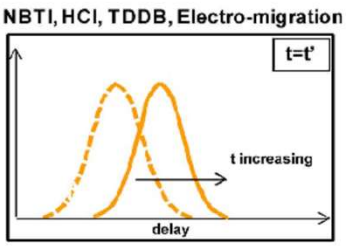
Process Variations and Aging







After a while the distribution shifts
This shape might become longer

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Intel characterizes processors based on their performance. They run tests and sell components on the left as max operating frequency components at maximum price. Tests are called speed binning.

Some interesting videos

- What's inside a microchip? http://www.youtube.com/watch?v=GdqbLmdKgw4
- Zoom Into a Microchip http://www.youtube.com/watch?v=Fxv3JoS1uY8
- Counterfeit Electronics Could Be Dangerous, Funding Nefarious People http://www.youtube.com/watch?v=dbZiUe6guxc
- How Computers and Electronics Are Recycled (about proper electronic waste management) http://www.youtube.com/watch?v=Iw4g6H7alvo
- Counterfeit Electronic Components Process http://www.youtube.com/watch?v=5vN_7NJ4qYA
- Counterfeit Visual Inspection http://www.youtube.com/watch?v=MbQUvu2LN6o
- Gold from waste circuit electronics http://www.youtube.com/watch?v=ZkhOuNvkuu8 (no longer available)

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Any questions?

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