

Electronics Systems

LM Cyber Security – Fall 2024

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This slides have been adapted from the lecture given by Prof. Roberto Saletti in the previous years

# Data conversion

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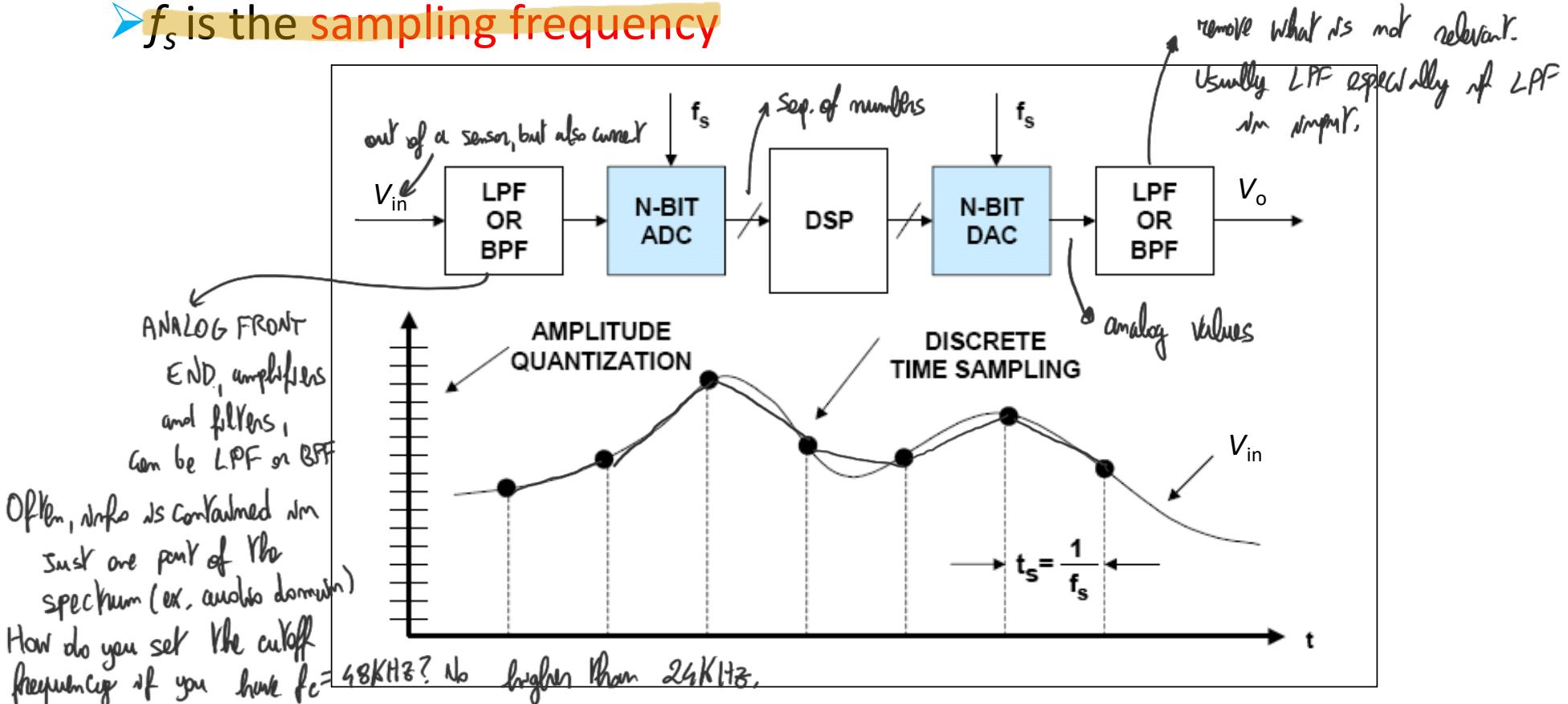
# Digital representation of signals

Real world is analog, but process is

- How is it possible to represent analog signals with digital numbers? digital
  - Sampling Theorem due to Shannon gives sampling frequency constraint
- Passage from continuous-time to discrete-time
- Analog signals can be represented and processed as sequences of numbers with no losses
- How is it possible to represent analog signals with digital numbers?
  - Quantization of the signal levels
- The numbers representing the signal samples are expressed in binary form with fixed number of digits
  - We already have noise
- A sequence of binary numbers represents the analog signal with loss

# Basic Sampling Theory

➤  $f_s$  is the sampling frequency



Often, noise is contained in  
just one part of the  
spectrum (ex, audio domain)

How do you set the cutoff  
frequency if you have  $f_c = 48\text{kHz}$ ? No higher than  $24\text{kHz}$ .

# The Nyquist Criterion

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- A continuous analog signal is sampled at discrete intervals  $t_s = 1/f_s$  ( $f_s$  is the sampling frequency)
- $f_s$  must be carefully chosen for an accurate representation of the original analog signal
- The sampling frequency must be at least twice the highest frequency contained in the signal
- If the Nyquist Criterion is not satisfied information about the signal will be lost [Um sample per unit  $f_s < 2B$  will cause aliasing]
- A phenomenon known as aliasing occurs when the sampling frequency is less than twice the maximum analog signal frequency

# Fundamentals of data conversion

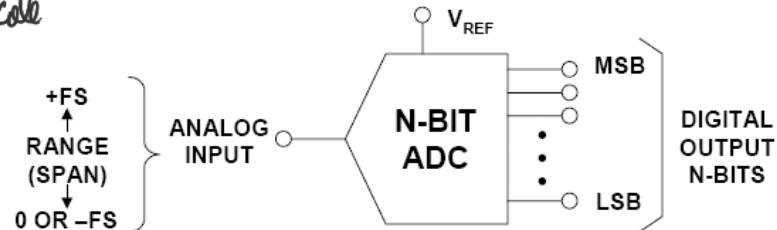
## ➤ Analog-to-Digital converters (ADCs)

- Translate “real world” analog quantities to digital language

## ➤ Digital-to-Analog converters (DACs)

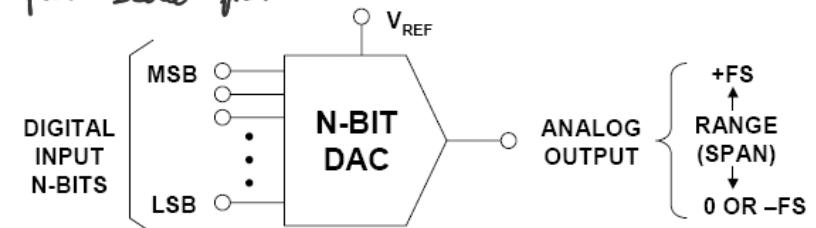
- Transform the results of digital processing back to the “real world”

$FS = \text{full scale}$



Unipolar: scale from 0 to FS

Bipolar: scale from -FS to FS



$V_{REF}$  is a voltage that rules the behaviour of the converter. Important that it is an accurate value. Errors introduced depend on the accuracy of

The  $V_{REF}$ :

$$q = \text{LSB} = \frac{V_{ref}}{2^N}$$

↓  
quantit. step

DAC: number of input × quantit. step for output.

• What is the conversion law for the ADC? Imp 8

# Signal Quantization

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- Analog signals can be represented by sequences of numbers
- Possible analog values are continuous and thus infinite
- Digital values are finite
  - 8 bit represents  $2^8 = 256$  digital values
  - 16 bit represents  $2^{16} = 65536$  digital values
- How we manage with that?
- Quantization (approximation) of the sampled value to the nearest digital value
- It means an error is always added by the quantization process



# Analog to Digital Converter (ADC)

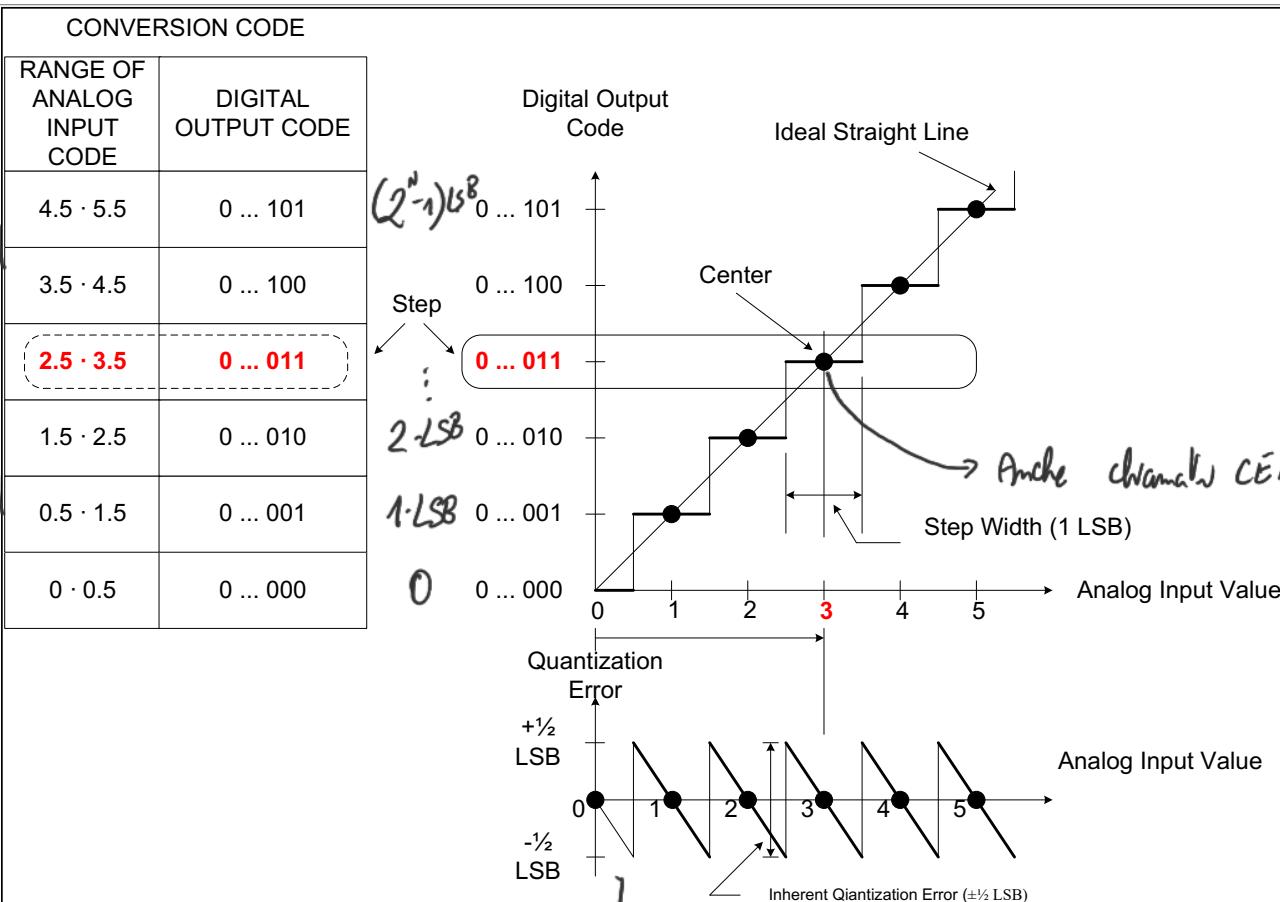
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- An electronic component that:
  - Samples the input signal at the sampling frequency
  - Provides a sequence of digital numbers as output
- The sequence of digital numbers consists of the quantized values of the samples of the input signal
- The ADC transfer function describes the relationship between analog input and digital output

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# ADC Ideal Staircase Transfer Function

How are the thresholds for value posed?  
On the X-axis, multiples of LSB (4). The threshold is placed between two multiples of the quantizer step. This for unipolar converters. Why are thresholds set in this way?

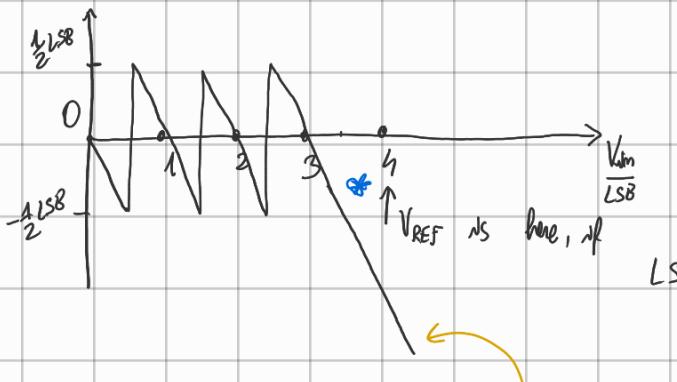


① Error band located between  $[-\frac{1}{2} \text{ LSB}, \frac{1}{2} \text{ LSB}]$

Thresholds are put in between two multiples of quantizer step. This choice of threshold gives this error. ① ←

$$\text{Full Scale: } FS = V_{ref} \quad N=2$$

$$E = \text{LSB} \cdot \text{out} - V_{in} \quad [\text{QUANTIZATION ERROR: OUT of CONVERTER} \times \text{LSB} - V_{in}]$$



$$\text{LSB} = \frac{V_{ref}}{2^N} \quad \text{and} \quad \text{out} =$$

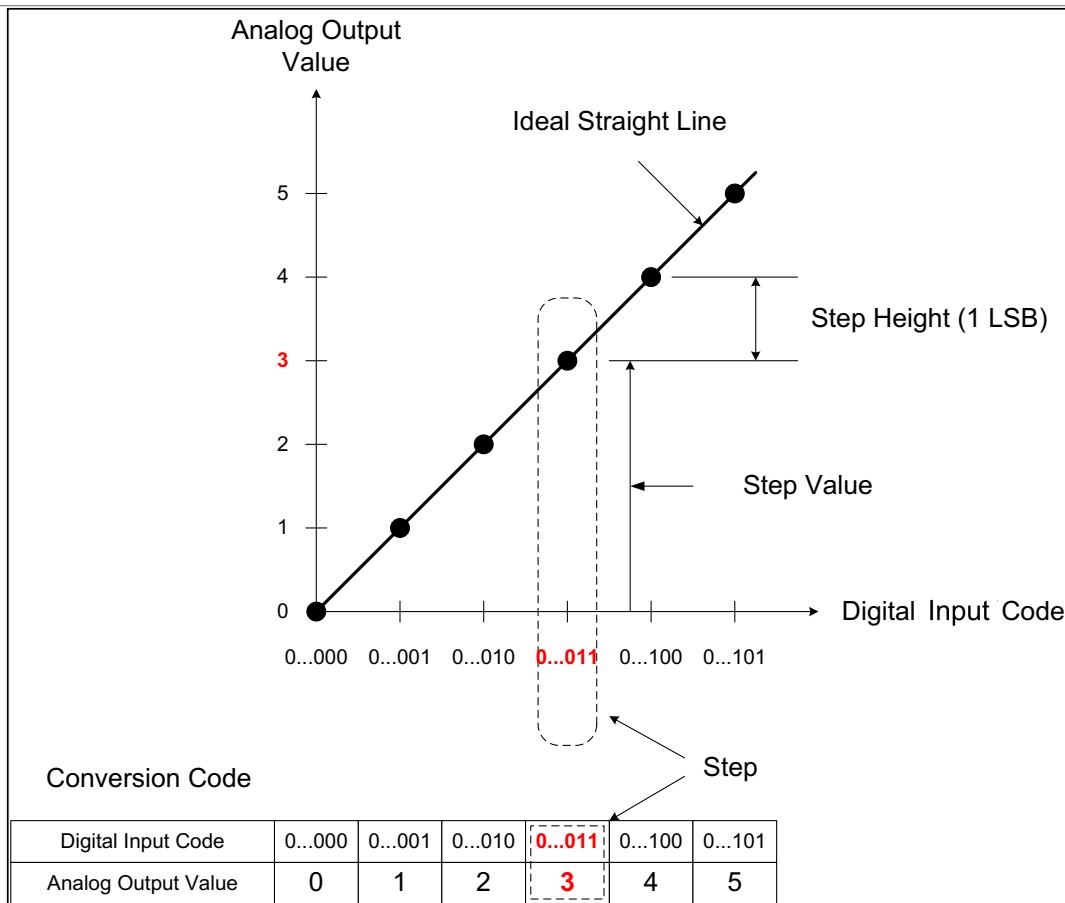
We cannot express more than  $V_{in}$  than  $V_{REF} - \frac{LSB}{2}$  [in practice, to avoid damage, not apply  $V_{in} > V_{ref}$ ]

\* Error behaviour is only true up to  $V_{REF} - \frac{LSB}{2}$ , because we do not go over to the next value.

$$\text{OUT} = \left\lfloor \frac{V_{in} + \frac{LSB}{2}}{LSB} \right\rfloor \quad \leftarrow \text{changes exactly at the threshold}$$

NOTA: in practice, la posizione della soglia non è esatta.

# DAC Ideal Transfer Function

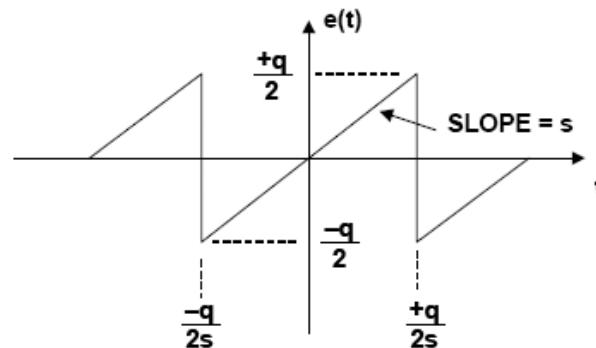


Number multiplied by LSB.

$$\text{out. LSB} = \text{out. } \frac{\text{ref}}{2^N}$$

# Quantization Noise as a Function of Time

- An error is always committed in quantization
- Quantization error range is  $\pm \text{LSB}/2$
- Root Mean Square error is  $\text{LSB}/\sqrt{12}$
- LSB (Least Significant Bit) amplitude is fundamental
- ADC resolution =  $N$  (number of bit)



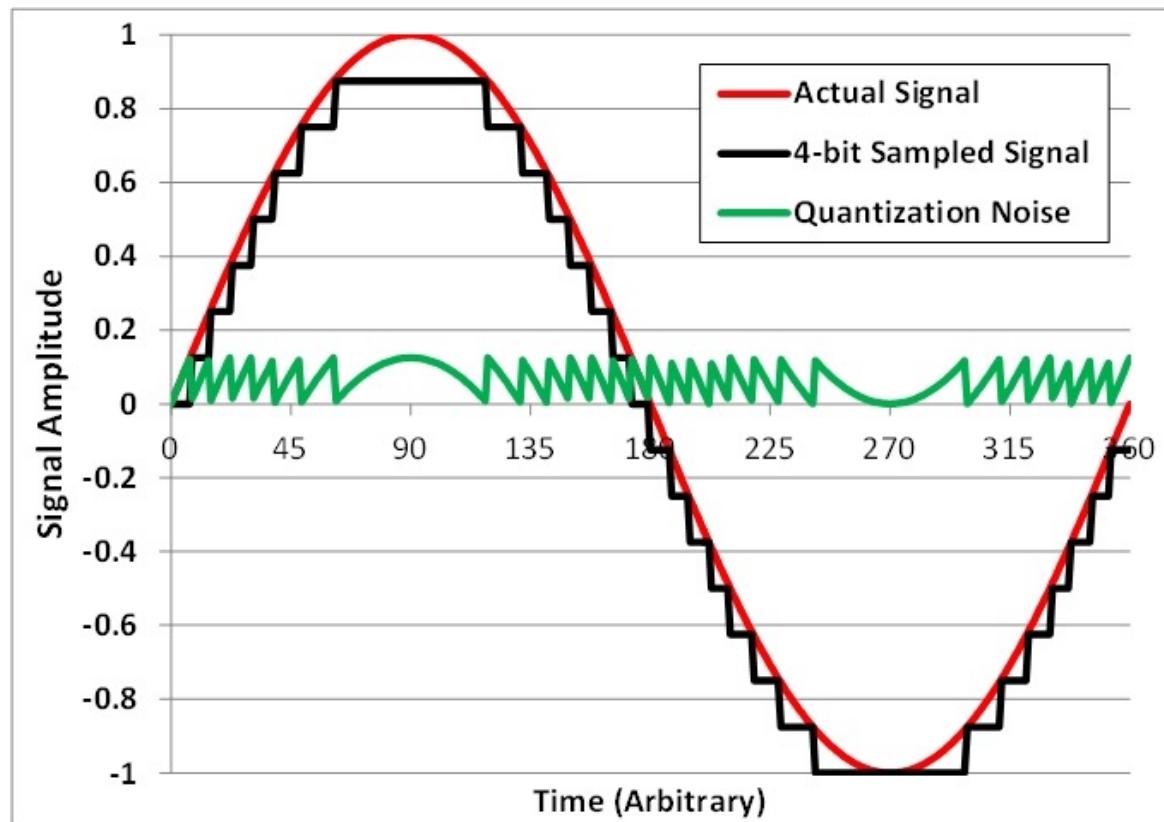
◆ ERROR =  $e(t) = st$ ,  $-\frac{q}{2s} < t < \frac{q}{2s}$

◆ MEAN-SQUARE ERROR =  $\overline{e^2(t)} = \frac{s}{q} \int_{-q/2s}^{q/2s} (st)^2 dt = \frac{q^2}{12}$

◆ ROOT-MEAN-SQUARE ERROR =  $\sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}}$

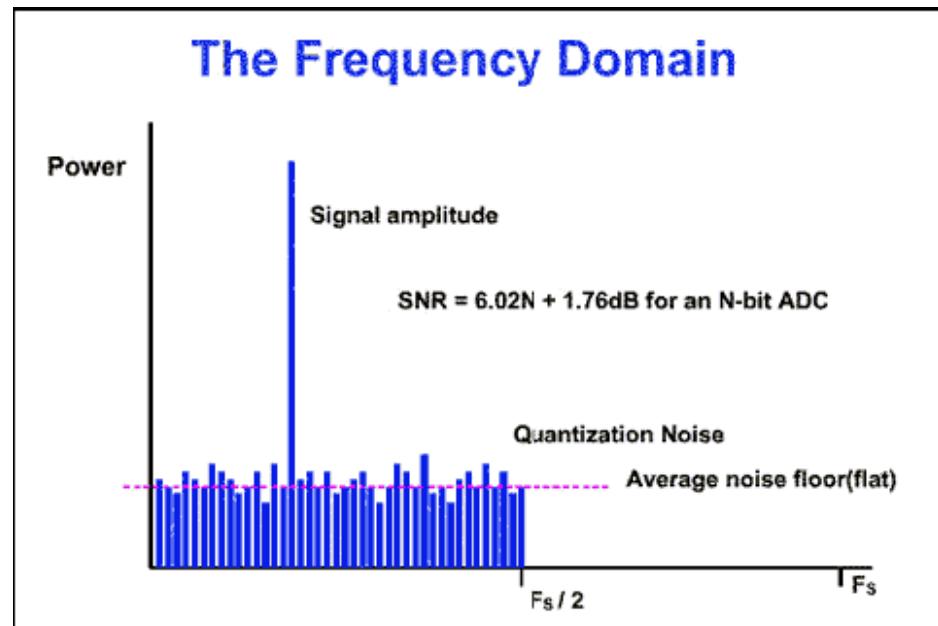
If you imagine input ranges from 0 to  $V_{REF} - LSB$  as uniformly distributed,  
the error can be seen as a random variable ranging from  $-\frac{LSB}{2}$  to  $\frac{LSB}{2}$ , with  
standard deviation =  $\frac{q}{\sqrt{2}}$

# Quantization error of a sine wave



# FFT of an ADC sampled and quantized sine

- This noise is approximately Gaussian
- It spans rather uniformly over the Nyquist bandwidth from 0 to  $f_s/2$
- Signal-to-Noise (SNR) ratio is the ratio between the power of signal and the power of quantization noise



# Signal-to-Noise Ratio of a N-Bit Converter

◆ FS INPUT =  $v(t) = \left[ \frac{q 2^N}{2} \right] \sin(2\pi f t)$

◆ RMS Value of FS Sinewave =  $\frac{q 2^N}{2\sqrt{2}}$

◆ RMS Value of Quantization Noise =  $\frac{q}{\sqrt{12}}$

◆  $\text{SNR} = 20 \log_{10} \left[ \frac{\text{RMS Value of FS Sinewave}}{\text{RMS Value of Quantization Noise}} \right] = 20 \log_{10} 2^N + 20 \log_{10} \sqrt{\frac{3}{2}}$

SNR increases  
linearly with the  
number of bits,  
coefficient is around 6.

$\text{SNR} = 6.02N + 1.76 \text{dB}$

(Measured over the Nyquist Bandwidth : DC to  $f_s/2$ )

With a sine  
wave spanning  
all the full  
scale

# Other sources of error

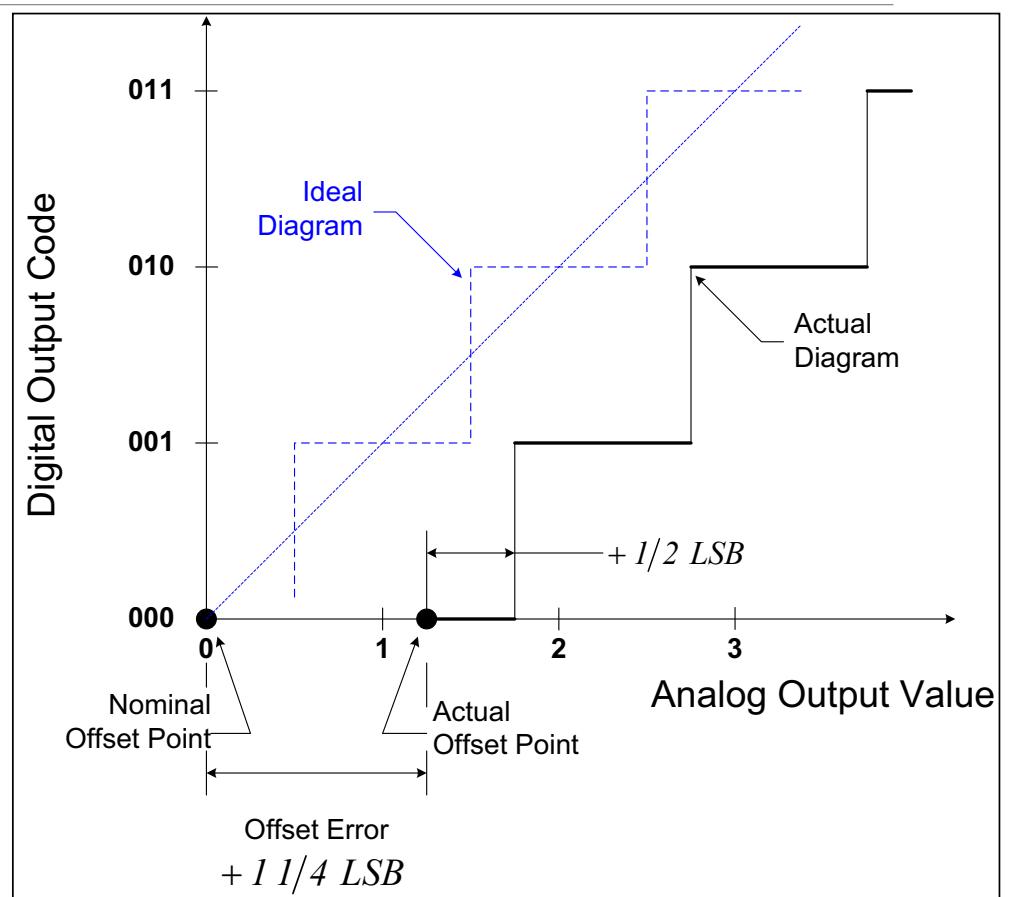
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- Quantization noise is unavoidable
  - Can be reduced increasing the ADC bit number  $N$  (ADC resolution)
- Further errors in **real** converters
  - offset error
  - gain error
  - integral nonlinearity (INL)
  - differential nonlinearity (DNL)
- Usually expressed in LSB units or as a percentage of the FSR (Full Scale Range). E.g.
  - INL = 1.2 LSB
  - INL = 1% FSR

May occur that all the thresholds are shifted, expressed as an offset in data sheet.

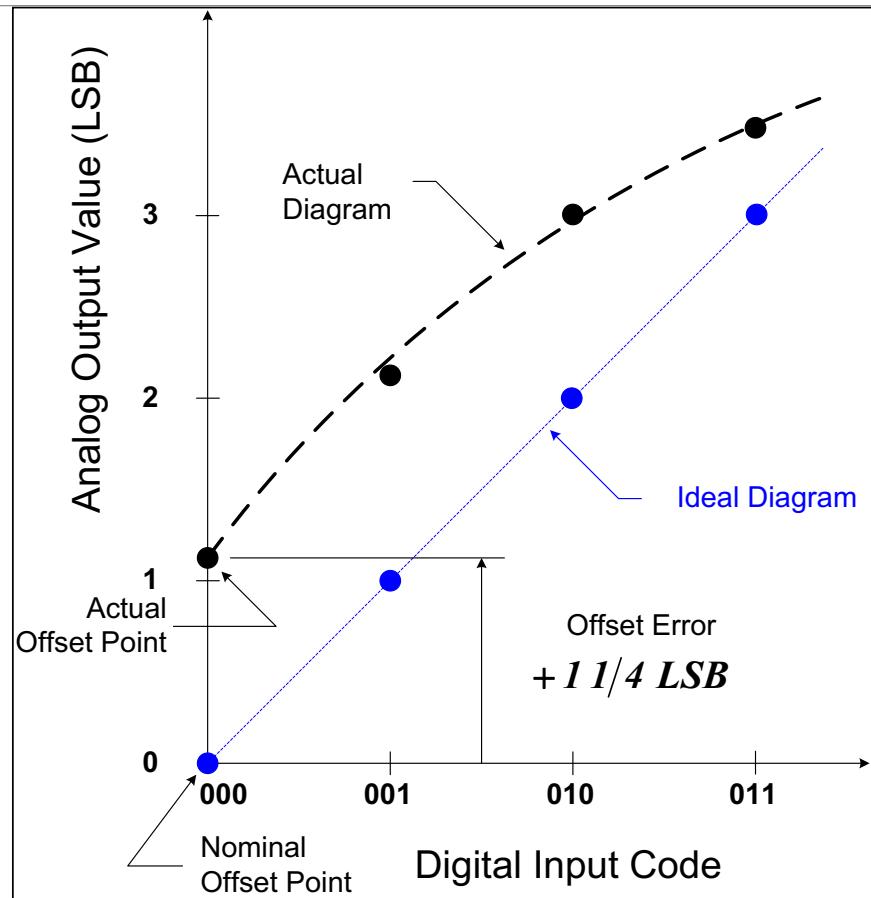
# ADC Offset Error

- The ideal stair is translated
- Difference between the nominal and actual offset points



# DAC Offset Error

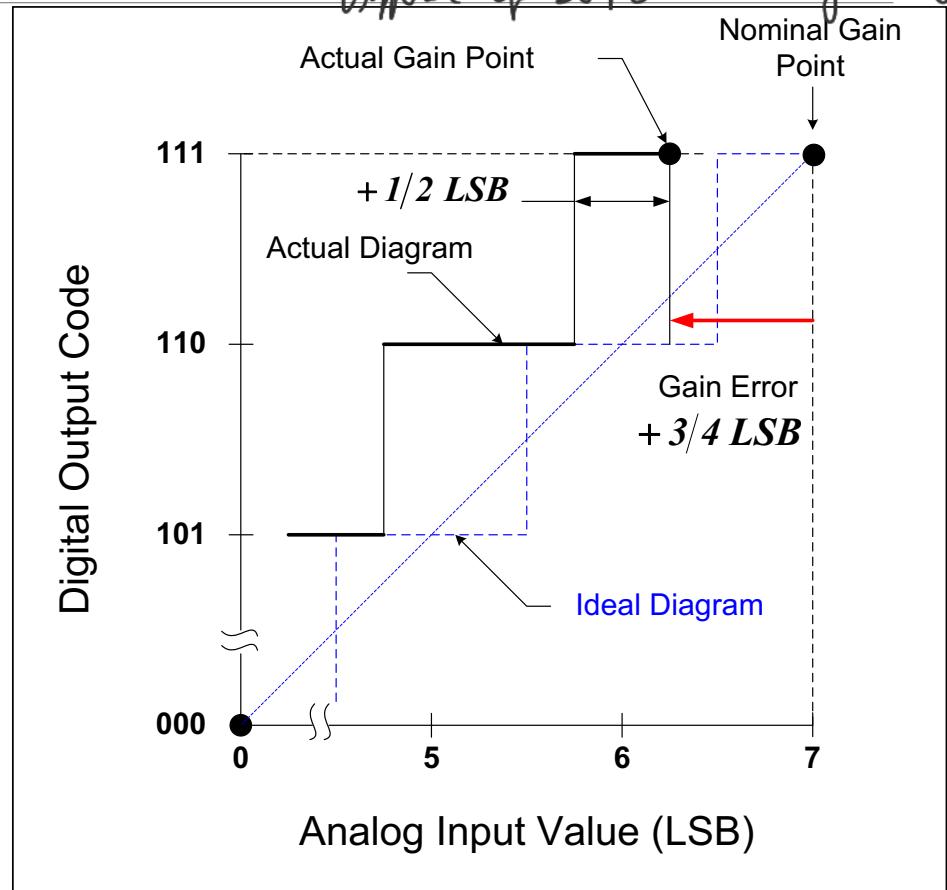
- The ideal curve is translated
- The offset error is the step value when the digital input is zero



# ADC Gain Error

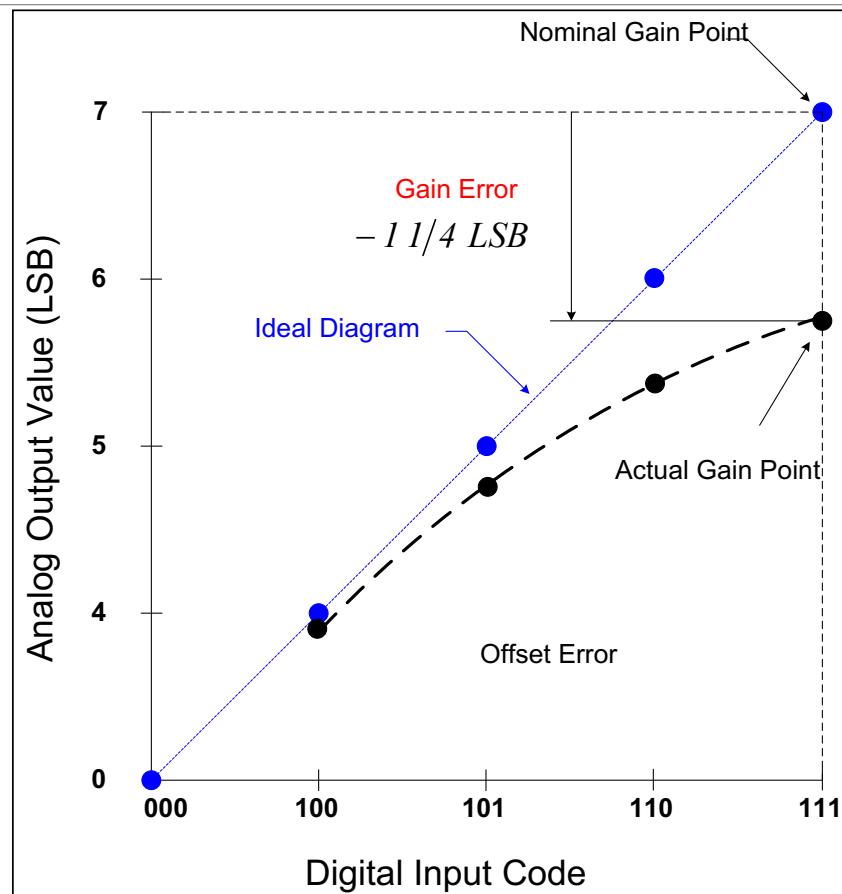
- Gain error is defined as the difference between the nominal and actual gain points after the offset error has been corrected to zero
- The gain point is the midstep value when the digital output is full scale

Gain error: Ideally you want a slope to be 1, but we be different. Difference of slope is called gain error.



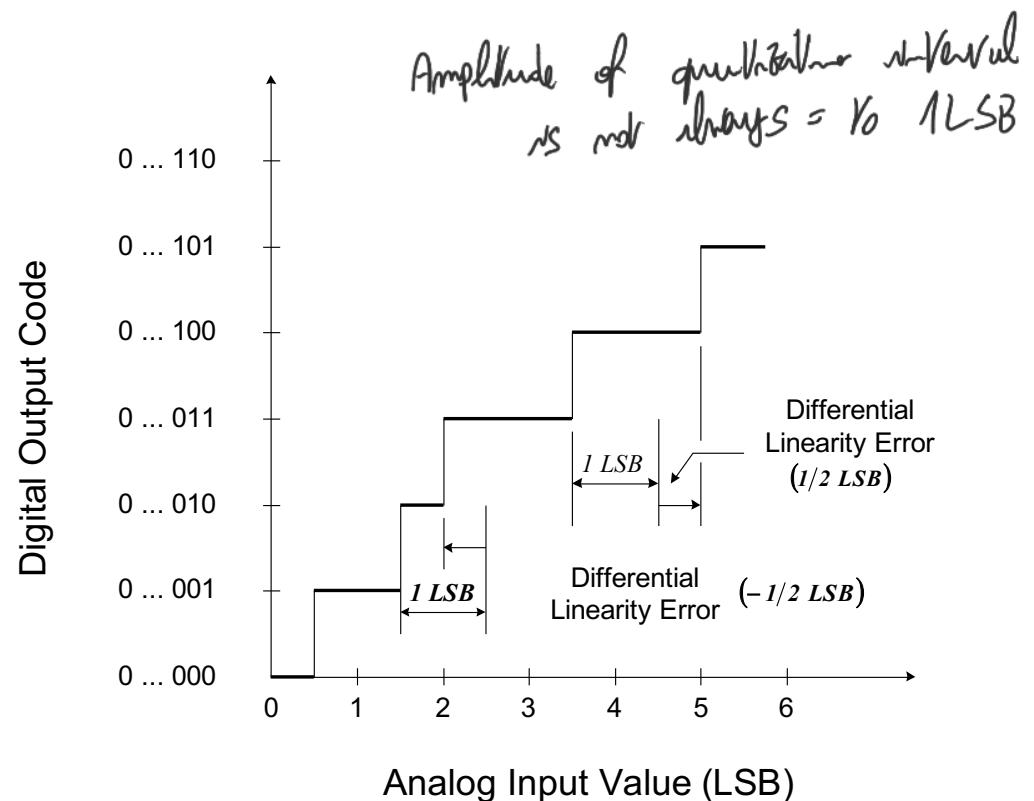
DAC Gain Error → you want a linear behaviour in converter, but you get something not linear.

- DAC Gain Error is the step value when the digital input is full scale
- It represents the difference in the slope of the actual and ideal transfer functions



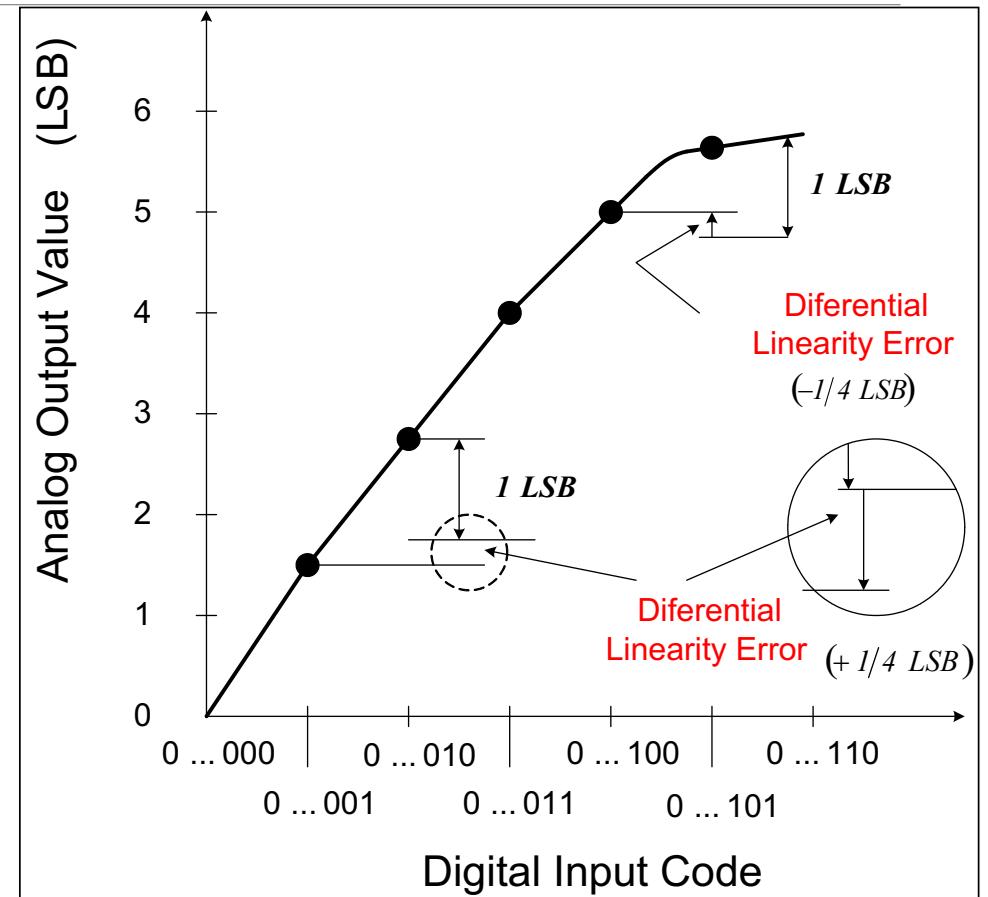
# ADC Differential Nonlinearity (DNL) Error

- DNL is the difference between an actual step width and the ideal value of 1 LSB
- DNL > +1 LSB
  - nonmonotonic (the magnitude of the output gets smaller for an increase in the magnitude of the input)
- DNL < -1 LSB
  - missing codes (one or more of the possible  $2^N$  binary codes are never output)



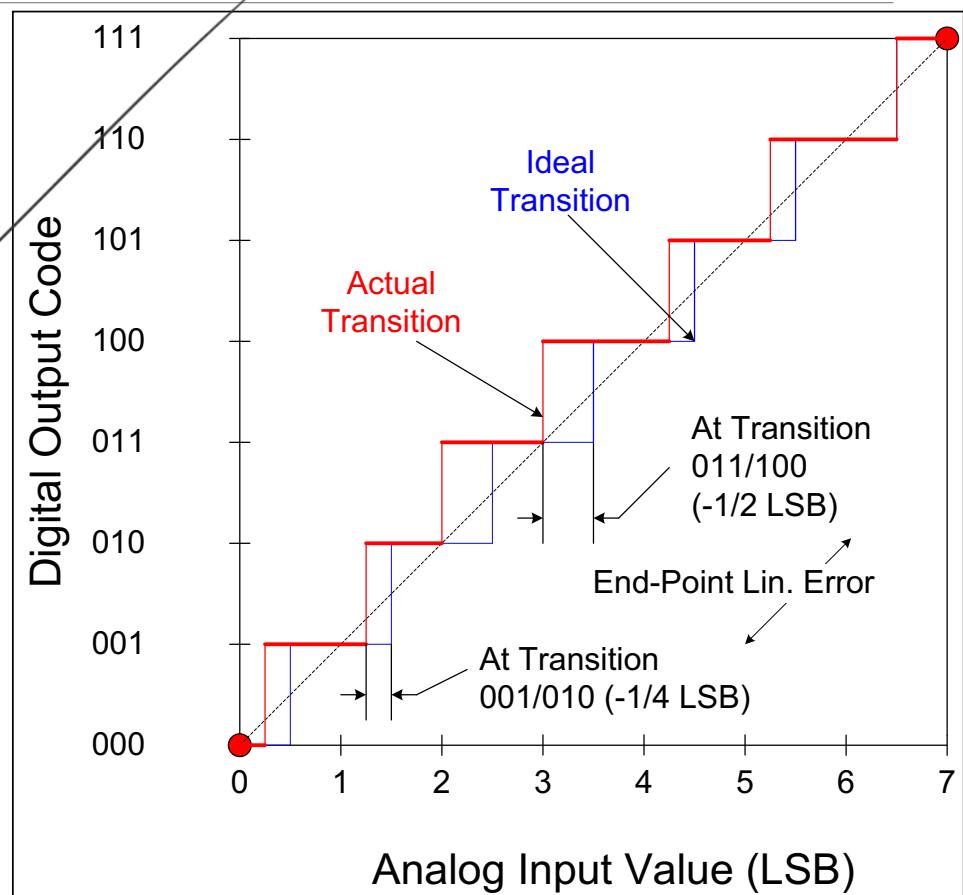
# DAC Differential Nonlinearity (DNL) Error

- DNL error is the difference between an actual step height and the ideal value of 1 LSB
- If the step height is exactly 1 LSB, the DNL error is zero

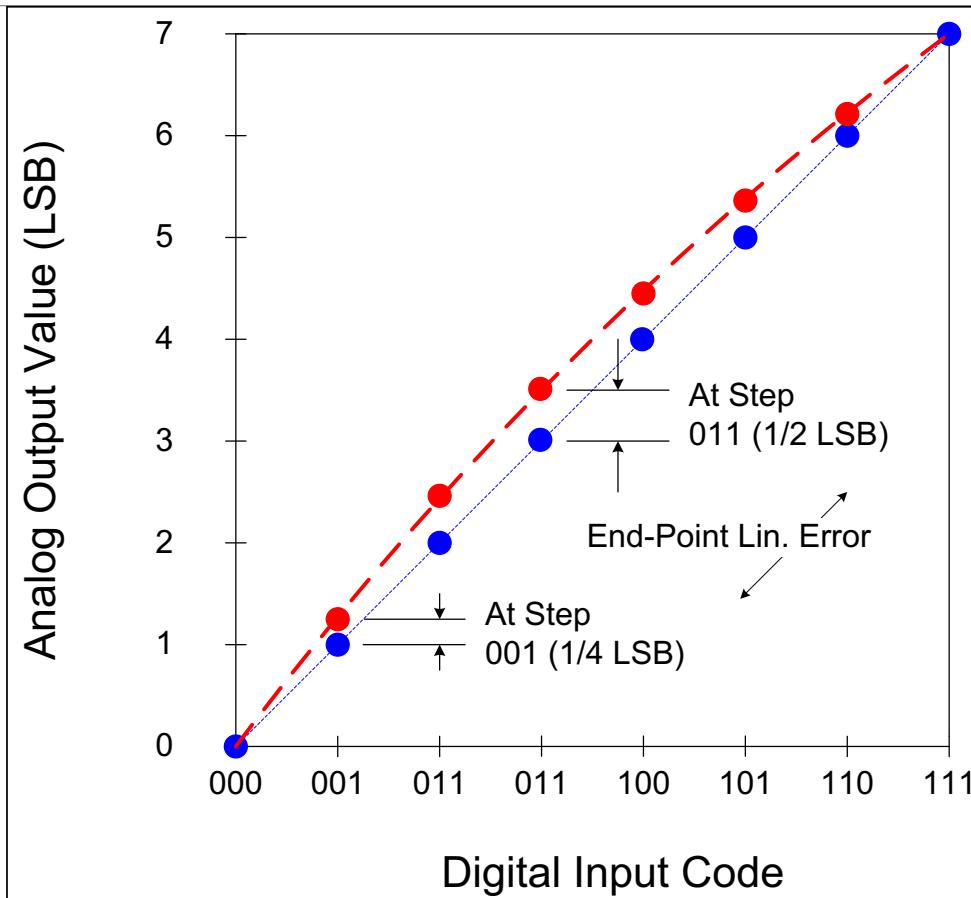


# ADC Integral Nonlinearity (INL) Error

- INL is the deviation of the values on the actual transfer function from a straight line
- This straight line can be
  - best straight line (drawn to minimize these deviations)
  - end points line (first and last points of the transfer function after gain and offset errors are cancelled)



# DAC Integral Nonlinearity (INL) Error



There are some errors, useful thing.  
Real conversion law differs from the real one. In practice |amplitude| of quantization error can be higher. This is unavoidable.

Various errors that happen in production process ( $1k\Omega$  resistors not actually  $1k\Omega$ ). Often expressed as gain, differential nonlinearity, offset, integral nonlinearity. They all reflect one original problem: real thresholds are a bit moved from the real positions. So you have problems. They all come from this

For DAC: offset is: input  $V_{DD}$  is 0 and you need 0.2 V. Or the points don't stay on a line, so gain error.

# Dynamic Range of ADCs

Dynamic Range is the ratio of the largest to the smallest possible signals that can be resolved. DO NOT confuse with Spurious Free Dynamic Range (SFDR).

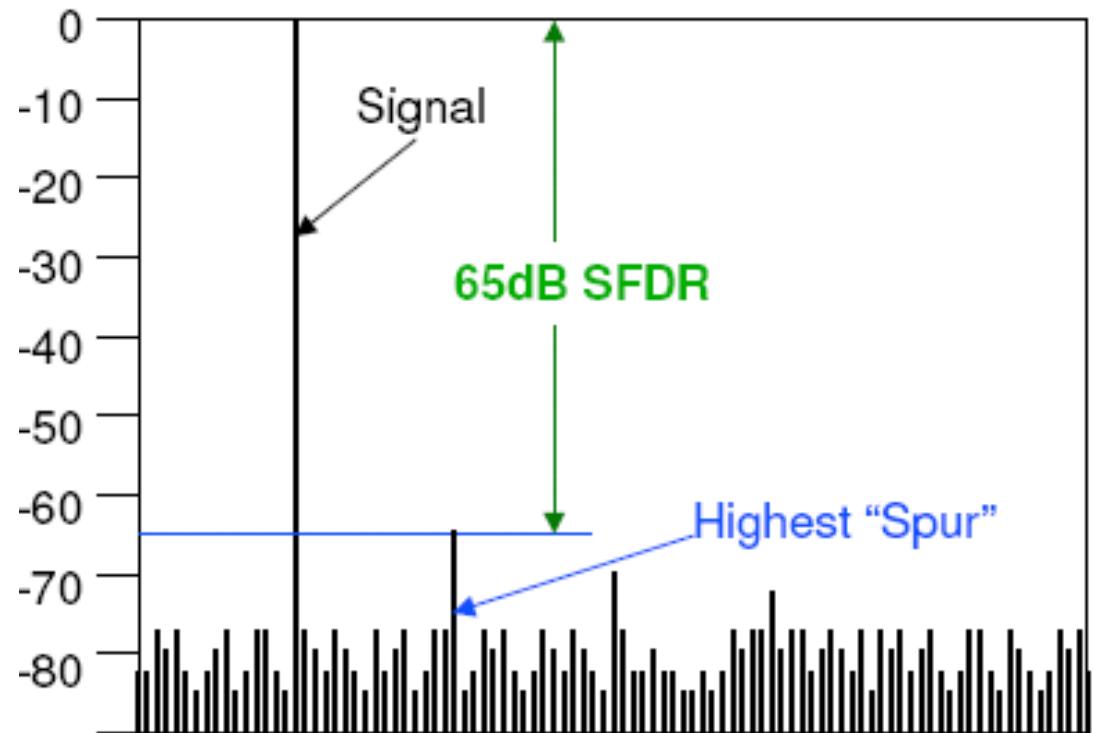
Resolution (Bits)	Dynamic Range (dB)
6	36.0
8	48.1
10	60.2
12	72.2
14	84.3
16	96.3
18	108.4
20	120.4

$$\text{Dynamic Range} = 20 * \log(2^n - 1)$$

$\uparrow$  max code expressed in dB.  
For power, which is squared  
 $\text{dB} = 10 \log_{10}(\text{Power})$

# Spurious Free Dynamic Range (SFDR)

- SFDR of an ADC is the ratio of the rms **signal amplitude** to the rms value of the **peak spurious spectral content** measured over the bandwidth of interest



# ADC Architectures

max sampling freq. and resolutions are the two parameters important.

SPEED  
↑  
↓ RESOLUT.

- Flash Converters : MAX CONV. SPEED and SAMP. FREQ. ↳ high speed converter, then small resolution.
- Successive Approximation ADCs MAX 8-12 bits Flash good for speed. Idea: all the bits of output obtained at the same time
- Pipelined ADCs (improved) ↑ SAR
- Integrating ADC

- Sigma-Delta ADC  
↓  
20-22-24 bits

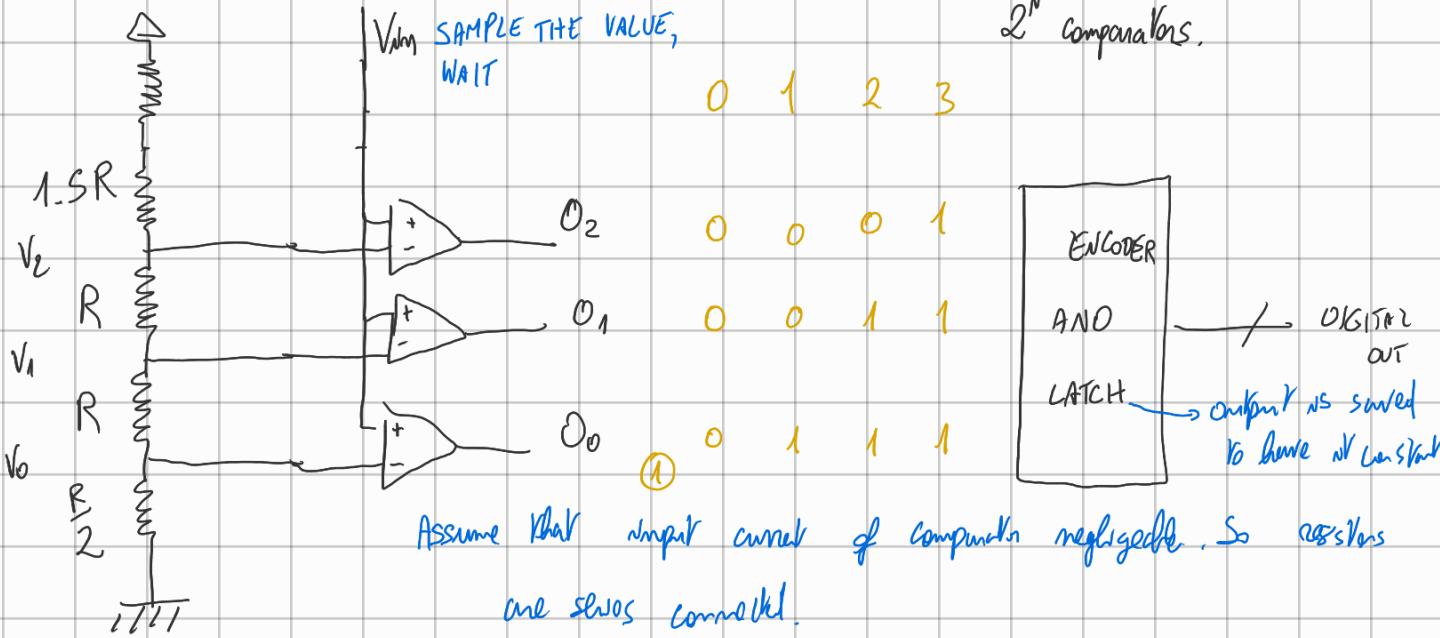
You need a # of clock cycles = to resolution to have result

Used in Audio Signal, very high resolution. Bandwidth useful not higher than 20 kHz.

↓ OPTIONAL ↓

How do you obtain all the thresholds? You have a voltage supply equal to  $V_{REF}$ .

How do you divide tension? You can use resistors; number of resistors = resolution



$$V_0 = \frac{R/2 \cdot V_{REF}}{4R} = \frac{V_{REF}}{8}$$

$$V_1 = \frac{3/2 R}{4R} V_{REF} = \frac{V_{REF}}{8} + \frac{V_{REF}}{4}$$

$$V_2 = \frac{5/2 R}{4R} V_{REF} = \frac{V_{REF}}{8} + 2 \cdot \frac{V_{REF}}{4}$$

VERY HIGH \*

Complexity: you have  $2^N$  comparators. Quite high. Comparators can be high speed. Apart from first and last resistor all resistors are equal.

Only problem in an unregulated circuit is having a resistor to have a certain value, having two resistors matched is a bit easier.

\* To get output code you need an encoder. The normal output is a thermometer.

①

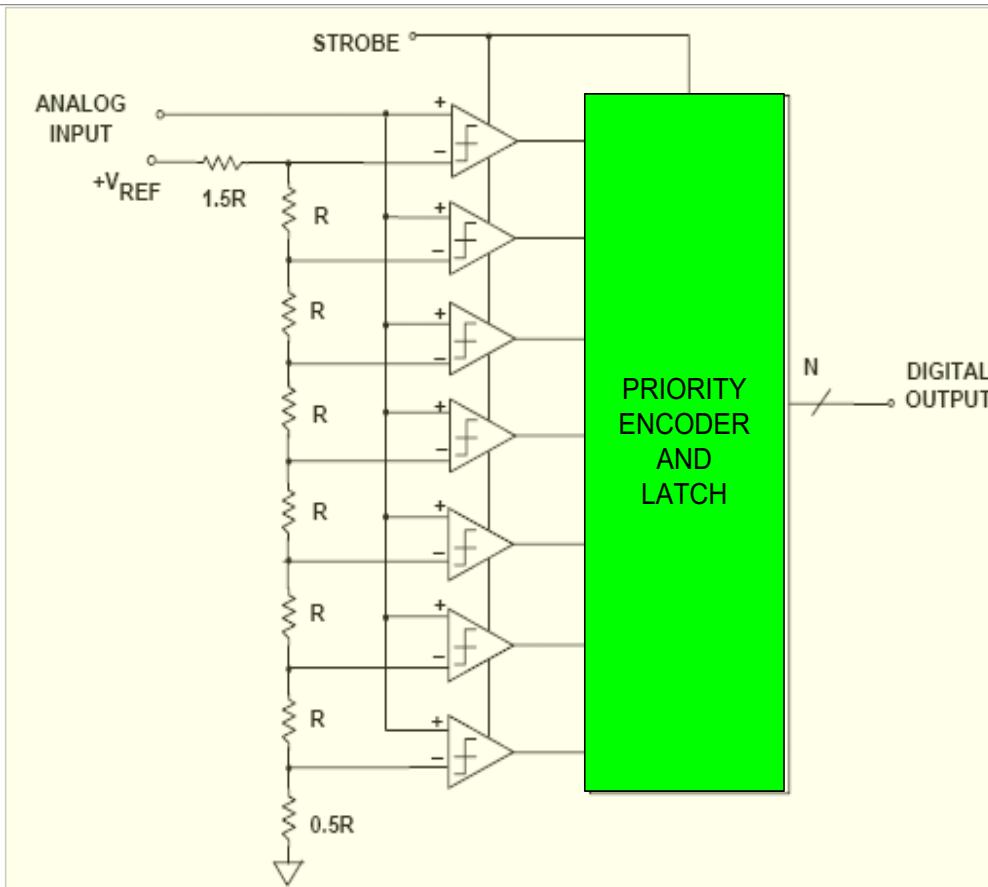
Sample value, wait for comparators to get stable, sample out at the same frequency of input.

# Flash Converter Features

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- Also known as parallel ADCs
- The fastest way to convert an analog signal to a digital signal
- Features
  - very large bandwidths
  - high power consumption
  - relatively low resolution
  - quite expensive
- An  $N$ -bit flash ADC consists of  $2^N$  resistors and  $2^N - 1$  comparators

# Flash Converter architecture



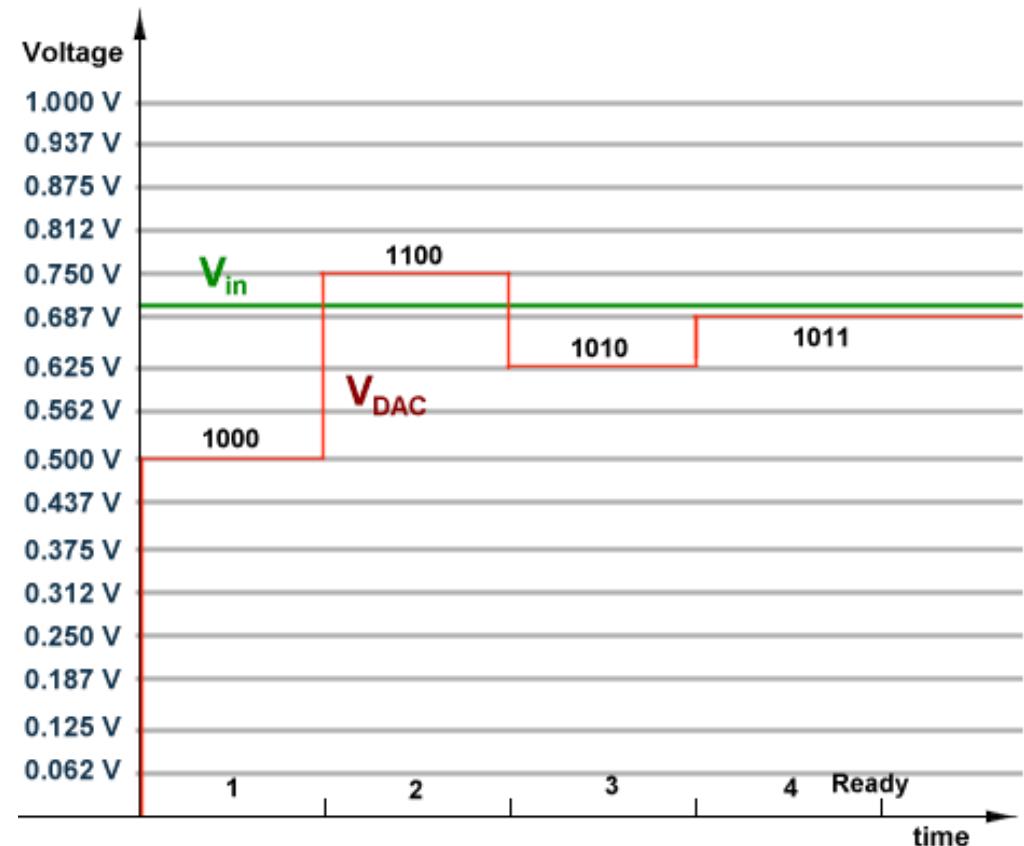
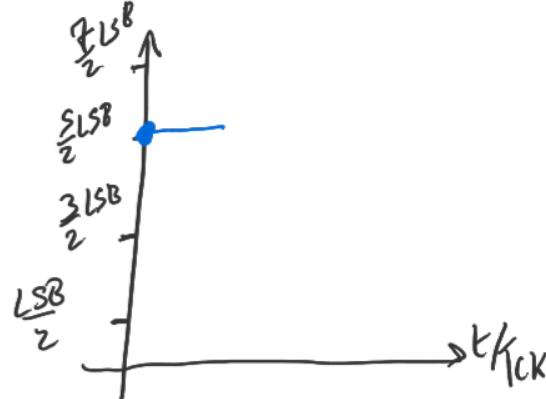
# Successive-Approximation ADCs (SAR)

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- The most popular architecture for data-acquisition applications
- Commercial SAR ADCs feature resolutions from 8 bits to 18 bits, with sampling rates up to several MHz
- Output data are generally provided via a standard serial interface ( $I^2C$  or SPI), but some devices are available with parallel outputs
- SAR ADCs are typically provided with a sample-and-hold (SHA) to keep the input signal constant during the conversion cycle

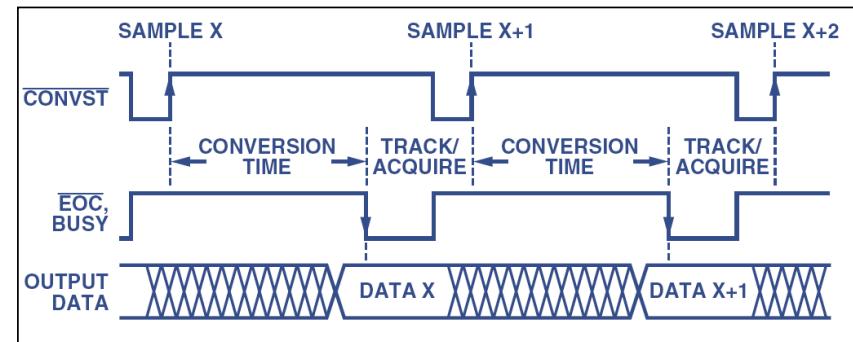
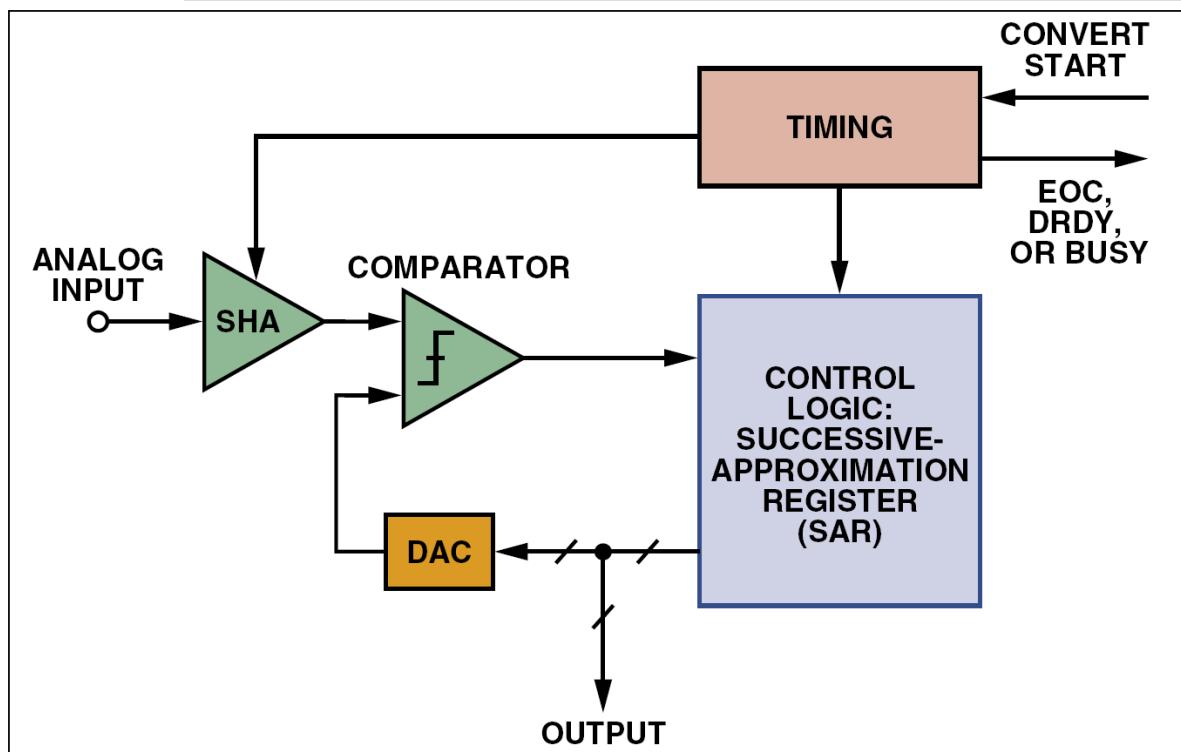
# Basic idea behind SAR ADC

- Input value is approached with approximation steps in which one bit per step is decided
- Conversion is final after  $N$  steps where  $N$  is the ADC bit resolution



1st we need to decide the MSB: So at the out of the DAC, we need the value at the half of the full scale: is  $V_{in} > \text{threshold set?}$  No, yes. Then you set the second bit of the DAC and redo a comparison. In N steps you get the right value.

## SAR Architecture



The overall accuracy and linearity of the SAR ADC are determined primarily by the internal DAC's characteristics

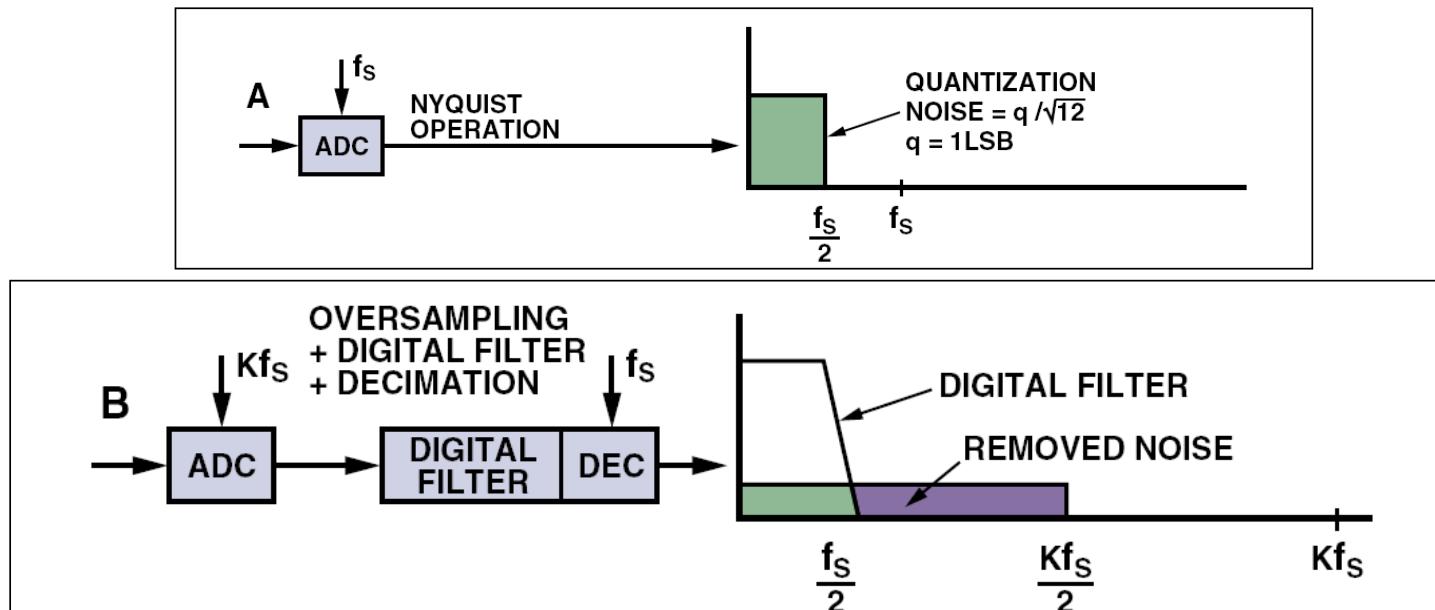
# SAR Operation Algorithm

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- Binary-tree-research alike conversion algorithm
- The internal D/A converter (DAC) is set to midscale
- The comparator determines whether the input is greater or less than the DAC output, and the result (the most-significant bit (MSB) of the conversion) is stored in the successive-approximation register (SAR) as a 1 or a 0
- The DAC is then set either to 1/4 scale or 3/4 scale (depending on the value of the MSB), and the comparator makes the decision for the second bit of the conversion
- The result (1 or 0) is stored in the register, and the process continues until all of the bit values have been determined

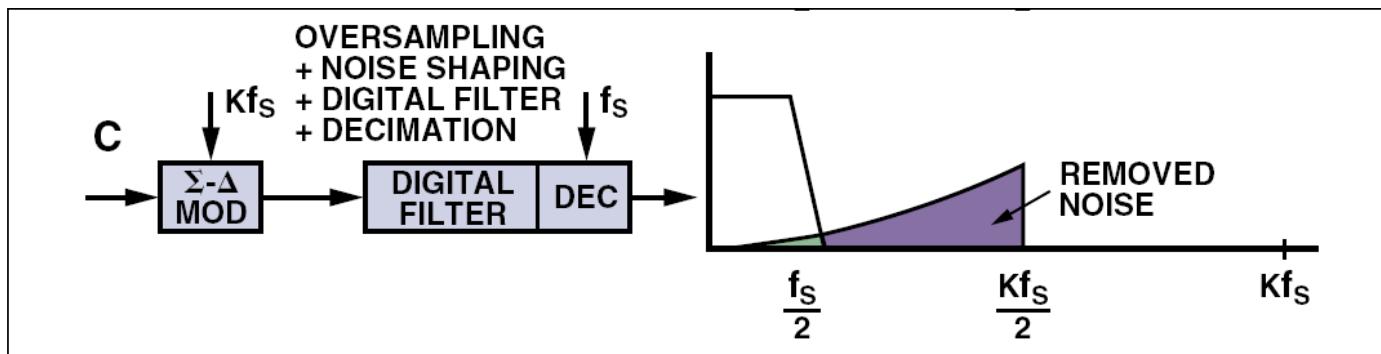
# Principle of oversampling

- Oversampling, digital filtering and decimation
- Quantization noise effect reduction
  - SNR between 0 and  $f_s/2$  increases by 3 dB for each doubling of  $K$



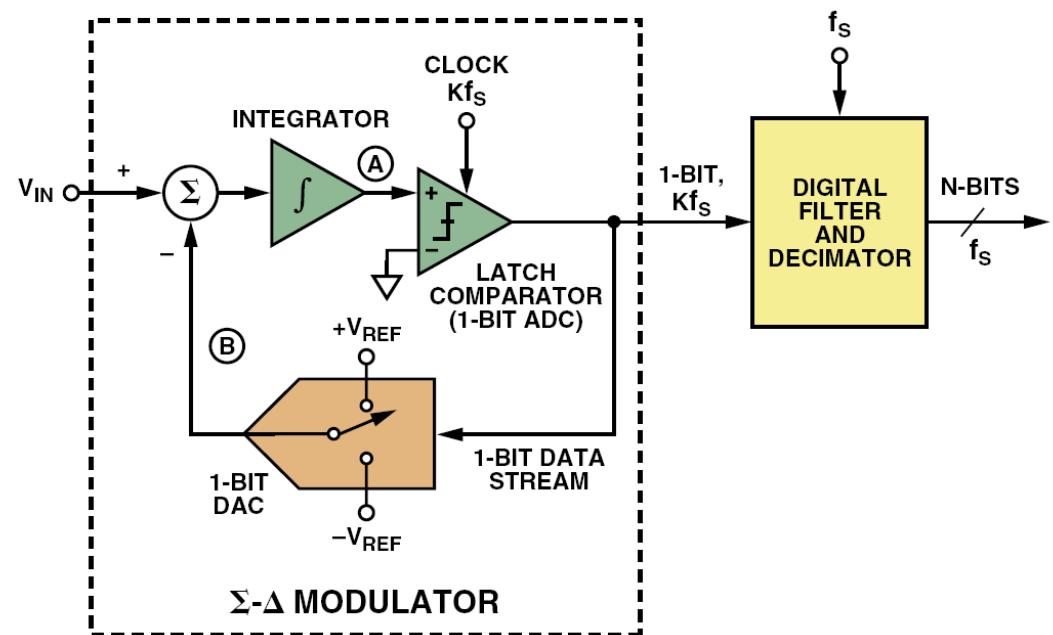
# $\Sigma$ - $\Delta$ ADC basic principles

- The traditional ADC is replaced by an oversampled  $\Sigma$ - $\Delta$  modulator
- The effect on noise is a shaping at high frequency
- Digital filtering further improves the SNR in the useful bandwidth



# $\Sigma$ - $\Delta$ ADC Architecture

- $\Sigma$ - $\Delta$  modulator consists of a 1-bit ADC and a 1-bit DAC closed in feedback
- The modulator output is a 1-bit stream of data
- Quantization noise is shaped towards high frequency



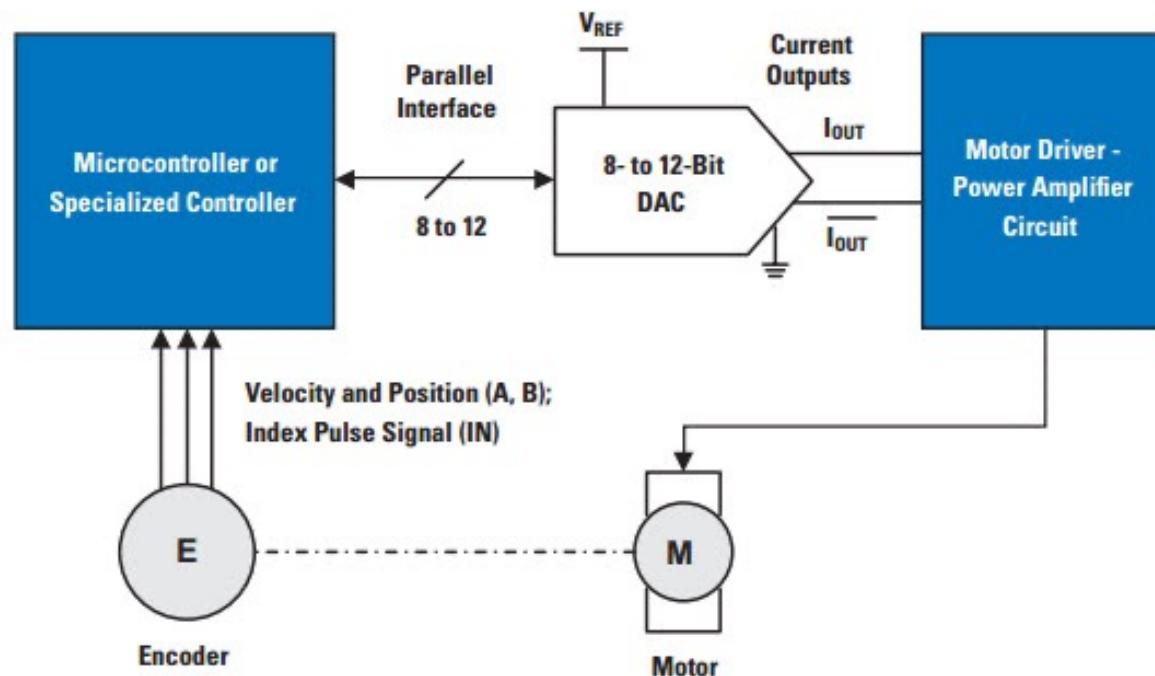
## $\Sigma\Delta$ ADC Pros and Cons

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- Noise shaping effect reduces noise in the signal bandwidth
  - Very simple 1-bit architecture
  - Most of computation is made on digital
- 
- Oversampling requires higher clock frequency
  - Filtering requires several clock cycles and a latency between input and output shows up

# Digital to Analog Converters (DACs)

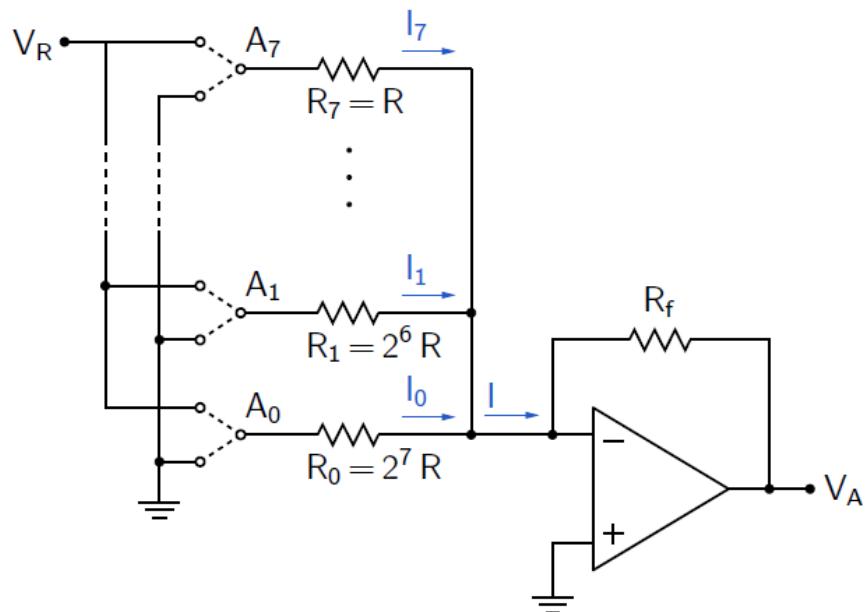
- Typical DAC application in motor control



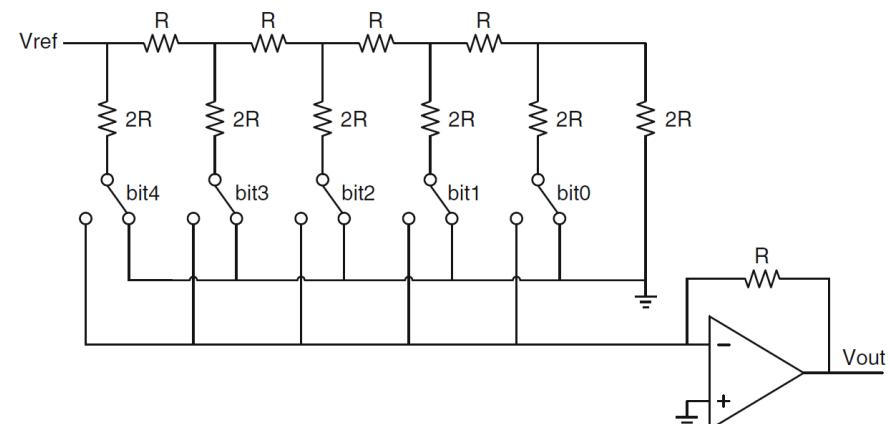
# DACs Architectures

2 different approaches for  
DACs.

## Binary weighted resistors



## R-2R ladder resistors



### FOR THE EXAM

To Remember: conversion law for ADC-DAC. Expressions of errors and discrepancy between ideal and real. Different approaches for ADC (flash, sigma delta etc).

Now serve two plane schemes of components