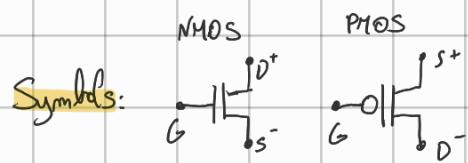


MOSFET TRANSISTOR (Metal Oxide Semiconductor)

2 types of mosfet transistor (nMOS, pMOS)



1 terminal: gate. Drain collects charges. Source provides charges.

NMOS: electrical conduction is obtained through electrons. Source is of electrons.

NOTE: the NMOS is symmetrical. The drain is the terminal with higher potential

$V_{DS} > 0$. With no external voltage we can't tell the difference.

The current between drain and source is holes. Source is source of positive charges. The source is the terminal with the higher potential.

CONCEPTS:

- In a semiconductor, there are two free (if we apply voltage they can move) carriers responsible for the electrical conduction, called electrons and holes. (holes are not real particles, but depending on the structure of the semiconductor we can have holes). When we apply an electrical field a free carrier acquires velocity (called drift proportional to the electrical field).

$$V_d = \mu E$$

magnitude of velocity
magnitude of the electrical field
mobility

NOTE: This linear equation applies if the magnitude of the electrical field is not too high ($\approx 10^5 \text{ V/cm}$)
We have mobility of electrons which can be different from the mobility of holes.

Let's call p and n the concentration of holes and electrons (# of holes and electrons per cm^3 or m^3)

- The concentration of free carriers at room temperature is much lower than the one in metals.
- The concentration depends exponentially from the temperature (high temperature, high concentration). This doesn't happen with metals. The resistivity in a metal increases over temperature.
- In an intrinsic (pure) semiconductor $n = p = N_{\text{intrinsic}}$

To do something interesting we need to have $n \neq p$. This is achieved with semiconductor doping.

This means that some silicon atoms are replaced with others called impurities.

Si is in the IV group of the periodic table, it has 4 valence electrons.

Impurities are taken by the 3rd and 5th group (Boron and Phosphorus). This is how we make $n \neq p$.

NOTE: It is sufficient to change only a little portion of the semiconductor (like one atom / 10^6).

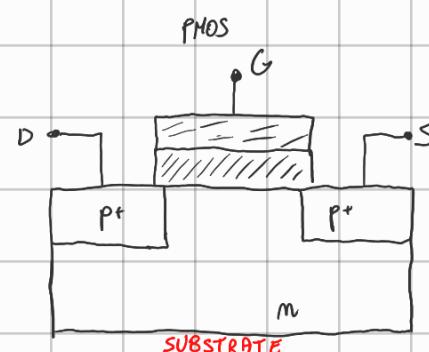
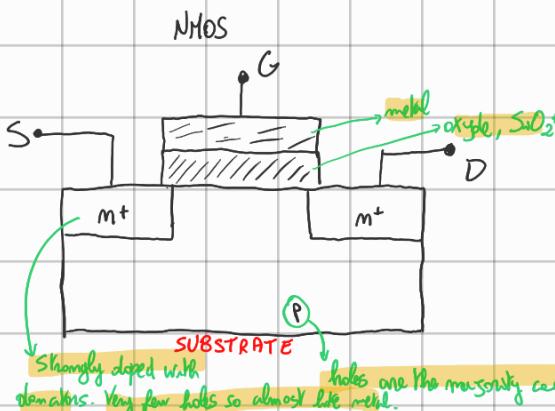
With Boron one bond is missing, we are increasing the concentration of holes (which are the majority carriers).

With Phosphorus there are a spare electrons, we are increasing the concentration of electrons.

If the impurity is from the 3rd group we call it acceptor otherwise donor.

5. What remains true in a doped semiconductor is that $n \cdot p = n_i^2$

CROSS SECTION OF THE 2 TRANSISTORS

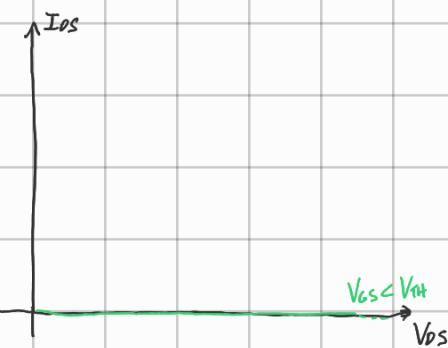


* Silicon has become widespread because it can give a powerful insulation as oxide.

NOTE: $I_G \approx 0$ because there is a good insulation.

We want to understand: $I_{DS} = I_{DS}(V_{GS}, V_{DS})$

So we apply a potential difference between D,S and G,S.



1. $V_{GS} = 0$: We have an electrons zone, holes zone and electrons zone. There is no path for electrons. We say there is no channel.

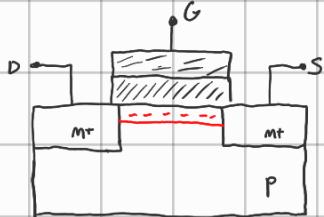
$\Rightarrow V_{GS} = 0, I_{DS} = 0 \forall V_{DS} \in \mathbb{R}$.

2. $V_{GS} > 0$: We have positive charges on the metal. $V_{GS} > 0$. The few electrons in the substrate are attracted to the gate. There is now a channel. We make a simplification.

The process is continuous but when $V_{GS} < V_{TH}, I_{DS} = 0$

[Invertible]

V_{th} is the value we need to apply to have below the gate a concentration equal to the holes in the substrate.

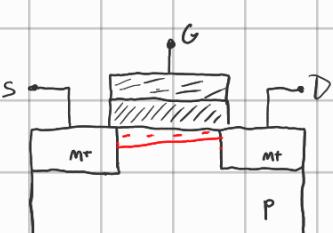


When we go over the V_{th} , initially the compact behaves almost like a resistor, but it saturates at a certain value.



Why do we saturate? $V_{GD} = V_{GS} + V_{SD} = V_{GS} - V_{DS}$

If $V_{SD} = 0$, $V_{GD} = V_{GS}$. When you increase V_{DS} , V_{GD} goes down. So on the drain side you start to have less electrons, and the thickness of the channel changes when approaching the drain. So the resistance of the channel changes with V_{DS} .

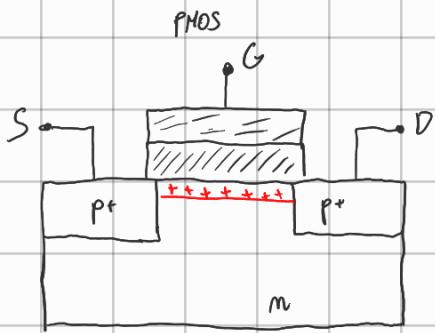
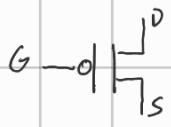


When the transistor is on, it behaves like a resistor, but the resistance depends from V_{DS} .

1. If $V_{GS} < V_{th}$, $I_{DS} \approx 0$

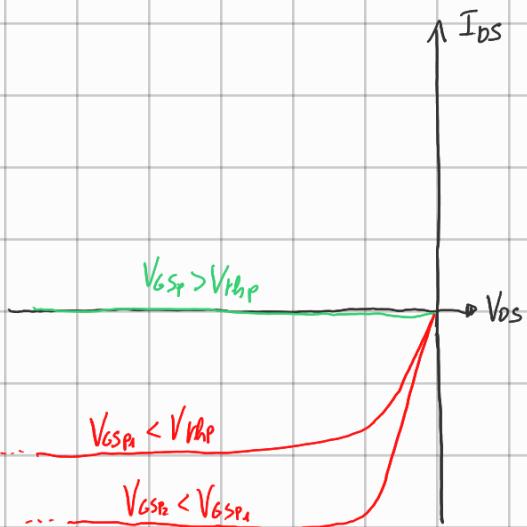
2. If $V_{GS} \geq V_{th}$, $I_{DS} > 0$ ON. Not ideal switch, we have a resistance that depends on V_{DS} .

pMOS:

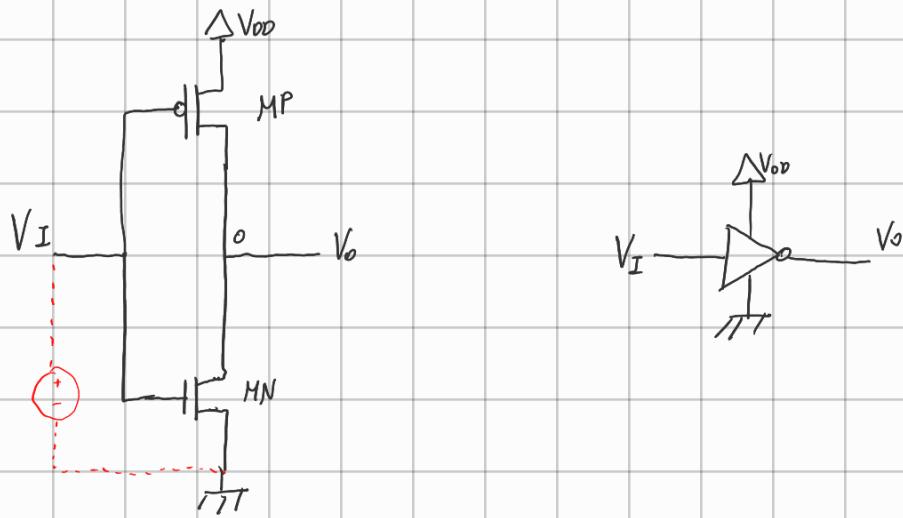


- If $V_{GS} = 0$, $I_{DS} \approx 0$
- If $V_{GS} \leq V_{thp}$, $I_{DS} < 0$ (holes go from source to drain with $V_{DS} < 0$)
 ↳ $V_{SG} \geq |V_{thp}|$, $I_{DS} > 0$ with $V_{SD} > 0$

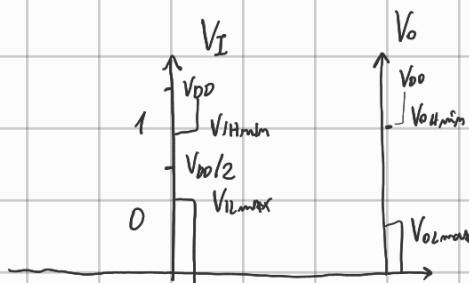
We need a channel of holes, a negative V_{GS}



INVERTER: This is a digital circuit but we have continuous values. What's the rule to say a voltage represents a 0 or a 1? [One node is pull at 0V potential as convention. Usually the negative terminal of the power supply]



When talking about the voltage of a mode is the potential difference between that mode and the 0 potential mode.



Ideally, all values over $V_{O,1/2}$ are 1, the others are 0. In reality though, you need a transition region.

So all values below $V_{I,Lmax}$ count as 0, all values above $V_{I,Hmin}$ count as 1.

To make things working, $V_{O,Hmin} > V_{I,Hmin}$, $V_{I,Lmax} > V_{O,Lmax}$.

$V_{O,Hmin} - V_{I,Hmin} = \text{Noise Margin High.}$

$V_{I,Lmax} - V_{O,Lmax} = \text{Noise Margin Low.}$ We want the output V_O to be closer to 0 or V_{DD} compared to the input ranges. Because you connect that output to be good as input for the following gates. The out has to be a valid logic value than the input. If you have noise that is below the noise margin everything works perfectly.