

CMOS INVERTERS (idea è connettere Scevo a punto a potenziale più basso per l'NMOS e viceversa. Se connetto terminali a massa chi NMOS, dovrà essere il source. Viceversa per il PMOS) [V_{cc} viene dalla logica TTL, V_{dd} perché prima il drain dell'NMOS era connesso a V_{dd}]



Dimostriamo che funziona come una NOT. Vogliamo disegnare "l'output characteristics", disegnare l'output in funzione dell'input (lo facciamo in maniera qualitativa)

$$\left. \begin{array}{l} V_{GSm} = V_I \\ V_{DSm} = V_O \end{array} \right\} M_m$$

$$\left. \begin{array}{l} V_{GSp} = V_I - V_{DD} \\ V_{DSP} = V_O - V_{DD} \end{array} \right\} M_p$$

Keep in mind:

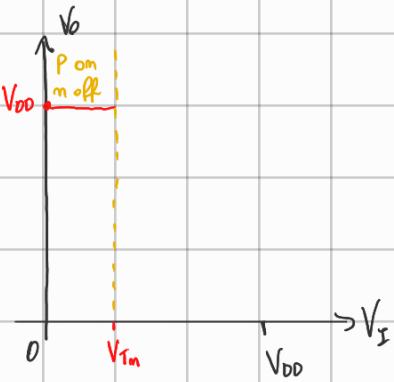


Reasoning: With low tension, the function is almost linear, slope representing the resistance, getting lower the higher the V_{GS} is. Modellabile by a Variable resistance (only with low V_{GS}).

NOTE: If the output is open: $I_{DSm} = -I_{DSP}$.

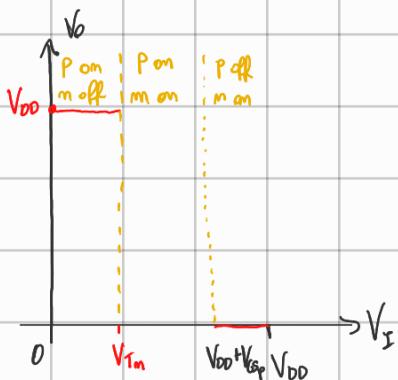
When $V_I = 0$, $V_{GSN} = 0$, so NMOS is off. Behaves like an open circuit. $V_{GSp} = -V_{DD}$ so PMOS is switched on. $V_{GSp} = -V_{DD} < V_{TP}$.

We know that $V_o = V_{GSp} + V_{DD}$. What's V_{GSp} ? Note that $I_{DSN} = 0$, so $\Rightarrow I_{DSp} = 0$, so (1), $V_{GSp} = 0$ on the p curve. So $V_o = V_{DD}$. So we have found one point of the output characteristics curve. NOTE: Until the NMOS is off, we can apply the same reasoning.



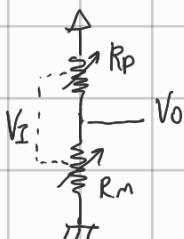
Now, $V_I = V_{DD}$. $V_{GSN} = V_I = V_{DD}$ and $V_{GSp} = V_I - V_{DD} = 0$. So NMOS is ON, PMOS is OFF. So $I_{DSN} = 0 \Rightarrow I_{DSp} = 0$. So for this reason $V_{DSN} = 0$ on the curve, so $V_o = V_{DSN} = 0$.

When PMOS is on, there is a path towards power supply, while NMOS creates a path towards 0. Until PMOS is off, nothing changes! Same as before. Until $V_{GSp} > V_{TP}$, $V_I - V_{DD} > V_{TP}$, $V_I > V_{DD} + V_{TP}$



In the middle both transistors are off but they have different resistances. Reasoning: When NMOS starts conducting, it is not conducting too well. The same applies for the PMOS, that is turning off though. When V_I is high, V_{GSN} is high and we stay on high curves. The PMOS has $V_{GSp} = V_I - V_{DD}$, so it is conducting not too well. And vice versa.

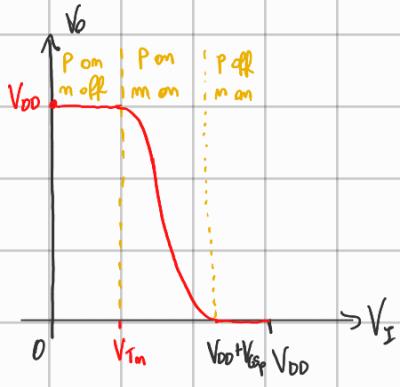
Basically:



$$V_o = \frac{V_{DD} R_m}{R_m + R_p}; \text{ With high } R_m \text{ we are on low } V_I \text{. When } R_m \text{ gets low, } R_p \text{ gets higher so } V_o \text{ is low. The two transistors are fighting.}$$

$$I = \frac{V_{DD}}{R_m + R_p} \quad V_o = \frac{R_m V_{DD}}{R_m + R_p}$$

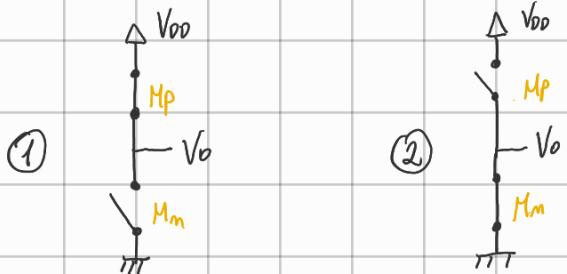
With high R_m we are on low V_I . When R_m gets low, R_p gets higher so V_o is low. The two transistors are fighting and a current is flowing into the circuit. Not good for power dissipation.



So now additional reasoning:

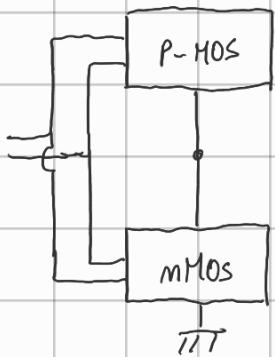
| V_I | M_n | M_p | V_o |
|----------|-------|-------|----------|
| 0 | OFF | ON | V_{DD} |
| V_{DD} | ON | OFF | 0 |

(1) (2)



CMOS NAND GATE

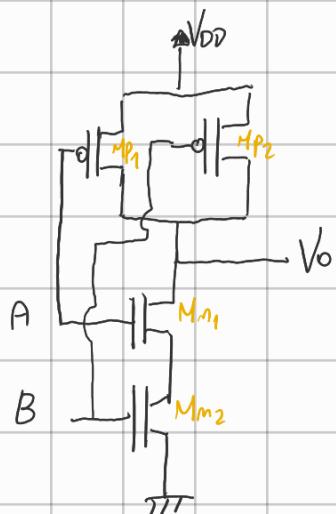
Note: pmos want to create a path towards the power supply, nmos to create a path toward the ground



Let's start with the nMOS: output is 0 only when both inputs are high \Rightarrow SERIES.

We need V_O to have 1 when we have at least 1 zero, so two PMOS in PARALLEL.

This is a general rule for logic functions: when n transistors appear in series they appear in parallel as pmos.



| V _A | V _B | M _{N1} | M _{N2} | M _{P1} | M _{P2} | V _O |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | OFF | OFF | ON | ON | V _{DD} |
| 0 | V _{DD} | OFF | ON | ON | OFF | V _{DD} |
| V _{DD} | 0 | ON | OFF | OFF | ON | V _{DD} |
| V _{DD} | V _{DD} | ON | ON | OFF | OFF | 0 |

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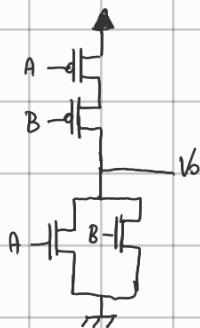
CMOS NOR



| A | B | OUT |
|---|---|-----|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

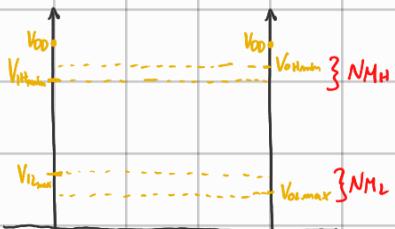
Only when both inputs are 0 we get a path to the power supply.

And we only need one 1 to have a path to the ground.



| V_A | V_B | M_{m_1} | M_{m_2} | M_{p_1} | M_{p_2} | V_0 |
|----------|----------|-----------|-----------|-----------|-----------|----------|
| 0 | 0 | OFF | OFF | ON | ON | V_{DD} |
| 0 | V_{DD} | OFF | ON | ON | OFF | 0 |
| V_{DD} | 0 | ON | OFF | OFF | ON | 0 |
| V_{DD} | V_{DD} | ON | ON | OFF | OFF | 0 |

How are the Noise Margins defined?



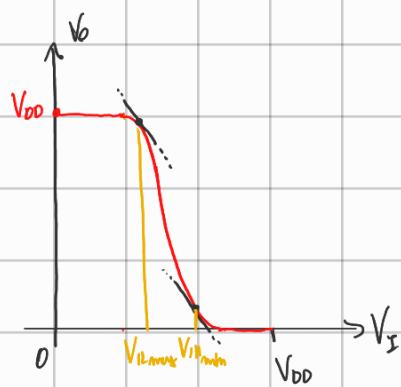
$NM_H, NM_L > 0$. Note it that if we have a disturbance

$V_{O_L} + \Delta < V_{I_L max}$, then the circuit works! The larger

NMs tell us the robustness of the circuit.

The output will either be $> V_{I_H min}$ or $< V_{I_L max}$

To find the noise margin, you take the output characteristic curve and look at when the derivative is 1.



Why? Because with a high slope, small variations in the input can cause huge variations in the output.