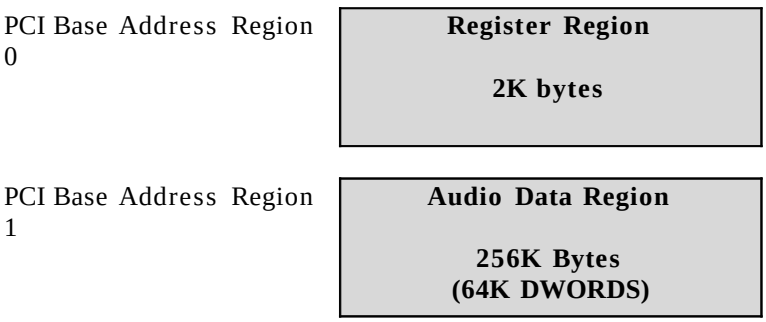
LynxTWO/L22 Interface Document

REVISIONS

DATE	WHO	DESCRIPTION
07/30/01	RJB	1. Added GSYNC bit to STRCTL reg 2. Added divide by 16 to PLLCTL reg 3. Added SYNCREADY mode to stream control regs 4. Added various model specific descriptions 5. Added LTC receive quarter frame interrupt flag to MSTAT reg 6. Added LTC receive quarter frame interrupt enable to LTC control reg
8/11/01	RJB	Added VPLLENn to MISC Control Register for new video PLL.
8/18/01	RJB	Changed SYNCREADY code to 11 in SCBLOCK
11/08/01	RJB	1. Added XferComplete bit to Stream Control Register. 2. Added GDIRMODE and GTESTDIR bits to DMACTL.
05/01/02	RJB	1. Changed record stream limit detection logic – see GLIMIT register description. 2. Renamed OPIOCTL to OPIOCTL 0 and added or changed various bits. 3. Added OPIOCTL 1 register and moved OPHSIG and OPHSIGDIR bits from OPIOCTL 0. 4. Changed description of OPCTL in PMIX Control Register 5. Added DMASingle and DMADualMono bits to Stream Control Register
06/06/02	RJB	1. Changed description of OPCTL and OPSTAT bits to reflect new LStream protocol.
06/12/02	RJB	1. Created OPBLOCK 2. Moved OPIOCTL regs to OPBLOCK 3. Added option port FIFO's, registers, and interrupt for LStream
06/18/02	RJB	1. Added LOCKED[1:0] to OPDEVSTAT and OPBUFSTAT registers 2. Reduced size of OP FIFO's to 63 3. Added upper 8 input channels of OP0 and OP1 as input sources in RMIX Control Register
05/15/03	RJB	1. Added ADCREV bit to PCICTL to control LRCK inversion for REV A AK5394 2. Removed OPBFCKDIR bit 5 in OPIOCTL 3. Changed OPHSIG bit 8 in OPIOCTL to OPHDUAL 4. Increased ADDR size from 6 bits to 7 bits in OPDEVCTL, OPDEVSTAT 5. Added LRSYNC status bit to OPBUFSTST for LRCK state detection 6. Added Big Endian flag to PDBLOCK, set for firmware supporting big endian systems, e.g., Macintosh computers.

Host Interface

The LynxTWO/L22 is PCI device that the host accesses through two address regions, the Register Region, the Audio Data Region, and a block of standard PCI configuration registers. The Register Region provides control and status register while Audio Data Region provides target access to the audio data buffers in dual-port RAM.



1 PCI Configuration Registers

The PCI configuration registers adhere to the PCI V2.1 specification and are accessed by the BIOS using PCI configuration read commands.

Important PCI configuration data stored in EEPROM:

Vendor ID: 1621h (Lynx vendor ID)
Device ID: 0020h (A Model device ID), 0021h (B Model device ID), 0022h (C Model device ID), 0023h (L22 device ID)

Auxiliary data specific to the LynxTWO/L22:

- Serial Number
- Revision
- Manufacture date

2 Register Region

Registers are accessed via target transfers to BAR0.

BYTE Offset	DWORD Offset	Register (32 bits)	R/W	Function
000 – 07F	00 – 1F	PDBLOCK (32 DWORDS)	R	Product Data Block
080 – 0FF	20 – 3F	FRBLOCK (32 DWORDS)	R	Frequency Counter Block
100	40	PCICTL	W	PCI bus control
104	41	DMACTL	W	Global DMA control
108	42	MISTAT	R	Misc. Interrupt status /reset
10C	43	AISTAT	R	Audio Interrupt status / reset
110	44	STRMCTL	W	Global stream control
114	45	PLLCTL	W	PLL Control
118	46	IOADDR	W	IOBLOCK Indirect Address
11C	47	IODATA	R/W	IOBLOCK Data
120	48	OPIOCTL	W	Option Port I/O control
124	49	OPDEVCTL	W	Option Port device control
128	50	OPDEVSTAT	R	Option Port device status
12C	51	OPBUFSTAT	R	Option Port FIFO status
200 – 2FF	80 – BF	SCBLOCK (64 DWORDS)	R/W	Stream Control Block
300 – 3FF	C0 – FF	TCBLOCK (64 DWORDS)	R/W	Time Code Block
400 – 7FF	100 – 1FF	MIXBLOCK (256 DWORDS)	R/W	Mix Control Block

2.1 PCICTL: PCI Bus Control (write only)

BIT	FUNCTION
0	GIE: PCI Bus interrupt enable – global
1	AIE: Audio interrupt enable
2	MIE: Miscellaneous interrupt enable for non- audio resources
3	LED: On- board LED enable
4	CNFDO: FPGA configuration EEPROM data out (to JTAG TDI)
5	CNFTMS: FPGA configuration EEPROM TMS (to JTAG TMS)
6	CNFCK: FPGA configuration EEPROM clock (to JTAG TCK)
7	CNFEN: FPGA configuration EEPROM write enable 1: EEPROM written from JTAG port 0: EEPROM written from FPGA (over PCI bus), used to update EEPROM
8	ADCREV: AK5394 revision, 0=REV NC, 1=REV A and above. Controls inversion of ADC LRCK. **Must be set for boards built with date code >= 0317.**

2.2 DMACTL: Global DMA Control Register (write only)

BIT	FUNCTION
0	GDMAEN: Global DMA enable. Enables the DMA controller.

21:1	GDBLADDR: DBL Host Address. Upper 21 bits of 2048 byte DMA buffer list.
22	GDIRMODE: Global DMA direction mode. 0=normal, 1=test mode
23	GTESTDIR: Global DMA transfer direction for test mode (see GDIRMODE bit). Controls direction of DMA transfers on all channels. Used with DMAHST to test on-board memory of each channel/stream. 0=PCI read, 1=PCI write.

2.3 MSTAT: Miscellaneous Interrupt Status / Reset Register (read only)

This register contains the state of miscellaneous interrupt flags. A high state indicates the corresponding resource is requesting an interrupt. ***All flags are reset when this register is read.***

BIT	FUNCTION
0	LRXAIF: LTC receive buffer A interrupt flag
1	LRXBIF: LTC receive buffer B interrupt flag
2	LTXAIF: LTC transmit buffer A interrupt flag
3	LTXBIF: LTC transmit buffer B interrupt flag
4	LRXQFIF: LTC receive quarter frame interrupt flag
5	OPSTATIF: Option port status received interrupt flag
6	RX8420: CS8420 interrupt flag. Clear 8420 interrupt assertion by reading CS8420 interrupt register.
7	CNFDI: FPGA configuration EEPROM data in (to JTAG TDO)
31:8	undefined

2.4 AISTAT: Audio Interrupt Status / Reset Register (read only)

This register contains the state of the audio interrupt flags. A high state indicates the corresponding resource is requesting an interrupt. ***All flags are reset when this register is read.***

BIT	FUNCTION
0	REC0AIF: Record stream 0 circular buffer interrupt flag
1	REC1AIF: Record stream 1 circular buffer interrupt flag
2	REC2AIF: Record stream 2 circular buffer interrupt flag
3	REC3AIF: Record stream 3 circular buffer interrupt flag
4	REC4AIF: Record stream 4 circular buffer interrupt flag
5	REC5AIF: Record stream 5 circular buffer interrupt flag
6	REC6AIF: Record stream 6 circular buffer interrupt flag
7	REC7AIF: Record stream 7 circular buffer interrupt flag
8	PLAY0AIF: Play stream 0 circular buffer interrupt flag
9	PLAY1AIF: Play stream 1 circular buffer interrupt flag
10	PLAY2AIF: Play stream 2 circular buffer interrupt flag
11	PLAY3AIF: Play stream 3 circular buffer interrupt flag
12	PLAY4AIF: Play stream 4 circular buffer interrupt flag
13	PLAY5AIF: Play stream 5 circular buffer interrupt flag
14	PLAY6AIF: Play stream 6 circular buffer interrupt flag
15	PLAY7AIF: Play stream 7 circular buffer interrupt flag
16	REC0DIF: Record stream 0 DMA buffer interrupt flag
17	REC1DIF: Record stream 1 DMA buffer interrupt flag
18	REC2DIF: Record stream 2 DMA buffer interrupt flag
19	REC3DIF: Record stream 3 DMA buffer interrupt flag
20	REC4DIF: Record stream 4 DMA buffer interrupt flag
21	REC5DIF: Record stream 5 DMA buffer interrupt flag
22	REC6DIF: Record stream 6 DMA buffer interrupt flag
23	REC7DIF: Record stream 7 DMA buffer interrupt flag
24	PLAY0DIF: Play stream 0 DMA buffer interrupt flag
25	PLAY1DIF: Play stream 1 DMA buffer interrupt flag
26	PLAY2DIF: Play stream 2 DMA buffer interrupt flag
27	PLAY3DIF: Play stream 3 DMA buffer interrupt flag
28	PLAY4DIF: Play stream 4 DMA buffer interrupt flag
29	PLAY5DIF: Play stream 5 DMA buffer interrupt flag
30	PLAY6DIF: Play stream 6 DMA buffer interrupt flag
31	PLAY7DIF: Play stream 7 DMA buffer interrupt flag

2.5 STRMCTL: Global Stream Control Register (write only)

BIT	FUNCTION
11:0	GLIMIT[11:0]: Global circular buffer limit size. Threshold for circular buffer interrupt generation. RECORD: Limit set when 0 < (PCPTR-L2PTR) < GLIMIT; where PCPTR-L2PTR indicates the number of empty DWORDS in circular buffer. ***NOTE:Record limit logic was changed on 4/29/02.*** PLAY: Limit set when (L2PTR-PCPTR) > GLIMIT; where L2PTR-PCPTR indicates the number of already played DWORDS in circular buffer.
12	GSYNC: Global sync start enable. Writing a one to this register generates a pulse that starts all streams in Sync Ready mode. There is not requirement to

	reset this bit when set.
31:13	undefined

2.6 PLLCTL: PLL Register (write only)

This register is used to control the sample rate generator.

BIT	FUNCTION			
10:0	M register – 11 bits, range: 2 - 2047			
11	M register bypass for M=1 setting			
22:12	N register – 11 bits, range: 2 - 2047			
24:23	P register – range 0 – 2 (0: divide by 2, 1:divide by 4, 2:divide by 8, 3:divide by 16)			
27:25	Reference clock source select bits:			
	b27	**b26**	**b25**	**Clock Source**
	0	0	0	Internal 32 MHz clock
	0	0	1	Digital input clock (use WORDALIGN always, DILRCKDIR must be set to zero for proper operation)
	0	1	0	External clock (from bracket input)
	0	1	1	Header clock (from internal header)
	1	0	0	Video Clock (24 MHz)
	1	0	1	Bracket Option Port Clock (OPBFCKDIR must be set to zero for proper operation)
	1	1	0	Header Option Port Clock (OPHFCKDIR must be set to zero for proper operation)
	1	1	1	not defined
28	WORDALIGN: Enables word clock phase alignment function			
30:29	SPEED: Controls clock signals for A/D and D/A converters. 00: Single speed, sample rates 11 – 50 kHz 01: Double speed, sample rates 50 – 100 kHz 10: Quad, speed, sample rates 100 – 200 kHz 11: undefined NOTE: In quad speed the number of streams processed by the onboard mixer is reduced by four.			
31	REV NC PCB - PLLPDn: PLL power down, active low. REV A and above - PLLPD: PLL power down, active high			

Sampling Rate = Fref *N / (M * 2^(P+1)) / 256; where Fref is the frequency of the selected clock source

2.7 IOADDR Register

Indirect address register used to access data registers in I/O Control Block

BIT	FUNCTION	R/W
7:0	ADDR[7:0] – IOBLOCK Address	W
8	RDWRn: IOBLOCK R/W indictor, 0= write, 1 = read	W
31:9	undefined	

2.8 IODATA Register

I/O Control Block data register provide access to register specified by IOADDR
NOTE: During writes to the IOBLOCK, IODATA must be written before IOADDR is written.

BIT	FUNCTION	R/W
7:0	DATA[7:0] – IOBLOCK Data	R/W
31:8	undefined	

2.9 OPIOCTL: Option Port (LStream) I/O Control Register (write only)

This register is used to control option port interface signals and routing

BIT	FUNCTION
0	OPHD1DIR: Header option port OPHD1 direction, 0 = output, 1 = input
1	OPHD2DIR: Header option port OPHD2 direction, 0 = output, 1 = input
2	OPHDINSEL: Header option port input data select, 0 = OPHD1, 1 = OPHD2
3	OPBBLKSEL: Selects the data sources for bracket option port output 0 = PMIX 8 –15 routed to bracket port channels 0 - 7, PMIX 0 – 7 routed to bracket port channels 8 – 15 1 = PMIX 0 – 7 routed to bracket port channels 0 - 7, PMIX 8 – 15 routed to bracket port channels 8 - 15
4	OPHBCKENn: Header option port bit clock output enable, 0 = enabled, 1 = hi- z
5	Unused
6	OPHFCKDIR: Header option port frame clock direction, 0 = output, 1 = input
7	OPHBLKSEL: Selects the data sources for header option port output 0 = PMIX 8 –15 routed to header port channels 0 - 7, PMIX 0 – 7 routed to header port channels 8 – 15 1 = PMIX 0 – 7 routed to header port channels 0 - 7, PMIX 8 – 15 routed to header port channels 8 - 15
8	OPHDUAL: Enables header port dual LStream mode. Routes bracket port data to second LStream (AUX) channel on header port. NOTES: 1. OPHFCK pin is used as AUX LStream input in dual mode; OPHFCKDIR must be set to 1. 2. OPHSIG pin is used as AUX LStream output in dual mode; OPHSIGDIR must be set to 0.
9	OPHSIGDIR: Header option port OPHSIG direction, 0 = output, 1 = input.

10	OPSTATIE: Option port status interrupt enable. Enables interrupt generation when status data from either option port is available in status FIFO. An interrupt is generated when the FIFO becomes not empty or full.
11	OPCTLRST: Option port device control FIFO reset. Resets FIFO pointers to an empty state. Writing a "1" to this bit position generates a single reset pulse. Clear is not required.
12	OPSTATRST: Option port device status FIFO reset. Resets FIFO pointers to an empty state. Writing a "1" to this bit position generates a single reset pulse. Clear is not required.

Option Port (LStream) Channel Count

The number of active option port (LStream) channels varies with speed mode as follows

SPEED	Number of LStream Channels
1X	16
2X	8
4X	4

2.10 OPDEVCTL: Option Port (LStream) Device Control Register (write only)

This register is used to send control data to an LStream device connected to either option port. Data written to this register is stored in a 63- word FIFO prior to transmission. Bits in the OPBUFSTATor OPDEVSTAT register indicate the state of this FIFO**. In order to avoid lost control data, do not write to this register when the option port is not locked. Use the LOCKED[1:0] bits in OPBUFSTAT to determine this condition.**

Each LStream device has unique control data structure described its LStream Device Map. Refer to this document for details.

BIT	FUNCTION
7:0	DATA[7:0]: Device control data
14:8	ADDR[6:0]: Device control register address
15	PORT: Indicates target option port. 0 = bracket port (LStream 1), 1 = header option port (LStream 2)
31:16	unused

2.11 OPDEVSTAT: Option Port (LStream) Device Status Register (read only)

This register contains status data received from an LStream device connected to either option port. Data is stored in a 63- word FIFO. ***Each read of this register decrements the FIFO's data pointer***. Status bits in this register indicate the state of this FIFO **AFTER** the data is read during a read of this register. The OPBUFSTAT can be queried to determine the current state of the FIFO without decrementing the FIFO's pointers.

An interrupt to indicate the arrival of status data is available and can be enabled in the OPIOCTL register.

Each LStream device has unique status data structure described its LStream Device Map. Refer to this document for details.

BIT	FUNCTION
7:0	DATA[7:0]: Device status data
14:8	ADDR[6:0]: Device status register address
15	PORT: Indicates target option port. 0 = bracket port (LStream 1), 1 = header option port (LStream 2)
16	STAT_EMPTY: Option port status FIFO empty flag
17	STAT_FULL: Option port status FIFO full flag
18	CTL_EMPTY: Option port control FIFO empty flag
19	CTL_FULL: Option port control FIFO full flag
20	LOCKED0: Option port 0 (bracket) input locked flag
21	LOCKED1: Option port 1 (header) input locked flag
31:22	unused

2.12 OPBUFSTAT: Option Port (LStream) Buffer Status Register (read only)

This register status bits that indicate the state of the option port device control and status FIFO's. These bits are also available in OPDEVSTAT for convenience**.** ***Reading this register has no effect on FIFO pointers***.

BIT	FUNCTION
15:0	unused (actually contains same bits as OPDEVSTAT)
16	STAT_EMPTY: Option port status FIFO empty flag
17	STAT_FULL: Option port status FIFO full flag
18	CTL_EMPTY: Option port control FIFO empty flag
19	CTL_FULL: Option port control FIFO full flag
20	LOCKED0: Option port 0 (bracket) input locked flag
21	LOCKED1: Option port 1 (header) input locked flag
22	LRSYNC: LRCK state
31:23	unused

2.13 SCBLOCK: Stream Control Block (read/write)

BYTE Offset	DWORD Offset	Register (32 bits)
000 - 01F	00 - 07	Record 0 – Record 7 Stream Control
020 -	08 - 0F	Play 0 – Play 7 Stream Control

03F		
040 - 05F	10 – 17	Record 0 – Record 7 Stream Status
060 – 07F	18 - 1F	Play 0 – Play 7 Stream Status

2.13.1 Stream Control Registers. Each stream has one of these.

BIT	FUNCTION	R/W
11:0	PCPTR: Host circular buffer pointer *NOTES:* 1) During DMA transfers the DMA controller maintains a copy of PCPTR used for addressing the circular buffer and does not update PCPTR until completion of a DMA transfer. 2) During host transfers the host must update PCPTR *after* data is read or written to the stream's circular buffer. 3) The host must reset PCPTR prior to placing the stream into run mode. This is a requirement for both DMA and host transfers. 4) If DMAEN is low, DMA engine will not write to this register 5) If DMAEN is high, host must not write to this register	R/W
13:12	MODE[1:0]: Mode control, 00 = IDLE, 01 = RUN, 10 = reserved , 11 = SYNCREADY	R/W
15:14	FMT[1:0]: Format control, 00 = PCM8, 01 = PCM16, 10 = PCM24, 11 = PCM32	R/W
16	CHNUM: Channel Number control, 0 = mono, 1 = stereo	R/W
17	LIMIE: Limit Interrupt Enable. Enables interrupt generation when circular buffer limit is hit.	R/W
18	OVERIE: Overrun Interrupt Enable. Enables interrupt generation for circular buffer overrun/underrun. (CB pointer wrap condition)	R/W
19	XFERCMP: Transfer complete flag. Set during target mode transfer to inform IOP that data has been transferred to/from CB. IOP will generate a limit interrupt in response if a limit condition exists. Non-functional during DMA transfers.	W
20	DMAEN: Stream DMA enable	R/W
21	DMAHST: DMA host start. Initiates one DMA transfer. Used to pre-load circular buffer prior to playback. Transfer will complete when either the CB is full/empty or the host data buffer is empty/full. Upon completion the DMA controller will reset this bit, providing status to host. The host must not write to this bit when it is set.	R/W
25:22	DMABINX: DMA buffer index. Indicates the index of the host buffer currently being accessed by the DMA controller for this stream. The index is reset when DMAEN is low.	R
26	DMAMODE: Indicates the DMA state for this stream. Acts as an acknowledgment of the DMAEN bit.	R
27	DMASTARV: Indicates that the host buffers are empty (play) or full (record) and the DMA controller needs to transfer more data. The host must add more buffers to the DBL for this stream. This starve condition is reevaluated by the DMA controller each DMA controller cycle (once ever sample period min.). During a host start, DMASTARV is reset one DMA cycle after a host started transfer is complete.	R

28	DMASingle: Limits DMA controller to transferring one host buffer when a stream limit condition is detected. This bit is used for low-latency drivers such as ASIO. NOTE: DMASTARV bit will not be set with DMASingle asserted until the DMA controller detects a zero length host buffer descriptor.	R/W
29	DMADualMono: Enables DMA transfers from two adjacent host buffers to left and right positions in the CB. Allows full utilization of 16 output channels when drivers, such as ASIO, utilize synchronized mono channel buffers. For proper operation this bit can be set only if the following requirements are met: 1. FMT = PCM32 2. CHNUM = 1 (stereo) 3. Left and right host buffer lengths are identical and a maximum of 1000h bytes (1024 DWORDS) 4. Right buffer start 1000h bytes after left in host memory 5. Left host buffer resides on a 2000h byte address boundary 6. Left and right host buffer data is transferred synchronously 7. Amount of data in left and right host buffers must never be more than required to completely fill/deplete CB. Typically DMASingle is set for record devices and play devices are run in starved mode. 8. HBUFPTR descriptor in DMA buffer list must point to start of left host buffer. 9. HBUFLEN descriptor in DMA buffer list must be set to the combined length of left and right host buffer in DWORDS.	R/W

2.13.2 Stream Status Registers. Each stream has one of these.

BIT	FUNCTION	R/W
11:0	L2PTR: LynxTWO (hardware) controlled circular buffer pointer	R
13:12	BYTECNT[1:0]: Indicates which byte in current DWORD is being accessed by the IOP	R
14	MODE: 0 = IDLE, 1 = RUN. Indicates the actual state of the stream	R
15	LIMHIT: Circular buffer limit hit flag	R
16	OVER: Circular buffer overrun flag	R

2.14 TCBLOCK: Time Code Block (read/write)

BYTE Offset	DWORD Offset	Register (16 bits)	R/W
000 - 00F	00 - 03	LTC Receive Buffer A	R
010 - 01F	04 – 07	LTC Receive Buffer B	R
020 – 02F	08 – 0B	LTC Transmit Buffer A	W
030 – 03F	0C – 0F	LTC Transmit Buffer B	W
040 - 04F	10 - 13	VITC Receive Buffer 1A	R
050 – 05F	14 – 17	VITC Receive Buffer 1B	R
060 – 06F	18 – 1B	VITC Receive Buffer 2A	R
070 – 07F	1C – 1F	VITC Receive Buffer 2B	R
080	20	LTC Control Register	W
084	21	VITC Control Register	W
088	22	Time Code Status Register	R
08C	23	LTC Receive Frame Rate	R

2.14.1 Time Code Buffers

Time code receive and transmit buffers contain LTC or VITC address data organized in to four 16-bit words. Each word is resides in the lower 16-bits of a 32-bit register in which the upper 16 bits are unused.

	BIT										
LTC WORD	**31:16**	**15:12**	**11**	**10**	**9**	**8**	**7:4**	**3**	**2**	**1**	**0**
0	unused	binary group 2	color frame	drop frame	frame tens		binary group 1	frame units			
1	unused	binary group 4	phase corr (LTC)	seconds tens			binary group 3	seconds units			
			field mark (VITC)								

2	unused	binary group 6	bg flag 55	minutes tens		binary group 5	minutes units
3	unused	binary group 8	bg flag 75	unused	hours tens	binary group 7	hours units

2.14.2 LTC Control Register

BIT	FUNCTION
0	LRXEN: LTC receive enable. Enables LTC receive processor
1	LRXIE: LTC receive interrupt enable. An interrupt is generated when a complete address is received. LTC Receive Buffers A and B generate separate interrupt flags in an alternating pattern. **This bit must be changed only when LRXEN is low.**
2	LTXEN: LTC transmit enable. Enables LTC transmit processor
3	LTXIE: LTC transmit interrupt enable. An interrupt is generated when a complete address is transmitted. LTC Transmit Buffers A and B generate separate interrupt flags in an alternating pattern. **This bit must be changed only when LTXEN is low.**
4	LTXCLK: LTC transmit clock source select 0 = Internal 32 MHz clock 1= LTC receive clock (load 1 into divider for divide by 2) – *this bit is not currently implemented* **This bit must be changed only when LTXEN is low.**
6:5	LTXSYNC[1:0]: LTC transmit sync source 0 = free running, transmit starts when LTXEN is high 1 = video input line 5 2 = LTC receive sync pattern detect 3 = register write NOTE: LTXEN must be low when LTXSYNC is changed to avoid LTC transmission errors **This bit must be changed only when LTXEN is low.**
8:7	LTXRATE[1:0]: LTC transmit frame rate 0 = 24 fps 1 = 25 fps 2 = 29.97 fps 3 = 30 fps NOTE: If LTXCLK is 1 the transmit frame will track the LTC receive frame rate **This bit must be changed only when LTXEN is low.**
9	LRXQFIE: LTC receive quarter frame interrupt enable

2.14.3 VITC Control Register

NOTE: This register and all VITC functions are not implemented

BIT	FUNCTION
0	VRXEN: VITC receive enable. Enables VITC receive processor
1	VRXIE: VITC receive interrupt enable. An interrupt is generated when a complete address is received. VITC Receive Buffers A and B generate separate interrupt flags in an alternating pattern.
6:2	VRXLINE1[4:0]: VITC read line 1. The read line is equal to the contents +10. A value of 1F will enable line searching.
11:7	VRXLINE2[4:0]: VITC read line 2. The read line is equal to the contents +10. A value of 1F will enable line searching.

2.14.4 Time Code Status Register

BIT	FUNCTION
0	LRXLOCK: LTC receiver lock indicator. Asserted when a valid forward or backward sync pattern is detected. Deasserted when sync pattern is not found (after 16 bit periods or time out)
1	LRXDIR: LTC receive direction. 1 = forward 0 = backward
2	VRXLOCK: VITC receiver lock indicator. Asserted when a valid forward or backward sync pattern is detected
3	VRXFIELD: VITC receiver field 0 = even 1 = odd
4	VRXFRAME: VITC receiver frame (PAL only) ??
5	VRXLOCK1: VITC receiver read line 1 lock indicator. Asserted a valid VITC address has been received on the line specified by VRXLINE1.
6	VRXLOCK2: VITC receiver read line 2 lock indicator. Asserted a valid VITC address has been received on the line specified by VRXLINE2.

2.14.5 LTC Receive Frame Rate

BIT	FUNCTION
15:0	LRXCOUNT: Count value indicates actual frequency of received LTC. RATE = 50000 / (LRXCOUNT +1) frames/second

2.15 FRBLOCK: Frequency Counter Block (read only)

This block contains a frequency measurement data for various LynxTWO system clocks.

BYTE Offset	DWORD Offset	Register
000	00	Left/right Clock COUNT
004	01	Left/right SCALE

008	02	Digital Input Clock COUNT (DILRCKDIR must be set to zero for proper operation)
00C	03	Digital Input Clock SCALE
010	04	External Clock COUNT
014	05	External Clock SCALE
018	06	Header Clock COUNT
01C	07	Header Clock SCALE
020	08	Video Clock COUNT (HSYNC rate: 15.734 kHz NTSC or 15.625 kHz PAL)
024	09	Video Clock SCALE
028	0A	Bracket Option Port Input Clock COUNT (OPBFCKDIR must be set to zero for proper operation)
02C	0B	Bracket Option Port Input Clock SCALE
030	0C	Header Option Port Input Clock COUNT (OPHFCKDIR must be set to zero for proper operation)
034	0D	Header Option Port Input Clock SCALE
038	0E	PCI Clock COUNT
03C	0F	PCI Clock SCALE

2.15.1 COUNT Register

BIT	FUNCTION
15:0	COUNT[15:0] Number of 32MHz cycles counted during measurement period
31:16	undefined

2.15.2 SCALE Register

BIT	FUNCTION
3:0	SCALE[3:0] Scale factor, range 0 – 9
4	NTSCPALn: Video input format status 0 = PAL, 1 = NTSC This bit is replicated in all SCALE registers.
31:5	undefined

Clock Frequency = (32E6 * $2^{(SCALE+2)}$) / COUNT

BOB: Add notes regarding limits on significant digits displayed for each scale.

2.16 PDBLOCK: Product Data Block (read only)

BYTE Offset	DWORD Offset	Register Contents		
		b31:16	b15:8	b7:0

000	00	undefined	“LY” (4C59h)		
004	01	undefined	“NX” (4E58h)		
008	02	undefined	Device ID = 0020h, 0021h, 0022h		
00C	03	undefined	PCB Rev		
010	04	undefined	BE*	Firmware ID	Firmware Rev
014	05	undefined	Firmware Date		
018	06	undefined	Minimum Software API Build		
01C	07	undefined	SPARE		
020	08	undefined	USER0		
024	09	undefined	USER1		
028	0A	undefined	USER2		
02C	0B	undefined	USER3		
030	0C	undefined	USER4		
034	0D	undefined	USER5		
038	0E	undefined	USER6		
03C	0F	undefined	USER7		

*BE = Big Endian flag, bit 15: set for firmware supporting big endian systems, e.g., Macintosh computers

REVISION CODES: 0=none, 1=A, 2=B,…

DATE ENCODING: yyyymmmm000ddddd;

yyyyy = year – 2000

ddddd = day (1-31)

mmmm = month (Jan=1, Feb=2, Mar=3…)

2.17 IOBLOCK: I/O Control Block (read/write)

Address	Register

(written to IOADDR)	(8 bits)
00 - 7F	CS8420 Control/Status Block (128 bytes, serially-controlled)
80 - 83	DAC A Control (serially-controlled) – All Models
84 - 87	DAC B Control (serially-controlled) - A and B Models
88 – 8B	DAC C Control (serially-controlled) - B Model
90	ADC A Control (pin-controlled) – All Models
91	ADC B Control (pin-controlled) – A and C Models
92	TRIM: Analog Trim Control (pin-controlled)
93	MISC: Miscellaneous Control (pin-controlled)
95	ADC C Control (pin-controlled) - C Model

2.17.1 CS8420 Control/Status Registers

-------- *Insert table of 128 bytes here from CS8420 data sheet*

Refer to the CS8420 data sheet for a complete description.

*2.17.2 DAC A Control Registers (CS4396) – **ALL MODELS***

Controls D/A Converter for LINE OUT 1 and LINE OUT 2.

Mode Control Register @ byte address 81h

BIT	FUNCTION	R/W
0	PDN: Power Down – must be low for normal operation	R/W
5:1	MODE[4:0]: Mode Select – controls operation including digital interface format, de-emphasis filter, clocking configuration (see below for details)	R/W
6	MUTEn: Soft Mute – active low. Causes the analog outputs to ramp to a muted state.	R/W
7	CAL: Enables calibration to minimize differential DC offset. NOTE: This is not a pulse width timing requirement for this signal	R/W

MODE Select Bits:

Mode	MODE[4:0]
Single Speed / No De-emphasis	01101
Single Speed / 32 kHz De-emphasis	00001
Single Speed / 44.1 kHz De-emphasis	00101
Single Speed /48 kHz De-emphasis	01001
Double Speed	11101
Quad Speed	11001

*2.17.3 DAC B Control Registers (CS4396) – **MODEL A AND B ONLY***

Controls D/A Converter for LINE OUT 3 and LINE OUT 4

Mode Control Register @ byte address 85h

BIT	FUNCTION	R/W
0	PDN: Power Down – must be low for normal operation	R/W
5:1	MODE[4:0]: Mode Select – controls operation including digital interface format, de-emphasis filter, clocking configuration (see data sheet for details)	R/W
6	MUTEn: Soft Mute – active low. Causes the analog outputs to ramp to a muted state.	R/W
7	CAL: Enables calibration to minimize differential DC offset.	R/W

Refer to section 3.13.2 for a description of the Mode Select bits.

*2.17.4 DAC C Control Registers (CS4396) – **MODEL B ONLY***

Controls D/A Converter for LINE OUT 3 and LINE OUT 4

Mode Control Register @ byte address 89h

BIT	FUNCTION	R/W
0	PDN: Power Down – must be low for normal operation	R/W
5:1	MODE[4:0]: Mode Select – controls operation including digital interface format, de-emphasis filter, clocking configuration (see data sheet for details)	R/W
6	MUTEn: Soft Mute – active low. Causes the analog outputs to ramp to a muted state.	R/W
7	CAL: Enables calibration to minimize differential DC offset.	R/W

Refer to section 3.13.2 for a description of the Mode Select bits.

*2.17.5 ADC A Control Registers (AK5394) – **ALL MODELS***

Controls A/D converter for LINE IN 1 and LINE IN 2

Control Register 1 @ byte address 90h

BIT	FUNCTION	R/W
0	RSTn: Reset, active low	W
1	ZCAL: Zero calibration control. NOTE: This signal is global to all ADC's in FPGA FW Build 14 and above.	W
3:2	DFS[1:0]: Output Sample Rate Select 00= single speed, 01 = double speed, 10 = quad speed NOTE: This signal is global to all ADC's in FPGA FW Build 14 and above	W
4	HPFE: High-pass Filter Enable	W
7:5	Not Defined	W

2.17.6 ADC B Control Registers (AK5394) **– MODEL A and C ONLY**

Controls A/D converter for LINE IN 3 and LINE IN 4

Control Register 1 @ byte address 91h

BIT	FUNCTION	R/W
0	RSTn: Reset, active low	W
1	ZCAL: Zero calibration control NOTE: This signal is not used in FPGA FW Build 14 and above. Refer to ADC A Control register description.	W
3:2	DFS[1:0]: Output Sample Rate Select 00= single speed, 01 = double speed, 10 = quad speed NOTE: This signal is not used in FPGA FW Build 14 and above. Refer to ADC A Control register description.	W
4	HPFE: High-pass Filter Enable	W
7:5	Not Defined	W

*2.17.7 ADC C Control Registers (AK5394) – **MODEL C ONLY***

Controls A/D converter for LINE IN 3 and LINE IN 4

Control Register 1 @ byte address 95h

BIT	FUNCTION	R/W
0	RSTn: Reset, active low	W
1	ZCAL: Zero calibration control NOTE: This signal is not used in FPGA FW Build 14 and above. Refer to ADC A Control register description.	W
3:2	DFS[1:0]: Output Sample Rate Select 00= single speed, 01 = double speed, 10 = quad speed NOTE: This signal is not used in FPGA FW Build 14 and above. Refer to ADC A Control register description.	W
4	HPFE: High-pass Filter Enable	W
7:5	Not Defined	W

2.17.8 TRIM Control Register - Controls analog I/O trim.

@ byte address 92h

BIT	FUNCTION	R/W
0	**All Models:** TRIMIN12: Analog Input 1 and 2 trim control, 1 = +4 dBu, 0 = -10 dBV	W
1	**A and C Models:** TRIMIN34: Analog Input 3 and 4 trim control, 1 = +4 dBu, 0 = -10 dBV **B Model:** TRIMOUT56: Analog Output 5 and 6 trim control, 1 = +4 dBu, 0 = -10 dBV	W
2	**A and B Models:** TRIMOUT12: Analog Output 1 and 2 trim control, 1 = +4 dBu, 0 = -10 dBV **C Model:** TRIMIN56: Analog Input 5 and 6 trim control, 1 = +4 dBu, 0 = -10 dBV	W

3	**A and B Models:** TRIMOUT34: Analog Output 3 and 4 trim control, 1 = +4 dBu, 0 = -10 dBV **C Model:** TRIMOUT12: Analog Output 1 and 2 trim control, 1 = +4 dBu, 0 = -10 dBV	W
4	SPARE0: spare output	W
5	SPARE1: spare output	W
6	SPARE2: spare output	W
7	SPARE3: spare output	W

2.17.9 MISC Control Register

Miscellaneous controls

@ byte address 93h

BIT	FUNCTION	R/W
0	PDNDACCn: DAC C power down, active low – B MODEL ONLY	W
1	DIOFMT: Digital input/output electrical format, 0 = AES/EBU, 1 = S/PDIF	W
2	PDNDACAn: DAC A power down, active low	W
3	PDNDACBn: DAC B power down, active low	W
4	CS8420RSTn: CS8420 reset, active low	W
5	DILRCKDIR: Digital in LRCK direction 1: input, supports slaving to LRCK decoded from digital input 0: output, supports slaving from another clock source while receiving data from digital input. The other clock source must be synchronous with the digital input signal	W
6	DIRMCKDIR: Digital in RMCK direction 1=input, 0=output NOTE: This signal may be removed in production versions	W
7	*A Model Rev NC* VIDEN: Enables routing of SYNC IN signal to video sync extraction circuitry. Must be asserted in order to sync to video. NOTE: SYNC IN signal is always routed to the external clock input of the clock generator. A Model Rev A, B Model Rev NC No function A Model Rev B, B Model Rev A, C Model Rev NC VPLLENn: Enables video PLL. Active low.	W

2.18 MIXBLOCK:Mixer Control Block (read/write)

BYTE Offset	DWORD Offset	Register
000	00	RMIX0 Control to Record Stream 0 Left
004	01	RMIX1 Control to Record Stream 0 Right
008	02	RMIX2 Control to Record Stream 1 Left

00C	03	RMIX3 Control to Record Stream 1 Right
010	04	RMIX4 Control to Record Stream 2 Left
014	05	RMIX5 Control to Record Stream 2 Right
018	06	RMIX6 Control to Record Stream 3 Left
01C	07	RMIX7 Control to Record Stream 3 Right
020	08	RMIX8 Control to Record Stream 4 Left
024	09	RMIX9 Control to Record Stream 4 Right
028	0A	RMIX10 Control to Record Stream 5 Left
02C	0B	RMIX11 Control to Record Stream 5 Right
030	0C	RMIX12 Control to Record Stream 6 Left
034	0D	RMIX13 Control to Record Stream 6 Right
038	0E	RMIX14 Control to Record Stream 7 Left
03C	0F	RMIX15 Control to Record Stream 7 Right
040 – 0FF	10 - 3F	Reserved (48 DWORDS)
100 – 10F	40 - 43	PMIX0 Control to OUT 1
110 – 11F	44 - 47	PMIX1 Control to OUT 2
120 – 12F	48 – 4B	PMIX2 Control to OUT 3
130 – 13F	4C – 4F	PMIX3 Control to OUT 4
140 – 14F	50 – 53	PMIX4 A Model: Control to Loopback Left Register B Model: Control to OUT 5 C Model: Only output via OP2
150 – 15F	54 – 57	PMIX5 A Model: Control to Loopback Right Register B Model: Control to OUT 6 C Model: Only output via OP2
160 – 16F	58 – 5B	PMIX6 Control to DIGITAL OUT LEFT
170 – 17F	5C – 5F	PMIX7 Control to DIGITAL OUT RIGHT
180 – 18F	60 – 63	PMIX8 Control to Option Module Channel 1 Output
190 – 19F	64 – 67	PMIX9 Control to Option Module Channel 2 Output
1A0 – 1AF	68 – 6B	PMIX10 Control to Option Module Channel 3 Output
1B0 – 1BF	6C – 6F	PMIX11 Control to Option Module Channel 4 Output
1C0 – 1CF	70 – 73	PMIX12 Control to Option Module Channel 5 Output
1D0 – 1DF	74 – 77	PMIX13 Control to Option Module Channel 6 Output
1E0 – 1EF	78 – 7B	PMIX14 Control to Option Module Channel 7 Output
1F0 – 1FF	7C – 7F	PMIX15 Control to Option Module Channel 8 Output
200	80	RMIX0 Status to Record Stream 0 Left
204	81	RMIX1 Status to Record Stream 0 Right
208	82	RMIX2 Status to Record Stream 1 Left
20C	83	RMIX3 Status to Record Stream 1 Right
210	84	RMIX4 Status to Record Stream 2 Left
214	85	RMIX5 Status to Record Stream 2 Right

218	86	RMIX6 Status to Record Stream 3 Left
21C	87	RMIX7 Status to Record Stream 3 Right
220	88	RMIX8 Status to Record Stream 4 Left
224	89	RMIX9 Status to Record Stream 4 Right
228	8A	RMIX10 Status to Record Stream 5 Left
22C	8B	RMIX11 Status to Record Stream 5 Right
230	8C	RMIX12 Status to Record Stream 6 Left
234	8D	RMIX13 Status to Record Stream 6 Right
238	8E	RMIX14 Status to Record Stream 7 Left
23C	8F	RMIX15 Status to Record Stream 7 Right
240	90	PMIX0 Status to LEFT OUT 1
244	91	PMIX1 Status to RIGHT OUT 1
248	92	PMIX2 Status to LEFT OUT 2
24C	93	PMIX3 Status to RIGHT OUT 2
250	94	PMIX4 Status
254	95	PMIX5 Status
258	96	PMIX6 Status to DIGITAL OUT LEFT
25C	97	PMIX7 Status to DIGITAL OUT RIGHT
260	98	PMIX8 Status to Option Module Channel 1 Output
264	99	PMIX9 Status to Option Module Channel 2 Output
268	9A	PMIX10 Status to Option Module Channel 3 Output
26C	9B	PMIX11 Status to Option Module Channel 4 Output
270	9C	PMIX12 Status to Option Module Channel 5 Output
274	9D	PMIX13 Status to Option Module Channel 6 Output
278	9E	PMIX14 Status to Option Module Channel 7 Output
27C	9F	PMIX15 Status to Option Module Channel 8 Output

2.18.1 RMIX Control Register (Write Only)

BIT	FUNCTION
5:0	INSRC[5:0]: Controls input source select mux 0 = IN 1 1 = IN 2 2 = IN 3 3 = IN 4 4 = A Model: LOOPBACK REGISTER LEFT B Model: Not valid C Model: IN 5 5 = A Model: LOOPBACK REGISTER RIGHT B Model: Not valid C Model: IN 6 6 = DIGITAL IN LEFT

	7 = DIGITAL IN RIGHT 8 – 31 reserved 32 = OPTION PORT1 CHANNEL 1 INPUT 33 = OPTION PORT 1 CHANNEL 2 INPUT 34 = OPTION PORT 1 CHANNEL 3 INPUT 35 = OPTION PORT 1 CHANNEL 4 INPUT 36 = OPTION PORT 1 CHANNEL 5 INPUT 37 = OPTION PORT 1 CHANNEL 6 INPUT 38 = OPTION PORT 1 CHANNEL 7 INPUT 39 = OPTION PORT 1 CHANNEL 8 INPUT 40 = OPTION PORT1 CHANNEL 9 INPUT 41 = OPTION PORT 1 CHANNEL 10 INPUT 42 = OPTION PORT 1 CHANNEL 11 INPUT 43 = OPTION PORT 1 CHANNEL 12 INPUT 44 = OPTION PORT 1 CHANNEL 13 INPUT 45 = OPTION PORT 1 CHANNEL 14 INPUT 46 = OPTION PORT 1 CHANNEL 15 INPUT 47 = OPTION PORT 1 CHANNEL 16 INPUT 48 = OPTION PORT 2 CHANNEL 1 INPUT 49 = OPTION PORT 2 CHANNEL 2 INPUT 50 = OPTION PORT 2 CHANNEL 3 INPUT 51 = OPTION PORT 2 CHANNEL 4 INPUT 52 = OPTION PORT 2 CHANNEL 5 INPUT 53 = OPTION PORT 2 CHANNEL 6 INPUT 54 = OPTION PORT 2 CHANNEL 7 INPUT 55 = OPTION PORT 2 CHANNEL 8 INPUT 56 = OPTION PORT2 CHANNEL 9 INPUT 57 = OPTION PORT 2 CHANNEL 10 INPUT 58 = OPTION PORT 2 CHANNEL 11 INPUT 59 = OPTION PORT 2 CHANNEL 12 INPUT 60 = OPTION PORT 2 CHANNEL 13 INPUT 61 = OPTION PORT 2 CHANNEL 14 INPUT 62 = OPTION PORT 2 CHANNEL 15 INPUT 63 = OPTION PORT 2 CHANNEL 16 INPUT NOTE: Channels 9 – 16 of Option Port 1 and 2 are only available in single speed mode (sample rate < 50 kHz).
7:6	DTYPE[1:0]: Global dither type for all inputs. Resides in RMIX0 only. 0 = none 1 = Triangular PDF 2 = Triangular PDF – Hi Pass 3 = Rectangular PDF
9:8	DDEPTH[1:0]: Dither depth – number of bits. 0 = 8 1 = 16

	2 = 20 3 = 24
10	RMIXDITH: Dither enable. Enables dither addition on each stream.
11	RMUTE: RMIX Mute

2.18.2 PMIX Control Register Group (Write Only)

The PMIX mixer is controlled by four registers that specify the play source and associated volume for each mixer input. The CTLx registers are also used to send control data to option port outputs.

BYTE Offset	**DWORD Offset**	**Register (32 bits)**
0	0	CTLA: PMIX A control
4	1	CTLB: PMIX B control
8	2	CTLC: PMIX C control
C	3	CTLD: PMIX D control

PMIX Control Register (PMIX CTLA, PMIX CTLB, PMIX CTLC, PMIX CTLD)

BIT	**FUNCTION**
15:0	VOL[15:0]: Volume control, -32768 to32767 linear, signed 16-bit value. Negative values cause signal inversion (180 degree phase change).
16	VOLBYP: Volume bypass. 1 = volume bypass
21:17	PSRC[4:0]: Play source select 0 = RECORD STREAM 0 LEFT 1 = RECORD STREAM 0 RIGHT : : 14 = RECORD STREAM 7 LEFT 15 = RECORD STREAM 7 RIGHT 16 = PLAY STREAM 0 LEFT 17 = PLAY STREAM 0 RIGHT : : 30 = PLAY STREAM 7 LEFT 31 = PLAY STREAM 7 RIGHT
22	PMIXDITH: Enables triangular PDF dither for PMIX processing. Resides in CTLA register in each PMIX control group.
31:23	**Unused**

2.18.3 RMIX Status Register

BIT	**FUNCTION**	**R/W**
19:0	LEVEL[19:0]: RMIX peak level, 19-bits + 1, range = 0 to 80000h (note: convert 80000h to 7ffffh for convenient data handling)	R
20	LVLRESET: RMIX peak level reset. Asserting this bit forces the RMIX peak level to zero.	W
31:2	Reserved	

1		

2.18.4 PMIX Status Register

BIT	FUNCTION	R/W
19:0	LEVEL[19:0]: PMIX peak level, 20- bits	R
20	LVLRESET: PMIX peak level reset. Asserting this bit forces the PMIX peak level to zero.	W
21	MIXOVL: Playback mixer overload flag. Indicates an arithmetic overflow in a PMIX accumulator. This bit is sticky and must be reset with LVLRESET.	R
22	OVLRESET: PMIX overload flag reset. Asserting this bit forces the PMIX overload flag to zero.	W
31:21	Reserved	

3 Audio Data RAM Region

Accessed via target transfers to BAR1.

Host Address Offset		**Circular Buffer Resource** (4096 DWORDS each)
Byte Aligned	**DWORD Aligned**	
00000 – 03FFF	0000 - 0FFF	Record Stream 0
04000 – 07FFF	1000 - 1FFF	Record Stream 1
08000 – 0BFFF	2000 - 2FFF	Record Stream 2
0C000 – 0FFFF	3000 - 3FFF	Record Stream 3
10000 – 13FFF	4000 - 4FFF	Record Stream 4
14000 – 17FFF	5000 - 5FFF	Record Stream 5
18000 – 1BFFF	6000 - 6FFF	Record Stream 6
1C000 – 1FFFF	7000 - 7FFF	Record Stream 7
20000 – 23FFF	8000 - 8FFF	Play Stream 0
24000 – 27FFF	9000 – 9FFF	Play Stream 0
28000 – 2BFFF	A000 – AFFF	Play Stream 0
2C000 – 2FFFF	B000 – BFFF	Play Stream 0
30000 – 33FFF	C000 – CFFF	Play Stream 0
34000 – 37FFF	D000 – DFFF	Play Stream 0
38000 – 3BFFF	E000 – EFFF	Play Stream 0
3C000 – 3FFFF	F000 - FFFF	Play Stream 0

4 DMA Buffer List (DBL)

Resides in host memory at the location specified by GDBLADDR bits in DMACTL register. It is 2048 bytes in size and must reside on a 2048 byte memory boundary.

BYTE Offset	DWORD Offset	Stream Buffer Block (32 DWORDS each)	DMA Channel Index
000	000	Record 0	0
080	020	Record 1	1
100	040	Record 2	2
180	060	Record 3	3
200	080	Record 4	4
280	0A0	Record 5	5
300	0C0	Record 6	6
380	0E0	Record 7	7
400	100	Play 0	8
480	120	Play 1	9
500	140	Play 2	A
580	160	Play 3	B
600	180	Play 4	C
680	1A0	Play 5	D
700	1C0	Play 6	E
780	1E0	Play 7	F

Each Stream Buffer Block contains 16 host buffer descriptors.

BYTE Offset	DWORD Offset	Stream Buffer Block (32 DWORDS each)
000	000	Descriptor 0 Host Buffer Pointer
004	001	Descriptor 0 Control
008	002	Descriptor 1 Host Buffer Pointer
00C	003	Descriptor 1 Control
|	|	|
|	|	|
078	01E	Descriptor 15 Host Buffer Pointer
07C	01F	Descriptor 15 Control

Descriptor Host Buffer Pointer

BIT	FUNCTION
31:0	HBUFPTR: Host address of buffer (must by DWORD aligned). During DMA transfers the DMA controller will increment this register if the host buffer size exceeds the required circular buffer transfer size.

Descriptor Control

BIT	FUNCTION
21:0	HBUFLEN[21:0]: Host buffer length (in DWORDS).). During DMA transfers the DMA controller will decrement this register. A zero value indicates the completion of the transfer to/from the host buffer.
22	HBUFIE: Host buffer transfer completion interrupt enable

5 Mixer (A Model shown)