Lab3 report

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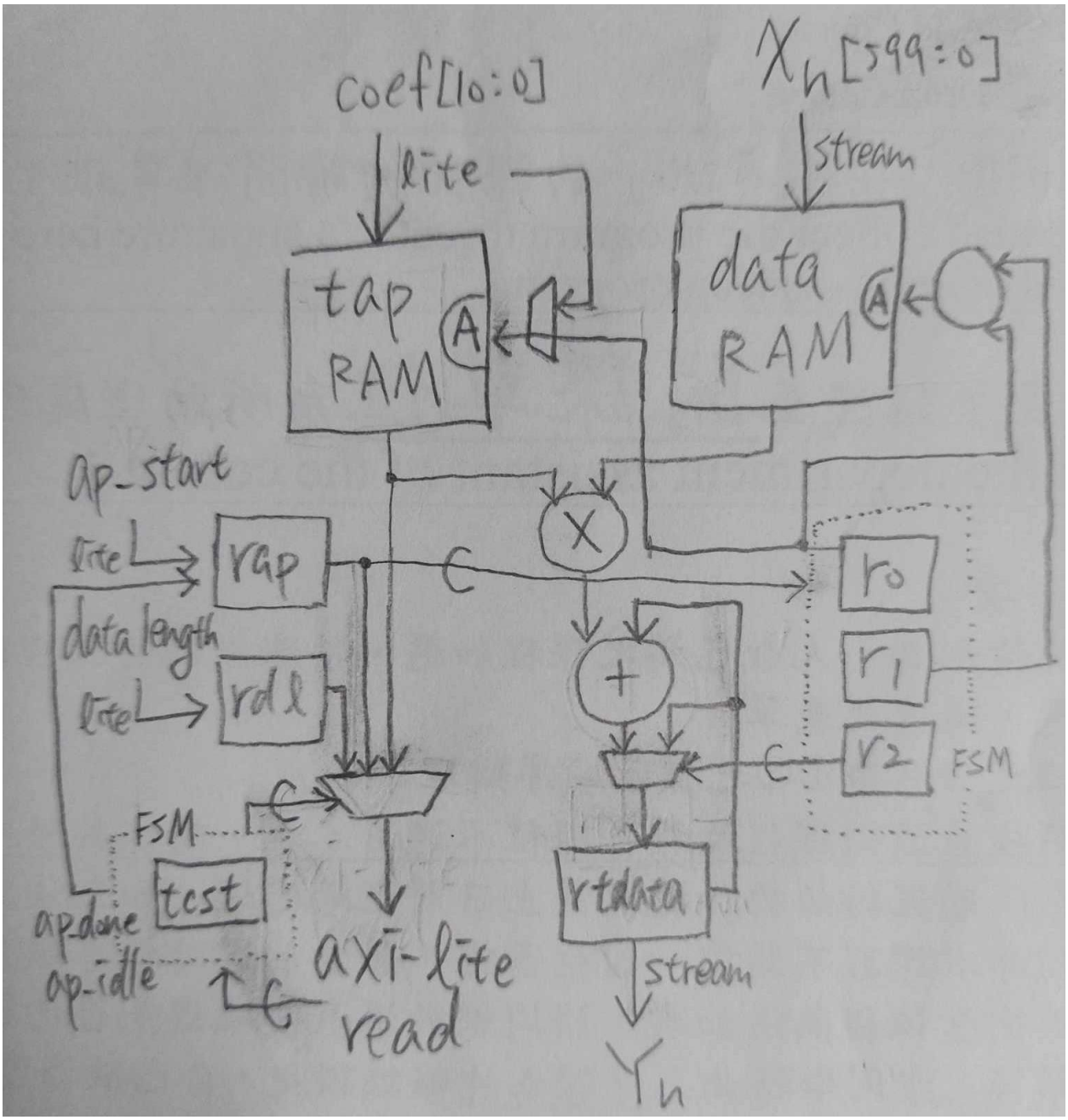
Block Diagram: b1.jpg



Describe operation

- How to receive data-in and tap parameters and place into SRAM

  Xn/coef -> reg -> SRAMs, use two FSMs to respectively control the two data flows.

- How to access shiftram and tapRAM to do computation
  Use the FSM with higher priority than another to control the A of two SRAMs, then take the data to do computation.
- How ap_done is generated.
  Y599 computed -> set sm_tlast -> ap_reg becomes 3'b110

Resource usage

Because the BRAMs are declared in testbench, they were not synthesized here in the FIR engine design.

LUT	FF	BRAM	URAM	DSP
285	178	0	0	3

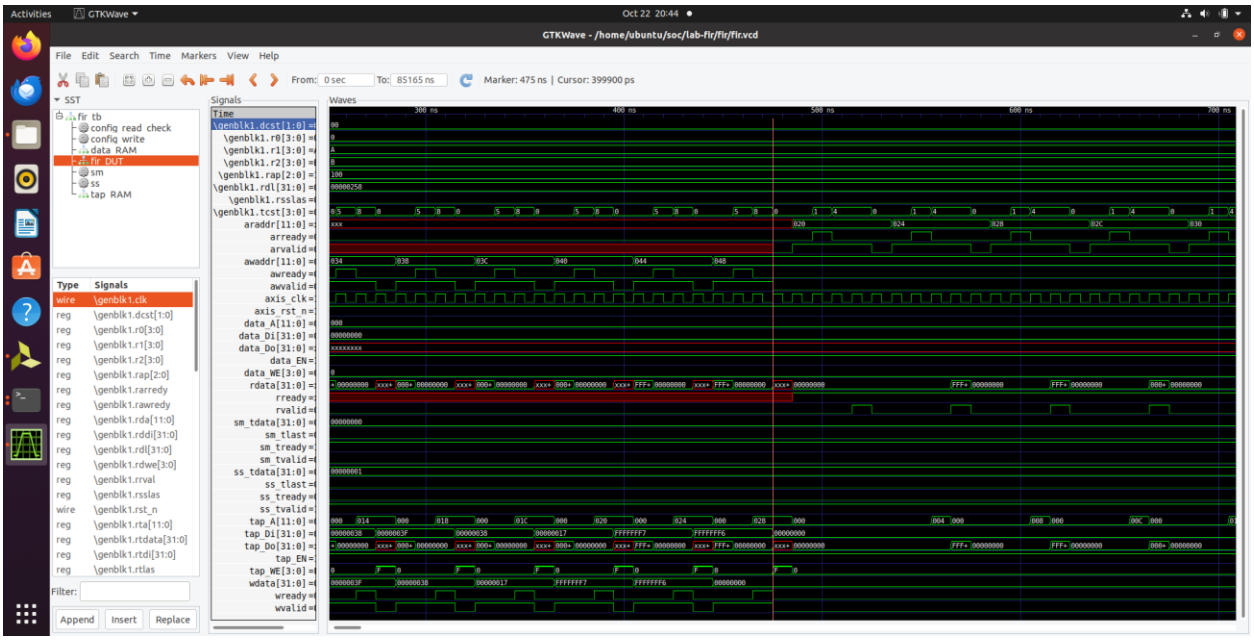
Timing Report

Clock period: 4 ns, Rise time: 0.000 ns, Fall time: 2.000 ns.

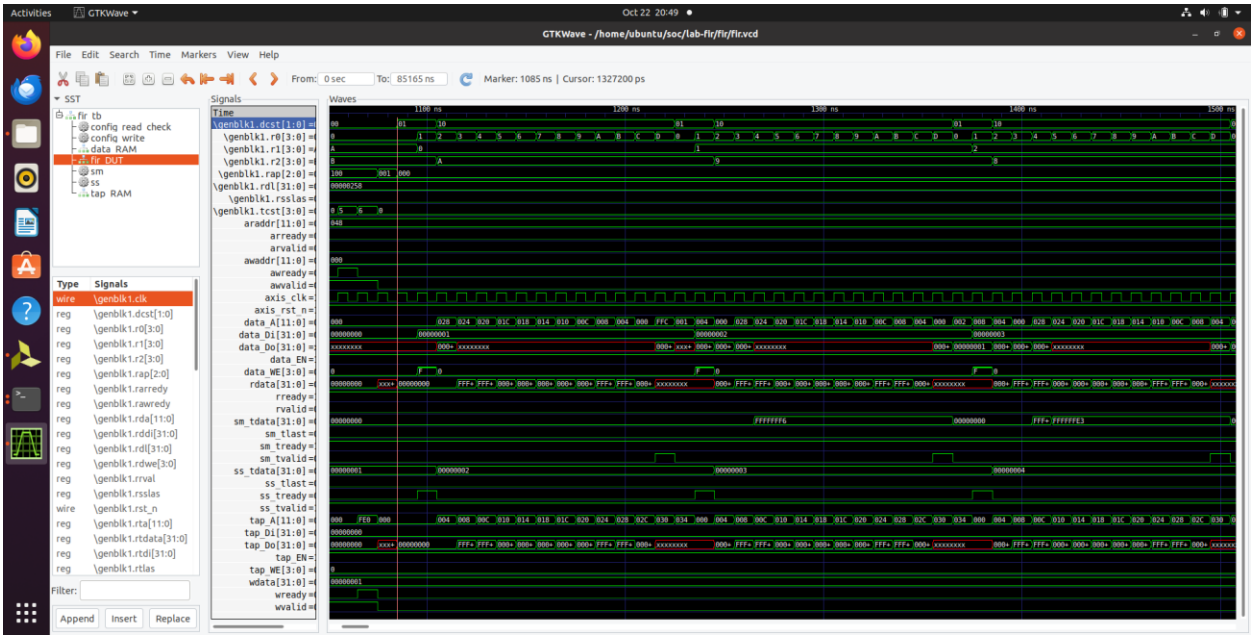
Worst negative slack	Worst hold slack	Worst pulse width slack
0.031 ns	0.147 ns	1.500 ns

Simulation Waveform

w1.png:



w2.png:



- Coefficient program, and read back:
  w1: the left half is coef program, and the right half is read back.
- Data-in stream in:
  w2: ss tdata ~ tvalid
- Data-out stream out:
  w2: sm tdata ~ tvalid
- Bram access control:
  w1: tap RAM, w2: data RAM
- FSM:
  w1: tcst, w2: dcst and r0 ~ 2

Supplementary Information

At {fir.v:1, fir.v:269, fir_tb.v:22, fir_tb.v:23, fir_tb.v:247}, I added something and commented with // !!!!!!!!!!!!!!!!!!!!!!!!!!!!.