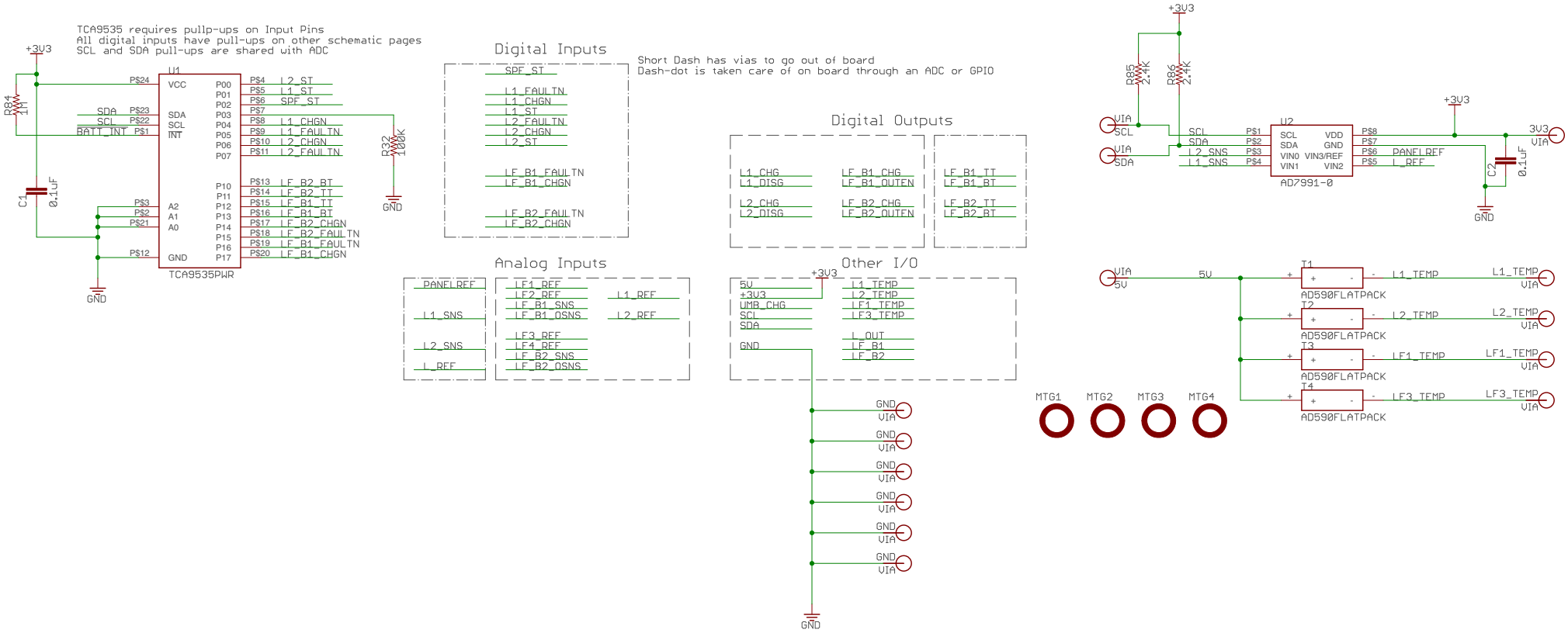
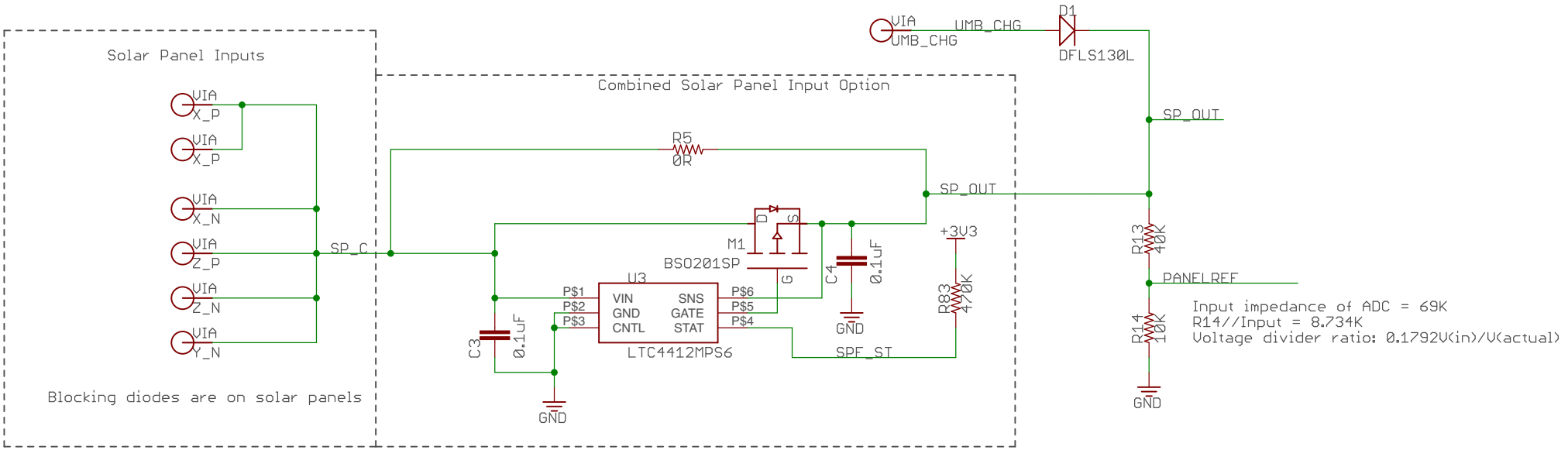
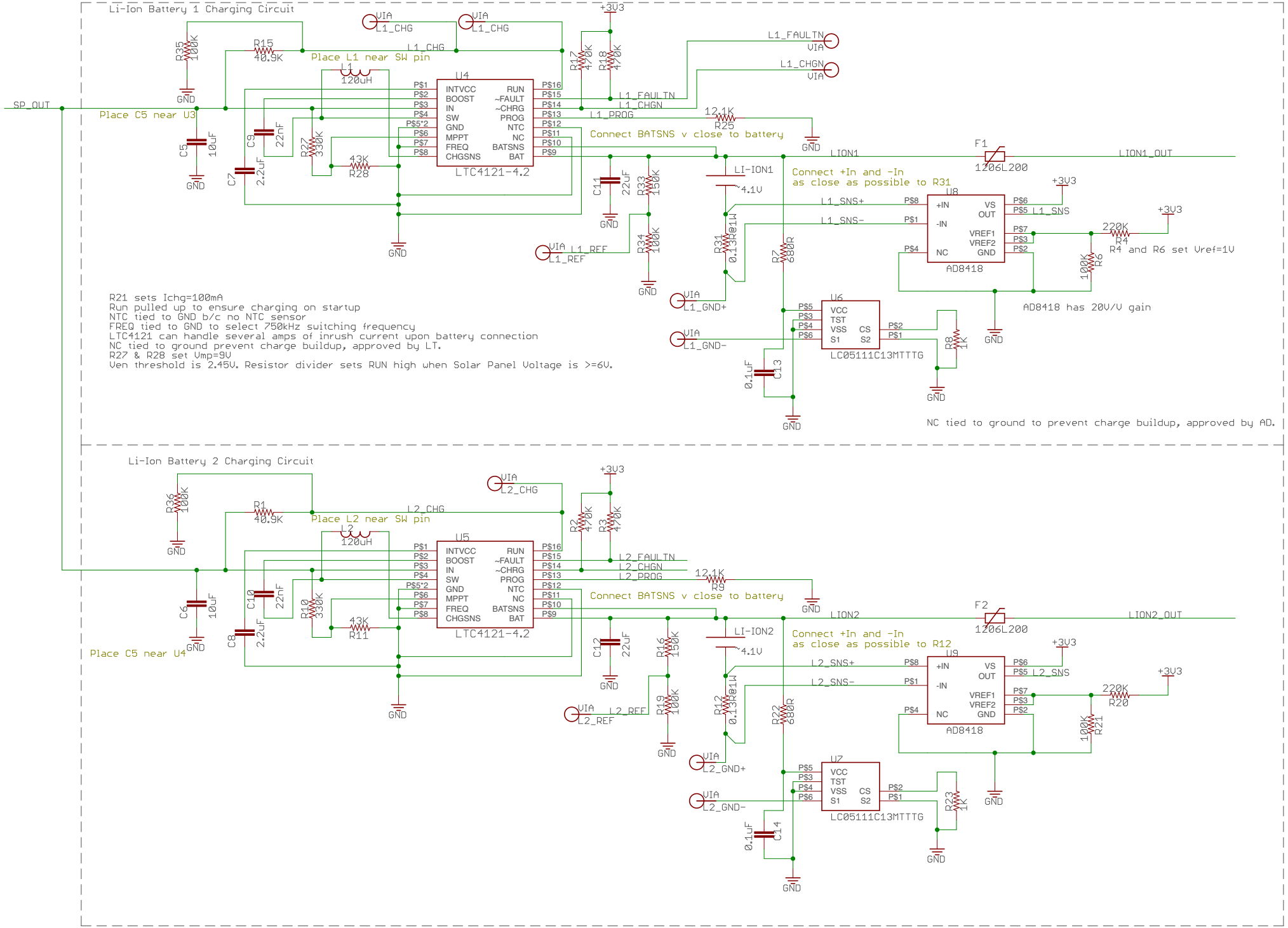
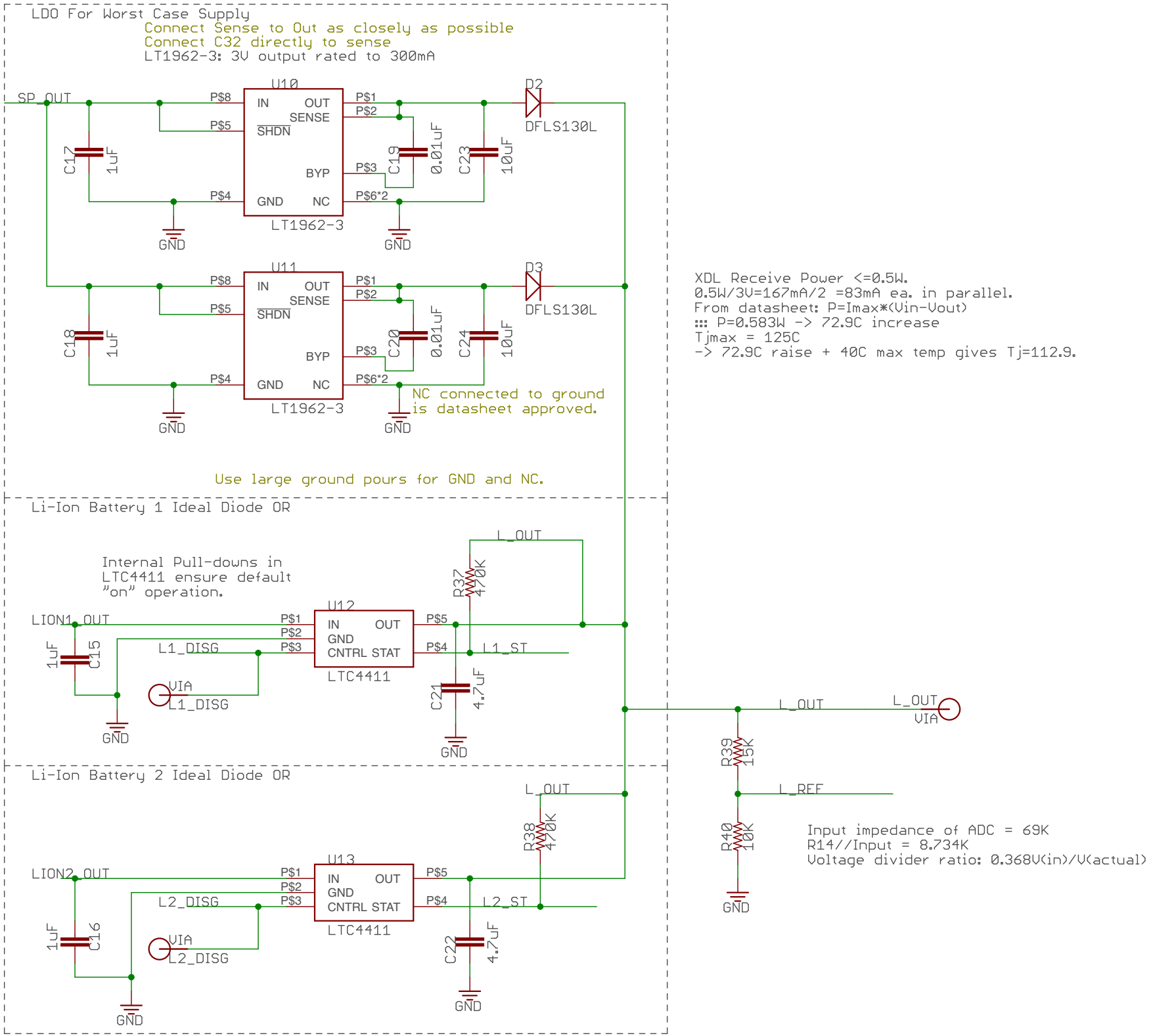
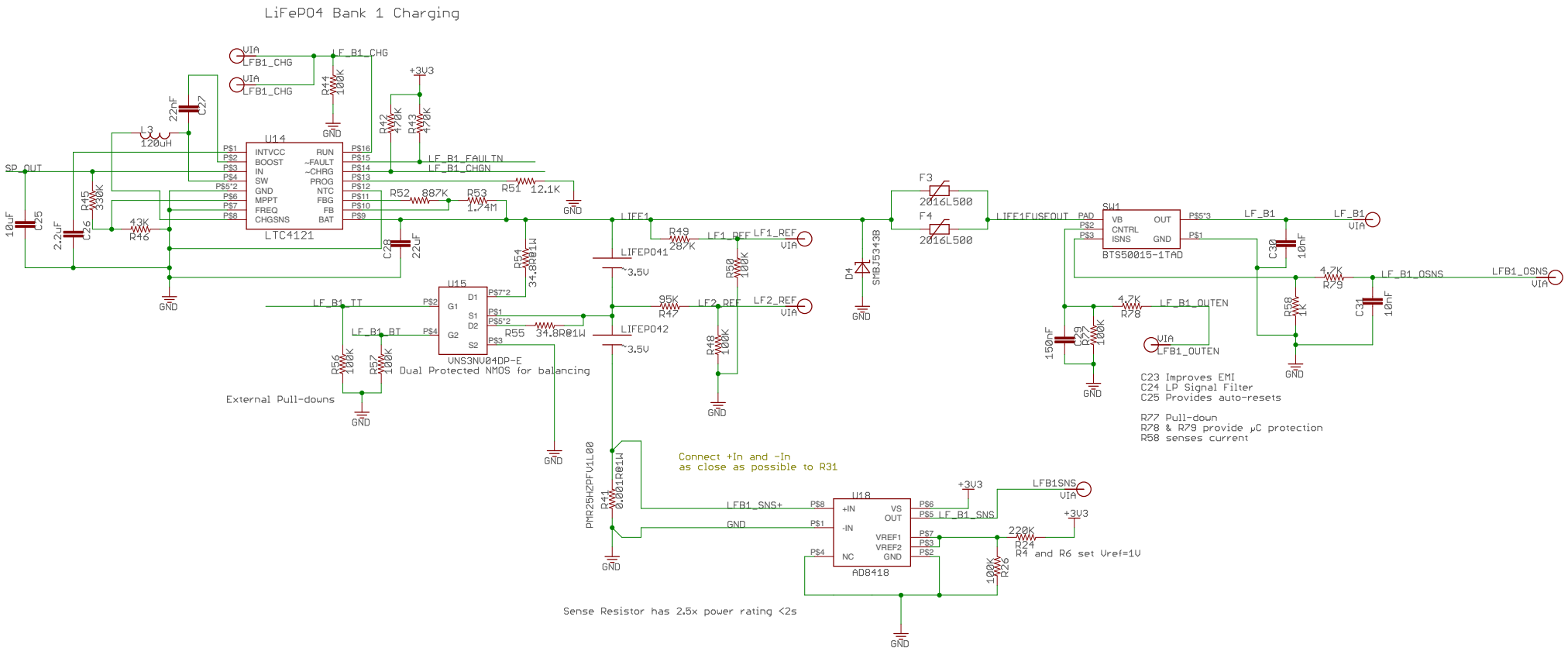

TCA9535 requires pullp-ups on Input Pins
All digital inputs have pull-ups on other schematic pages
SCL and SDA pull-ups are shared with ADC
+3V3
R84
1M
U1
VCC
SDA
SCL
INT
A2
A1
A0
GND
P00
P01
P02
P03
P04
P05
P06
P07
P10
P11
P12
P13
P14
P15
P16
P17
TCA9535PWR
C1
0.1uF
R32
100K
Digital Inputs
SPF_ST
L1_FAULTN
L1_CHGN
L1_ST
L2_FAULTN
L2_CHGN
L2_ST
LF_B1_FAULTN
LF_B1_CHGN
LF_B2_FAULTN
LF_B2_CHGN
Short Dash has vias to go out of board
Dash-dot is taken care of on board through an ADC or GPIO
Digital Outputs
L1_CHG
L1_DISG
L2_CHG
L2_DISG
LF_B1_CHG
LF_B1_OUTEN
LF_B2_CHG
LF_B2_OUTEN
LF_B1_TT
LF_B1_BT
LF_B2_TT
LF_B2_BT
Analog Inputs
PANEL_REF
L1_SNS
L2_SNS
L_REF
LF1_REF
LF2_REF
LF_B1_SNS
LF_B1_OSNS
LF3_REF
LF4_REF
LF_B2_SNS
LF_B2_OSNS
L1_REF
L2_REF
Other I/O
5V
+3V3
UMB_CHG
SCL
SDA
GND
L1_TEMP
L2_TEMP
LF1_TEMP
LF3_TEMP
L_OUT
LF_B1
LF_B2
GND
VIA
R85
2.4K
R86
2.4K
U2
AD7991-0
C2
0.1uF
3V3
PANEL_REF
L_REF
L1_SNS
L2_SNS
T1
T2
T3
T4
AD590FLATPACK
MTG1
MTG2
MTG3
MTG4

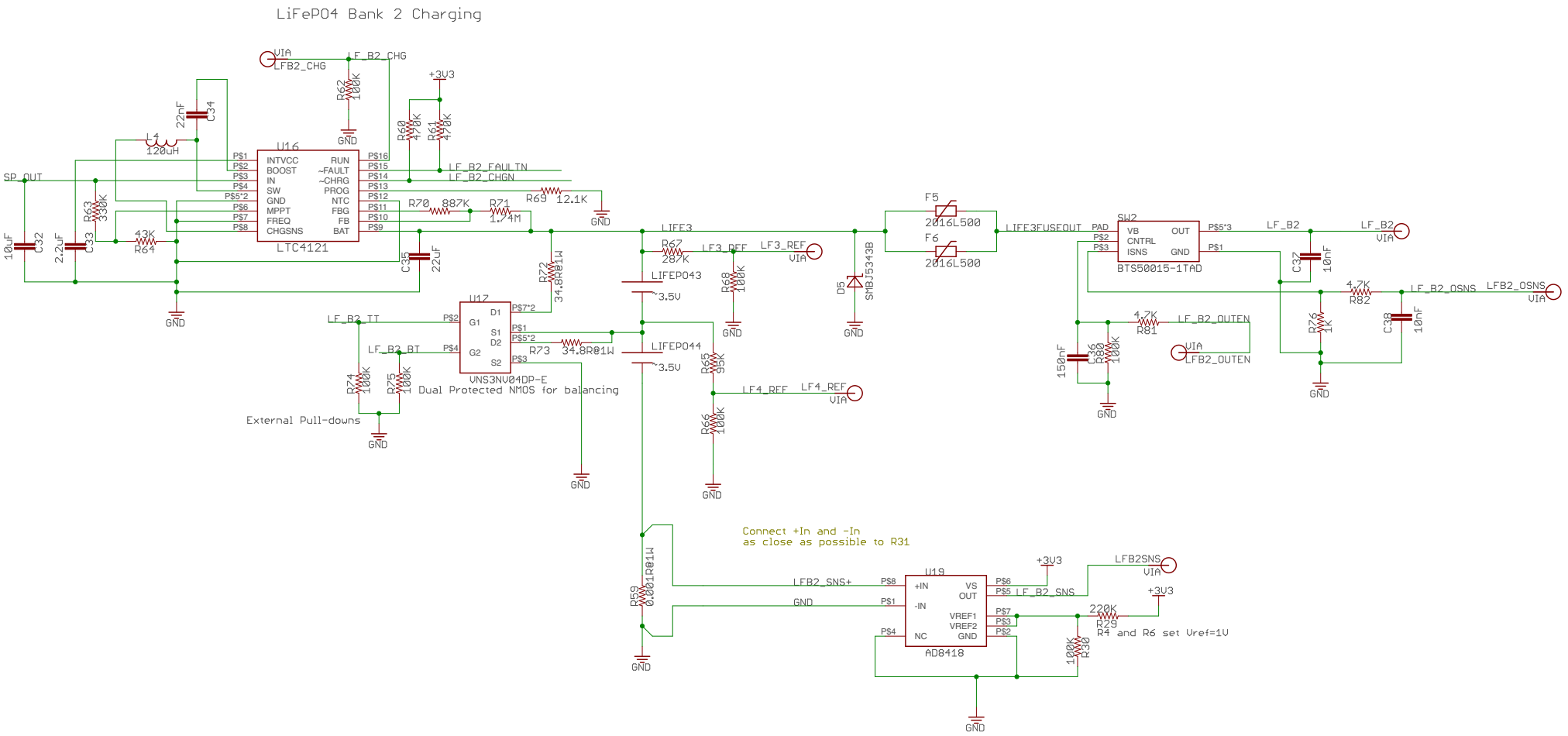
Solar Panel Front End




Place GND vias under U3 and U4.
Connect all caps to ground plane.
VIAs added for debugging circuit functionality.
Li-Ion Battery 1 Charging Circuit
SP_OUT
Place C5 near U3
Place L1 near SW pin
Connect BATSNS v close to battery
Connect +In and -In as close as possible to R31
LTC4121-4.2
AD8418
LC05111C13MTTTG
AD8418 has 20V/V gain
R4 and R6 set Vref=1V
R21 sets Ichg=100mA
Run pulled up to ensure charging on startup
NTC tied to GND b/c no NTC sensor
FREQ tied to GND to select 750kHz switching frequency
LTC4121 can handle several amps of inrush current upon battery connection
NC tied to ground prevent charge buildup, approved by LT.
R27 & R28 set Vmp=9V
Ven threshold is 2.45V. Resistor divider sets RUN high when Solar Panel Voltage is >=6V.
NC tied to ground to prevent charge buildup, approved by AD.
Li-Ion Battery 2 Charging Circuit
Place C5 near U4
Place L2 near SW pin
Connect BATSNS v close to battery
Connect +In and -In as close as possible to R12
LTC4121-4.2
AD8418
LC05111C13MTTTG


LDO For Worst Case Supply
Connect Sense to Out as closely as possible
Connect C32 directly to sense
LT1962-3: 3V output rated to 300mA
SP_OUT
U10
IN
OUT
SENSE
SHDN
BYP
GND
NC
LT1962-3
P$8
P$5
P$4
P$1
P$2
P$3
P$6*2
C17
1uF
C19
0.01uF
C23
10uF
D2
DFLS130L
GND
U11
C18
1uF
C20
0.01uF
C24
10uF
D3
DFLS130L
NC connected to ground
is datasheet approved.
Use large ground pours for GND and NC.
XDL Receive Power <=0.5W.
0.5W/3V=167mA/2 =83mA ea. in parallel.
From datasheet: P=Imax*(Vin-Vout)
::: P=0.583W -> 72.9C increase
Tjmax = 125C
-> 72.9C raise + 40C max temp gives Tj=112.9.
Li-Ion Battery 1 Ideal Diode OR
Internal Pull-downs in
LTC4411 ensure default
"on" operation.
LION1_OUT
U12
GND
CNTRL
STAT
LTC4411
L1_DISG
L1_ST
C15
1uF
VIA
C21
4.7uF
R37
470K
L_OUT
Li-Ion Battery 2 Ideal Diode OR
LION2_OUT
U13
L2_DISG
L2_ST
C16
1uF
C22
4.7uF
R38
470K
R39
15K
L_REF
R40
10K
Input impedance of ADC = 69K
R14//Input = 8.734K
Voltage divider ratio: 0.368V(in)/V(actual)


LiFePO4 Bank 1 Charging
VIA
LFB1_CHG
LF_B1_CHG
R44 100K
+3V3
R42 470K
R43 470K
22nF C27
L3 120uH
U14
LTC4121
INTVCC
BOOST
IN
SW
GND
MPPT
FREQ
CHGSNS
RUN
~FAULT
~CHRG
PROG
NTC
FBG
FB
BAT
LF_B1_FAULTN
LF_B1_CHGN
SP_OUT
10uF C25
2.2uF C26
R45 330K
43K R46
R52 887K
R53 1.74M
R51 12.1K
GND
C28 22uF
R54 34.8R@1W
LIFE1
LIFEPO41
3.5V
LIFEPO42
3.5V
R49 287K
LF1_REF
R50 100K
LF2_REF
R47 95K
R48 100K
D4 SMBJ5343B
F3 2016L500
F4 2016L500
LIFE1FUSEOUT
SW1
BTS50015-1TAD
VB
CNTRL
ISNS
OUT
GND
PAD
LF_B1
C30 10nF
4.7K R79
LF_B1_OSNS
LFB1_OSNS
C31 10nF
R58 1K
4.7K R78
LF_B1_OUTEN
LFB1_OUTEN
150nF C29
R77 100K
U15
VNS3NV04DP-E
Dual Protected NMOS for balancing
D1
G1
S1
D2
G2
S2
LF_B1_TT
LF_B1_BT
R55 34.8R@1W
R56 100K
R57 100K
External Pull-downs
C23 Improves EMI
C24 LP Signal Filter
C25 Provides auto-resets
R77 Pull-down
R78 & R79 provide µC protection
R58 senses current
Connect +In and -In
as close as possible to R31
PMR25HZPFV1L00
R41 0.001R@1W
LFB1_SNS+
LFB1_SNS-
U18
AD8418
+IN
-IN
NC
VS
OUT
VREF1
VREF2
LF_B1_SNS
LFB1SNS
220K R24
100K R26
R4 and R6 set Vref=1V
Sense Resistor has 2.5x power rating <2s


LiFePO4 Bank 2 Charging
VIA
LFB2_CHG
LF_B2_CHG
R62 100K
GND
+3V3
R60 470K
R61 470K
22nF C34
L4 120uH
U16
INTVCC
BOOST
IN
SW
GND
MPPT
FREQ
CHGSNS
RUN
~FAULT
~CHRG
PROG
NTC
FBG
FB
BAT
LTC4121
LF_B2_FAULTN
LF_B2_CHGN
SP_OUT
R63 330K
10uF C32
2.2uF C33
43K R64
R70 887K
R71 1.74M
R69 12.1K
C35 22uF
R72 34.8R01W
LIFE3
R67 287K
LF3_REF
LF3_REF
VIA
LIFEPO43
3.5V
R68 100K
D5 SMBJ5343B
F5 2016L500
F6 2016L500
LIFE3FUSEOUT
SW2
VB
CNTRL
ISNS
OUT
GND
PAD
BTS50015-1TAD
LF_B2
LF_B2
VIA
C37 10nF
4.7K R82
LF_B2_OSNS
LFB2_OSNS
VIA
R76 1K
C38 10nF
4.7K R81
LF_B2_OUTEN
VIA
LFB2_OUTEN
150nF C36
R80 100K
U17
D1
G1
S1
D2
G2
S2
VNS3NV04DP-E
Dual Protected NMOS for balancing
LF_B2_TT
LF_B2_BT
R73 34.8R01W
LIFEPO44
3.5V
R74 100K
R75 100K
External Pull-downs
R65 95K
R66 100K
LF4_REF
LF4_REF
VIA
Connect +In and -In
as close as possible to R31
R59 0.001R01W
LFB2_SNS+
GND
U19
+IN
-IN
VS
OUT
VREF1
VREF2
GND
NC
AD8418
+3V3
LFB2SNS
VIA
LF_B2_SNS
+3V3
220K R29
R4 and R6 set Vref=1V
100K R30