A Feedforward Double-Sampled Sigma-Delta Modulator with a Reduced Number of Switches

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***Abstract*— The double-sampling technique for sigma-delta modulators can help to increase the signal-to-noise ratio by increasing the oversampling ratio without changing the clock period. However, this technique suffers from technological mismatch of input capacitors (in the case of fixed-point circuit realization) and from amplifier overload. In this paper we propose a second-order feedforward double-sampled sigma-delta modulator structure, which overcomes mentioned problems and requires less number of switches in comparison with the conventional structure of double-sampled feedforward sigma-delta modulator. The circuit simulation using Cadence Virtuoso and parameters of a 180 nm CMOS process shows a dynamic range of 83 dB at an oversampling rate of 128.**

Keywords*— *sigma-delta modulator, double-sampling technique, feedforward, switched-capacitor circuit

I. INTRODUCTION

Sigma-delta (ΣΔ) modulators are widely used in analog-to-digital conversion [1]-[3]. The modulator characteristics are limited by the dynamic range of the input signal and imperfections of the blocks that make up the modulator. Thus, due to the nonlinear characteristics of the operational amplifiers, multiple harmonics appear in the output signal. Hence signal-to-noise-and-distortion ratio (SNDR) of the ΣΔ modulator's output signal would degrade. To resolve this problem, the feedforward structure can be used. In this case the signal swing in the modulator will be lowered.

The double-sampling technique is useful for switched-capacitor ΣΔ modulators as with this technique the circuit operates the input signal in both phases of a clock period. Therefore, the sampling frequency can be doubled without increasing the clock frequency. The basic double-sampling fixed-point integrator [4]-[5] is shown in Fig. 1. The capacitor C_{s1} is sampling the input signal during the first clock phase, and the capacitor C_{s2} is sampling the input signal during the second phase. The capacitor C is an integrating capacitor.

One of the main drawbacks of the double-sampling technique is associated with the input capacitance mismatch. The transfer function of the integrator is proportional to C_S/C. If sampling capacitances in first and second phase are different, there will be an additional harmonic near the half of the sampling frequency ($f_S/2–f_{in}$). This additional component does not affect the signal inside the band. Yet the output signal of a digital-to-analog converter (DAC) in the modulator feedback loop contains a high-frequency quantization noise. This signal interacts with the sampled signal through the feedback loop, and the noise is folded into the signal band. In this case the SNDR degrades [6]. There are several ways to overcome this problem. A common approach is the so-called floating-point structure. In this paper we will discuss a method using a double-sampling integrator with a DAC capacitor reset scheme [7].

This paper is concerned with the feedback structure, the feedforward structure and the structure proposed in [8] (for convenience, it will be named after the author of the article as the structure of Hao San), as well as the feedback double-sampling structure and the double-sampling Hao San structure of sigma-delta modulator. Firstly, the ideal operation is compared, and then the influence of capacitor mismatch is studied. A new compact structure of the switched-capacitor circuit is proposed.

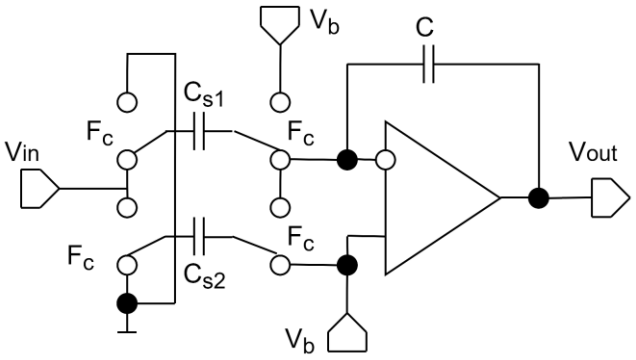

Fig. 1. A double-sampling integrator.

II. MODULATOR STRUCTURES

A. Second-Order Feedback ΣΔ Modulator

This section is devoted to three modulator structures and their transfer functions: the basic second-order feedback ΣΔ modulator, the second-order feedforward ΣΔ modulator and the Hao San structure. This way we can see main differences between the structures, their advantages and drawbacks. A ΣΔ modulator structure of an order greater than 2 can be unstable, so we use a second-order feedback structure as a reference to compare other structures with it.

The second-order feedback ΣΔ modulator is shown in Fig. 2. The output signal of the second-order feedback ΣΔ modulator can be expressed as in (1):

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z), \qquad (1)$$

where $Y(z)$ is the output signal; $X(z)$ – input signal; $E(z)$ – quantization noise.

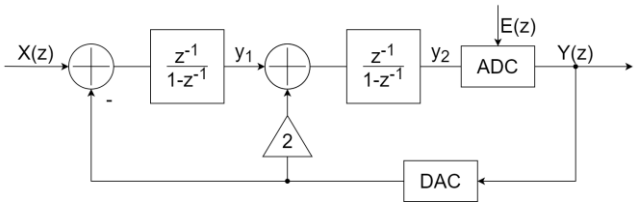

Fig. 2. Block diagram of a second-order feedback ΣΔ modulator.

In formulas (2) and (3) expressions are given for the transfer function of the signal (*STF*) and the quantization noise (*NTF*), respectively:

$$STF = z^{-2} \tag{2}$$

$$NTF = (1 - z^{-1})^2 \tag{3}$$

Expressions for the integrators' outputs are as follows:

$$y_1 = z^{-1}X(z) - z^{-1}(1 - z^{-1})E(z) \tag{4}$$

$$y_2 = z^{-2}X(z) - z^{-1}(2 - z^{-1})E(z) \tag{5}$$

where *y1* is the output signal of the first integrator; *y2* is the output signal of the second integrator.

Thus, it can be seen from formulas (4) and (5) that the output signal of both integrators is a function of the input signal *X*(*z*). As a result, the signal swing at the output of the integrator becomes large, which makes it difficult to use this structure in conditions of a low supply voltage. Multiple harmonics caused by the amplifier non-linearity also affect the swing at the integrator's output, thereby degrading the SNDR.

B. Second-Order Feedforward ΣΔ Modulator

The feedforward structure helps to lower the requirements on the analog blocks. The main purpose of this structure is to process only the quantization noise [9]-[10]. In Fig. 3, a standard block diagram of a second-order ΣΔ modulator using feedforward is shown.

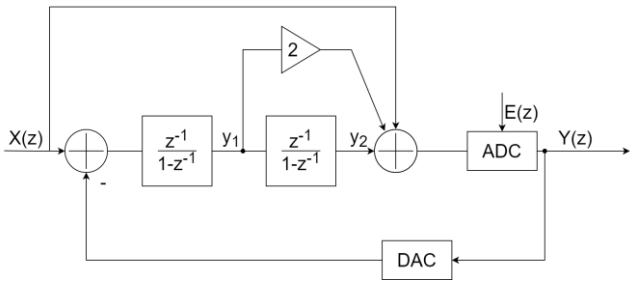

Fig. 3. Block diagram of a second-order feedforward ΣΔ modulator.

The expression for the output signal for the second-order modulator using feedforward is presented in (6):

$$Y(z) = X(z) + (1 - z^{-1})^2 E(z), \tag{6}$$

while signal transfer function and noise transfer function are

$$STF = 1 \tag{7}$$

$$NTF = (1 - z^{-1})^2 \tag{8}$$

Consider the expressions for the output signal of the first (9) and second (10) integrators for this structure:

$$y_1 = -z^{-1}(1 - z^{-1})E(z) \tag{9}$$

$$y_2 = -z^{-2}E(z) \tag{10}$$

As seen, in both cases the integrator output does not contain the input signal, which means that the feedforward ΣΔ modulator processes only the quantization noise. It means that the signal swing at the output of the integrator is lower than in the case of the feedback structure. Harmonic distortion in such a structure does not depend on the level of the input signal.

One of the drawbacks of the feedforward structure is the need to use an adder before the quantizer. In some cases, the adder is implemented as a passive switched-capacitor circuit, but this implementation attenuates the signal supplied to the quantizer (local ADC), thus being suitable only for a 1-bit system. In the case of using a multi-bit signal, a switched-capacitor adder with a weighted summing amplifier is used in front of the quantizer, which leads to a significant complication of the circuit and additional power consumption.

C. Hao San Structure

Fig. 4 shows a block diagram of a second-order ΣΔ modulator with a Hao San structure [8]. In this structure, the adder from the input of the local ADC is transferred to the input of the second integrator. The feedforward signal can be combined with the signal from the output of the first integrator and fed to the input of the second integrator. Thus, there is no need to use an additional amplifier for summing the signals. Also, this structure requires only a single DAC in the feedback loop. This implementation makes it possible to reduce the complexity of the analog part and the DAC, and also reduces the sensitivity of the modulator to the DC gain of the OTA. The expression for the output signal of this structure is the same as the expression for the output signal for the standard feedforward structure. The expressions for the signal at the output of the first (11) and second (12) integrators are:

$$y_1 = -z^{-1}(1 - z^{-1})E(z) \tag{11}$$

$$y_2 = X(z) - z^{-1}(1 - z^{-1})E(z) \tag{12}$$

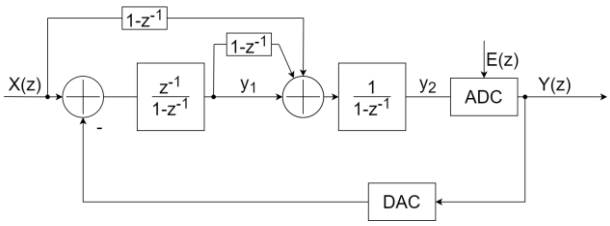

Fig 4. Block diagram of a second-order ΣΔ modulator with the Hao San structure.

From these expressions, it can be seen that the output signal from the second integrator contains a component of the input signal, but in this case, it is possible to avoid imperfections thanks to noise shaping in the feedback loop.

III. Practical Results

A. Hao San Structure Results

In this section the conventional structure of a second-order ΣΔ modulator and the single-sampling Hao San structure are compared. The next step will be to compare the conventional fixed-point double-sampling structure and the double-sampling Hao San structure. This way the advantage of Hao San structure in single-sampling and double-sampling methods will be figured out.

For practical implementation, parameters of a standard 1.8V 180 nm CMOS technology were used. The circuits were simulated in Cadence Virtuoso. The clock frequency was 1 MHz, and an oversampling ratio (OSR) of 128 was chosen.

In Fig. 5 the dependence of SNDR on the amplitude of the input signal for three ΣΔ modulator structures can be found. For the Hao San structure, the maximum SNDR is 69.3 dB with an input signal amplitude of 0.33V. For a standard second-order ΣΔ modulator, the maximum SNDR is 67.6 dB at an input signal amplitude of 0.3 V. It should be noted that for a feedforward (e.g. Hao San) structure, the SNDR is generally higher at higher input signal amplitudes.

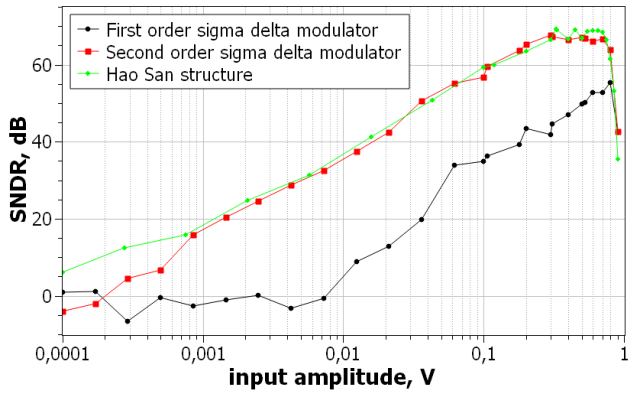

Fig. 5. Dependence of SNDR on the amplitude of the input signal for three ΣΔ modulator structures.

B. Results for Double-Sampling Hao San Structure

Fig. 6 shows the dependence of SNDR from input signal amplitude for the conventional ΣΔ modulator, the fixed-point double-sampling modulator and the double-sampling Hao San structure. In this case, the maximum SNDR for the feedback double-sampling circuit is 71.92 dB at an input signal amplitude of 0.2 V. The maximum SNDR for the ΣΔ modulator using the fixed-point feedforward double-sampling method is 83.39 dB at an amplitude of 0.15 V. From these results we can make a conclusion, that because of distortion at integrators, in the basic double-sampling circuit the SNDR does not give a significant increase in comparison with a conventional second-order ΣΔ modulator, thus we don't get all benefits of using the double-sampling technique. But using of Hao San structure can overcome this problem.

Fig. 7 shows the graph of the SNDR versus the amplitude of the input signal for the ΣΔ modulator using the fixed-point double-sampling method for different values of the capacitance mismatch in the sampling capacitors. It can be found from Fig. 7 that the SNDR of the double-sampling Hao San structure is quite sensitive to the variation in the capacitances of the input capacitors.

It should be noted that in this structure, one of the capacitors is used to implement a direct connection without additional switches. Thus, this circuit uses 40 CMOS switches, and the total capacitance of the capacitors (excluding the integrating ones) is 24.5 pF. For a ΣΔ modulator using the double sampling with a fixed point and feedback, 32 CMOS switches are used, and the total capacitance of the capacitors (excluding the integrating ones) is only 8 pF.

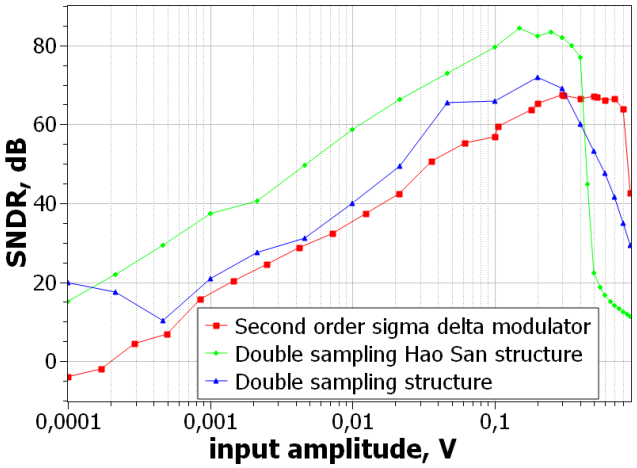

Fig. 6. Comparison of SNDR vs the input signal amplitude for double-sampling and conventional structures.

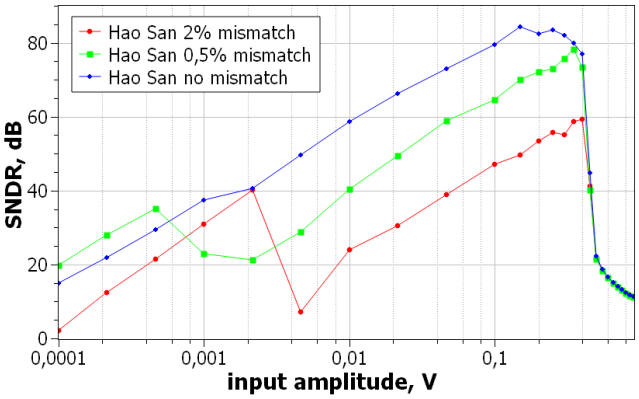

Fig. 7. SNDR vs the amplitude of the input signal for the Hao San structure using the fixed-point double-sampling technique for different values of the mismatch of the sampled capacitors.

In Fig. 8 a circuit of a conventional double-sampled integrator for Hao San structure is shown, while Fig. 9 shows a circuit of an optimized double-sampled integrator for Hao San structure.

In the case of a conventional integrator, in the first phase, one capacitor is connected to the input, which implements the feedforward path (1 – z –1), and the second one is connected to the reference voltage vcm, without affecting the operation of the circuit at the moment. During the second phase, the second capacitor is tied to the input, while the first capacitor is connected to the reference voltage vcm, also

without affecting the operation of the circuit during the second phase. Thus, if, during the operation of the circuit, one of the capacitors is connected to the input node, while the second capacitor does not affect the operation of the integrator, then this feedforward path can be replaced with one capacitor connected directly to the input node.

Fig. 10 shows the response of conventional and optimized double-sampled Hao San integrators. It can be found that two responses are close to each other. For example, at a 1 kHz frequency the difference is equal to 0.47 dB. Therefore, we can assume that both integrators operate identically.

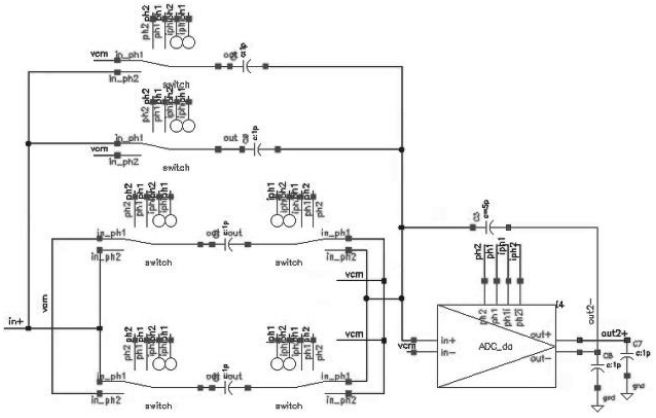

Fig. 8. Conventional double-sampled integrator for Hao San structure.

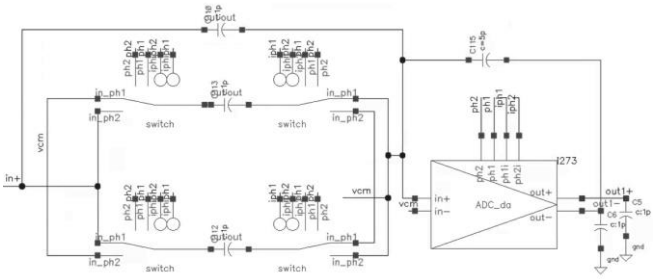

Fig. 9. Optimized double-sampled integrator for Hao San structure.

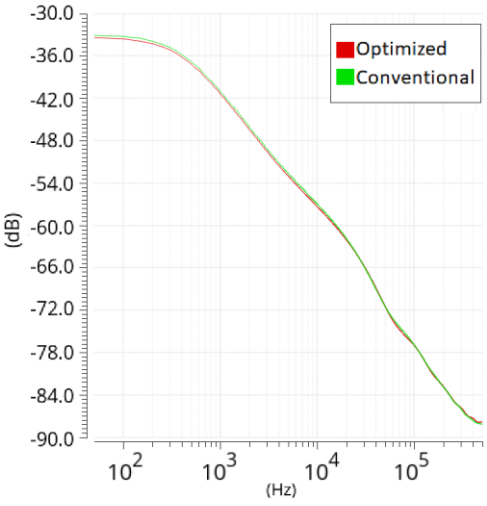

Fig. 10. Frequency response of conventional and optimized double-sampled Hao San integrators.

IV. Input Capacitance Mismatch Issue

The main drawback of the double-sampling technique is associated with the mismatch of the pair of sampling capacitors. A solution of the problem of spectrum folding with the mismatch of the capacitance of the sampling capacitors for the ΣΔ modulator is presented in [7].

In Fig. 11 the integrator with the feedback capacitor reset circuit is presented. Fig. 12 shows a timing diagram for an integrator with the reset circuit. Due to the fact that only one capacitor is used to provide feedback for both phases, it is possible to eliminate the spectrum folding effect. However, in order for this circuit to work, it is necessary to introduce an additional reset signal, which will be triggered between the pulses of the first and second phase. The clock circuit becomes more complex but the result is worth it.

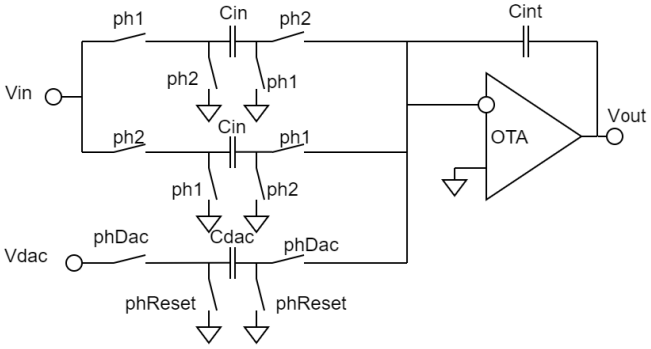

Fig. 11. Integrator with reset circuit.

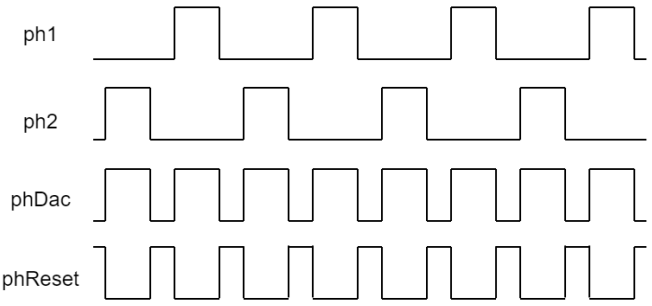

Fig. 12. Clock signal for integrator with reset circuit.

In Fig. 13 the dependence of the SNDR vs. the amplitude of the input signal for the proposed structure of ΣΔ modulator is presented for different values of the sampling capacitors mismatch. It can be seen that SNDR does not decrease when the capacitance mismatch of the input capacitors is present.

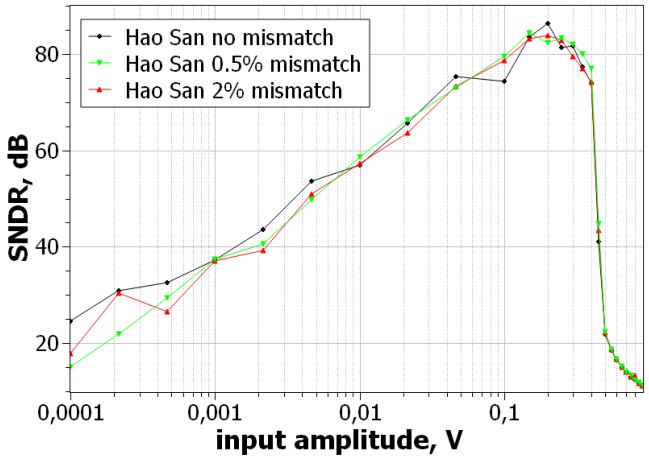

Fig. 13. SNDR vs. the amplitude of the input signal for the proposed structure of ΣΔ modulator for different values of the mismatch of the sampled capacitors.

Table 1 summarizes the values of maximum SNDR, number of switches, total capacity for discussed structures.

TABLE I. COMPARISON OF THE STRUCTURES

Structure	Max. SNDR, dB	Number of switches	Total capacitance, pF
Second-order ΣΔ modulator	67.5	20	9.6
Second-order ΣΔ modulator using Hao San structure	69.3	28	14.5
Double-sampling 2nd order ΣΔ modulator	71.9	32	8.0
Double-sampling 2nd order ΣΔ modulator using Hao San structure	83.4	40	24.5

V. CONCLUSIONS

The structure of a double-sampling modulator proposed in this paper can overcome both the problem of mismatch of the sampling capacitor and the problem of OTA distortion. Thus, it can achieve an SNDR value higher than in the conventional structure. A modified integrator circuit requires a less number of switches than the conventional one which helps to save chip area. The circuit was simulated in 180 nm CMOS using the Cadence Virtuoso software. At a clock frequency of 1 MHz and an OSR of 128, the proposed circuit consumes 3.4mA and shows an SNDR value of 83.4 dB.

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