CSE 436 - Introduction to Digital Integrated Circuits Assignment 1 Report

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1 Problem Definition

The goal of this assignment is to design and simulate fundamental CMOS logic gates, specifically a CMOS Inverter, a 2-input NAND, and a 2-input NOR gate. Using the Magic Layout tool, we will create layout designs for each circuit, which will then be extracted to SPICE format. By conducting simulations with SPICE, we aim to verify the functional correctness of these designs under TSMC 0.25µm technology parameters.

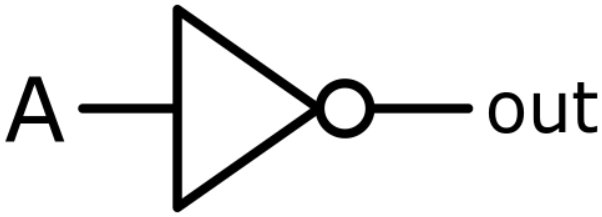


Figure 1: CMOS Inverter Layout

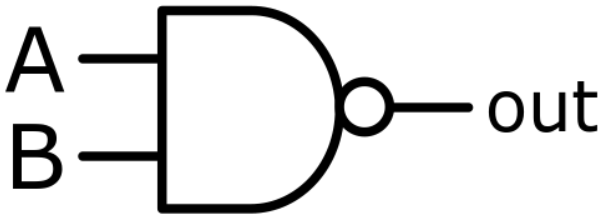


Figure 2: 2-Input NAND Gate Layout

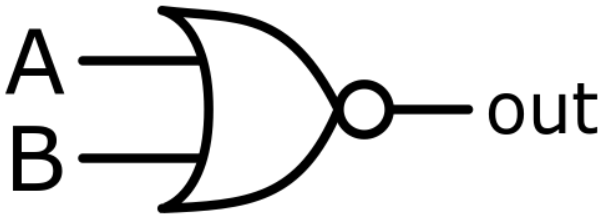


Figure 3: 2-Input NOR Gate Layout

2 Design Plan

In this section, we will outline the design plan for each CMOS logic gate.

2.1 CMOS Inverter

The CMOS inverter consists of one NMOS and one PMOS transistor. The PMOS transistor is placed in the n-well at the top and the NMOS transistor below it. The source of the PMOS is connected to VDD, while the source of the NMOS is connected to GND. The drains of both transistors are connected to form the output, and the input is provided through the gate.

Input	Output
0	1
1	0

Table 1: Truth Table for CMOS Inverter

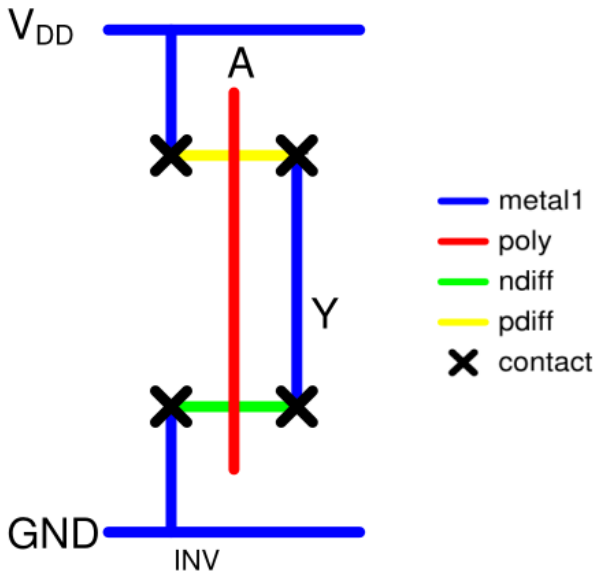


Figure 4: Stick Diagram for CMOS Inverter

2.2 2-Input NAND Gate

The 2-input NAND gate requires two NMOS transistors in series and two PMOS transistors in parallel. The PMOS transistors are placed in parallel in the n-well, and the NMOS transistors are arranged in series. The output is taken from the drains of both PMOS and NMOS pairs. The inputs, A and B, are applied to the gates of the PMOS and NMOS transistors.

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Table 2: Truth Table for 2-input NAND Gate

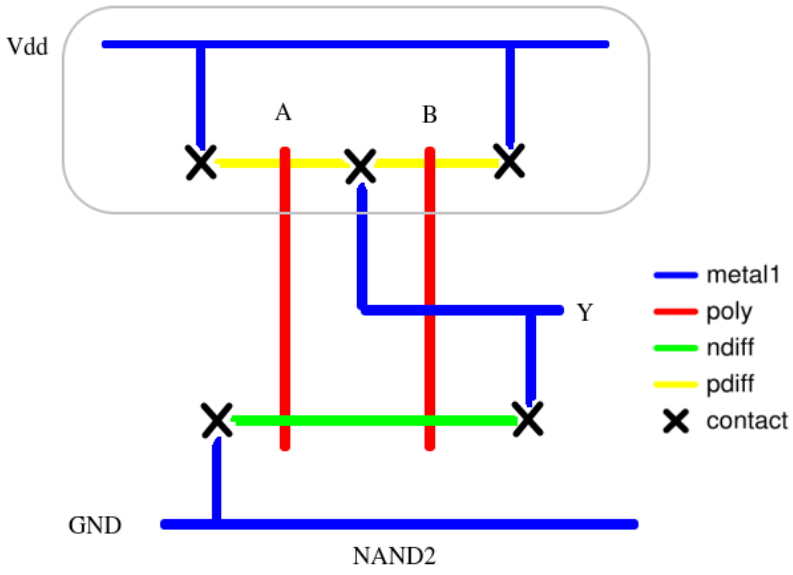


Figure 5: Stick Diagram for 2-input NAND Gate

2.3 2-Input NOR Gate

The 2-input NOR gate consists of two NMOS transistors in parallel and two PMOS transistors in series. The PMOS transistors are arranged in series in the n-well, while the NMOS transistors are placed in parallel. The drains are connected to form the output, and the inputs, A and B, are applied to the gates.

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Table 3: Truth Table for 2-input NOR Gate

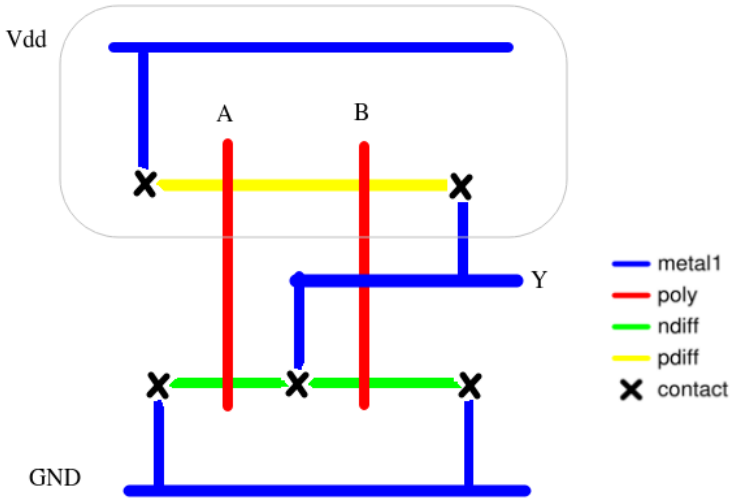


Figure 6: Stick Diagram for 2-input NOR Gate

3 Implementation and Analysis

This section describes the steps taken to design, extract, and simulate the layouts of CMOS Inverter, 2-input NAND, and 2-input NOR gates.

3.1 Magic Layout Setup

Before beginning the layout design, Magic was configured for TSMC 0.25µm technology using the following command:

```
magic -T SCN5M_DEEP.12.TSMC
```

The width-to-length ratios for the transistors were set according to the assignment specifications: NMOS W/L = $4\lambda/2\lambda$, PMOS W/L = $8\lambda/2\lambda$. The height of each cell was fixed at 100λ to ensure uniformity across designs.

3.2 Layout Design Process

The layout designs for each gate were created in Magic following CMOS logic design principles. Below are visuals of the design approach for each gate.

3.2.1 CMOS Inverter

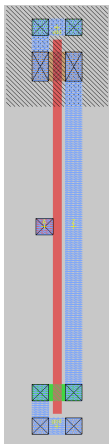


Figure 7: Magic Layout for CMOS Inverter

3.2.2 2-Input NAND Gate

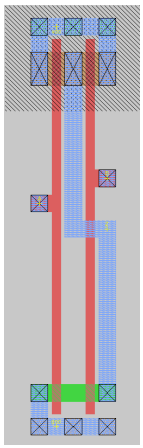


Figure 8: Magic Layout for 2-input NAND Gate

3.2.3 2-Input NOR Gate

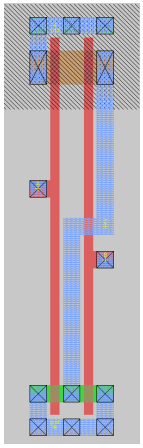


Figure 9: Magic Layout for 2-input NOR Gate

3.3 SPICE Extraction

After completing each layout, the next step was to extract the circuit's netlist for SPICE simulation. The following commands were used in Magic to extract the netlist:

```
: extract do all
: extract all
: ext2spice cthresh 0.001
: ext2spice rthresh 1
: ext2spice merge none
: ext2spice extresist off
: ext2spice
```

These commands produced a SPICE file (.spice) containing the extracted netlist of each design, which was then prepared for simulation.

3.4 SPICE File Modifications

To simulate each circuit, technology-specific parameters and power definitions were added to the SPICE files. At the top of each SPICE file, the TSMC 0.25µm model was included:

```
.include tsmc_cmos025
.model nfet NMOS
.model pfet PMOS
```

Power supply and input signal definitions for the inverter were added as follows:

```
Vdd vdd 0 2.5V
VinA A gnd PULSE(0 2.5 0ns 10ns 10ns 20ns 40ns)
VinB B gnd PULSE(0 2.5 0ns 5ns 10ns 20ns 40ns) -> added for NAND and NOR gates
CL Z 0 1fF
.TRAN 1ns 100ns
```

3.5 SPICE Simulation

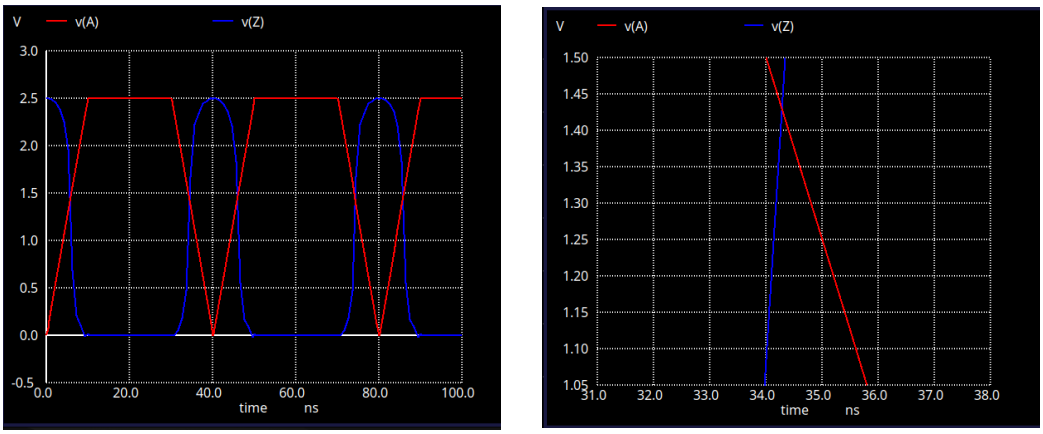
The SPICE simulations were conducted to verify the correctness of each circuit. Each SPICE file was loaded into the simulator (ngspice) with the command:

```
source gate.spice
run
```

Input A and B (just A for Inverter) and output (Z) voltages were plotted on the same graph to analyze the behavior over time:

```
.plot V(A) V(Z) -> Inverter
.plot V(A) V(B) V(Z) -> NAND2, NOR2
```

3.5.1 Inverter Simulation Analysis



(a) (b)

Figure 10: SPICE Simulation Results for Inverter

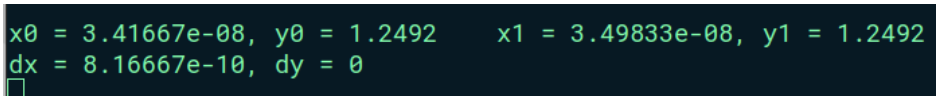


Figure 11: Delay at 1.25V of Inverter

To analyze the delay in a 0-2.5V inverter circuit, we specifically examined the timing difference at 1.25V.We measured the voltage transitions and determined the exact time interval between the points where the input and output signals reached 1.25V.

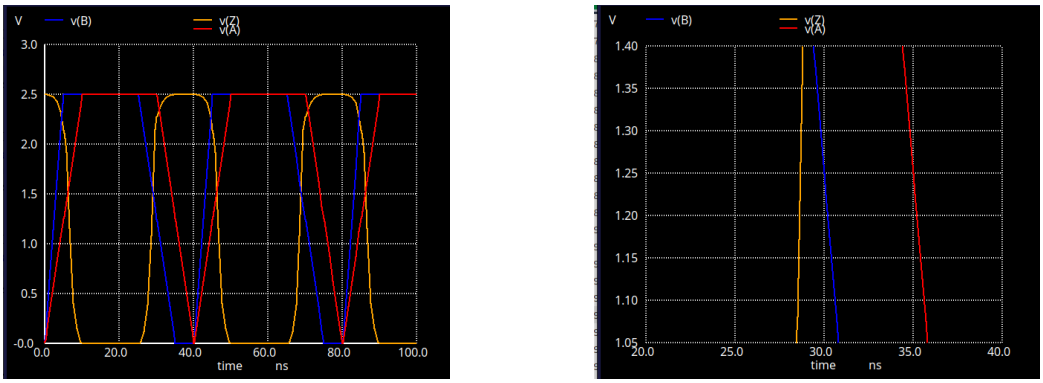
- **Input signal at 1.25V:**
  - $x_0 = 3.41667 \times 10^{-8}\,\mathrm{s}$
  - $y_0 = 1.2492\,\mathrm{V}$
- **Output signal at 1.25V:**
  - $x_1 = 3.49833 \times 10^{-8}\,\mathrm{s}$
  - $y_1 = 1.2492\,\mathrm{V}$

The delay, represented by Δt, was calculated as follows:

$$\Delta t = x_1 - x_0 = 3.49833 \times 10^{-8} - 3.41667 \times 10^{-8} = 8.16667 \times 10^{-10}\,\mathrm{s}$$

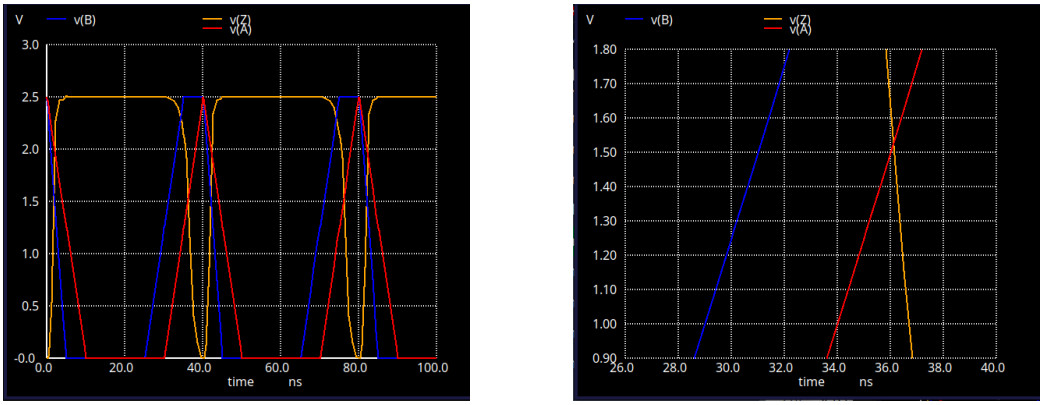
Thus, the measured delay at the 1.25V transition is approximately **816.67 ps**.

3.5.2 NAND2 Simulation Analysis



(a) (b)

Figure 12: SPICE Simulation Results for NAND2



(a) (b)

Figure 13: SPICE Simulation Results for NAND2
(With Different Initial Pulse Values)

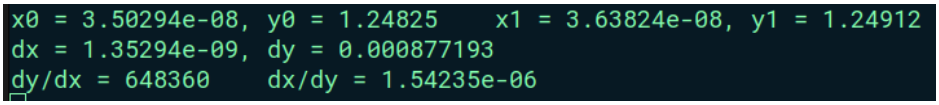


Figure 14: Delay at 1.25V of NAND2

To analyze the delay in a 0-2.5V NAND gate circuit, we specifically examined the timing difference at 1.25V for the input signal that was closest to the transition point. Since the 2-input NAND gate experiences state changes based on the inputs, the delay was measured for the input responsible for subsequently driving the change in output Z.

We measured the voltage transitions and determined the exact time interval between the points where the selected input and the output signals reached 1.25V.

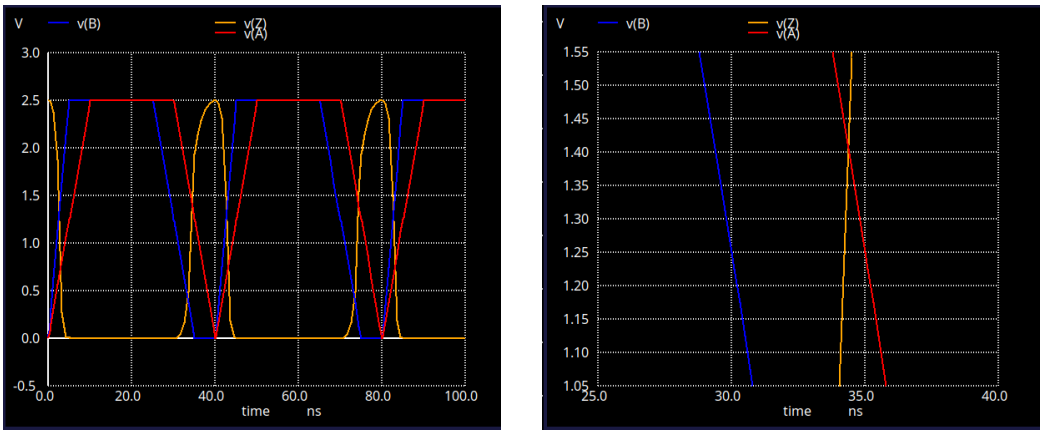
- Input signal at 1.25V (closest transition):
  - $x_0 = 3.50294 \times 10^{-8}$ s
  - $y_0 = 1.24825$ V
- Output signal at 1.25V:
  - $x_1 = 3.63824 \times 10^{-8}$ s
  - $y_1 = 1.24912$ V

The delay, represented by Δt, was calculated as follows:

$$\Delta t = x_1 - x_0 = 3.63824 \times 10^{-8} - 3.50294 \times 10^{-8} = 1.35294 \times 10^{-9} \text{ s}$$

Thus, the measured delay at the 1.25V transition is approximately **1.35294 ns**.

3.5.3 NOR2 Simulation Analysis



(a) (b)

Figure 15: SPICE Simulation Results for NOR2

```
ngspice 3 ->
x0 = 3.4225e-08, y0 = 1.25    x1 = 3.4975e-08, y1 = 1.25
dx = 7.5e-10, dy = 0
```

Figure 16: Delay at 1.25V of NOR2

To analyze the delay in a 0-2.5V NOR gate circuit, we specifically examined the timing difference at 1.25V for the input signal. Since the 2-input NOR gate experiences state changes based on its inputs, the delay was measured for the input responsible for subsequently driving the change in output Z.

We measured the voltage transitions and determined the exact time interval between the points where the selected input and the output signals reached 1.25V.

- Input signal at 1.25V:
  - $x_0 = 3.4225 \times 10^{-8}$ s
  - $y_0 = 1.25$ V
- Output signal at 1.25V:
  - $x_1 = 3.4975 \times 10^{-8}$ s
  - $y_1 = 1.25$ V

The delay, represented by Δt, was calculated as follows:

$$\Delta t = x_1 - x_0 = 3.4975 \times 10^{-8} - 3.4225 \times 10^{-8} = 7.5 \times 10^{-10} \text{ s}$$

Thus, the measured delay at the 1.25V transition is approximately **750 ps**.