1	Stackup - Impadence -Trace Width

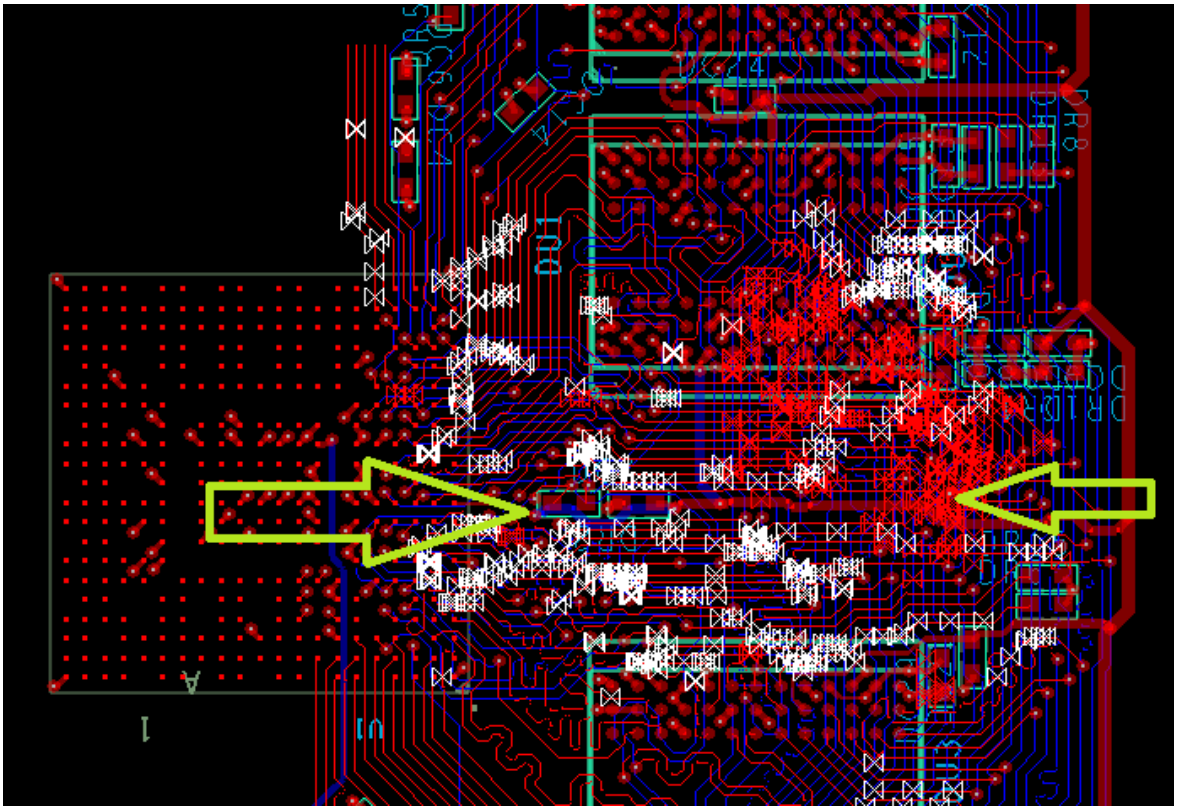
Total layers:	4
Board thickness:	1.6 mm +/- 10%
PCB material:	Typical FR4
Surface finish:	ENIG(化学镍金)

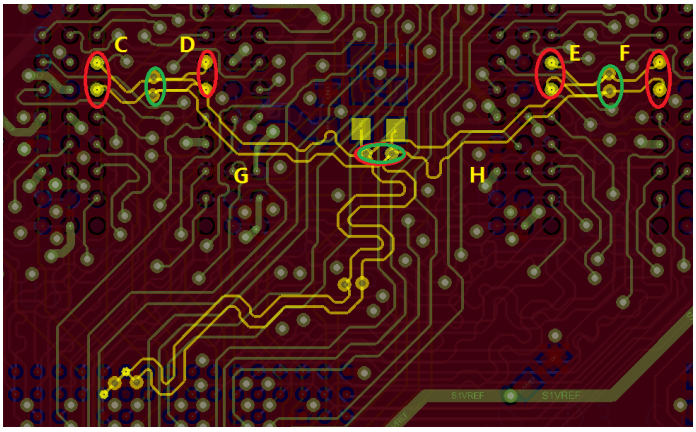
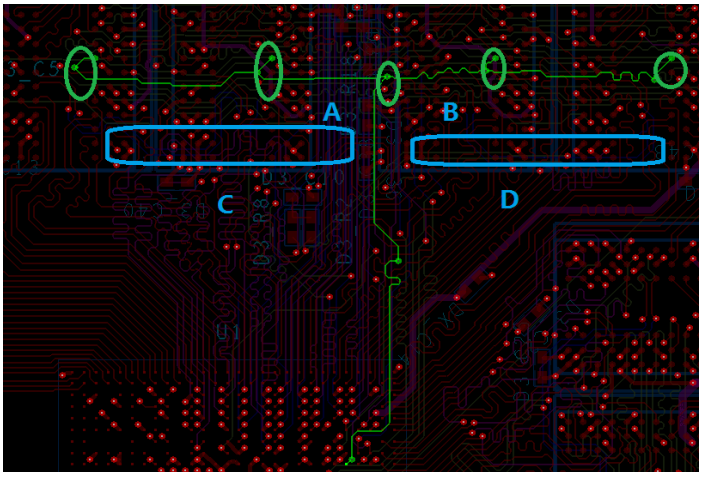
Stackup Control Table

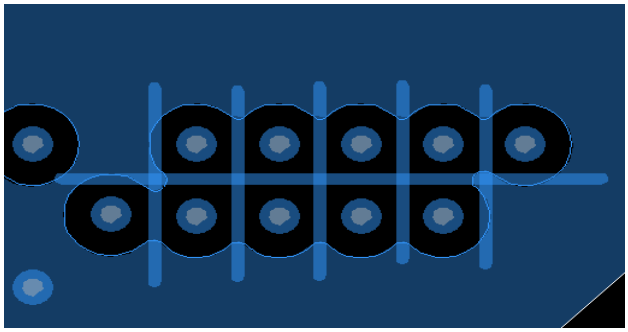
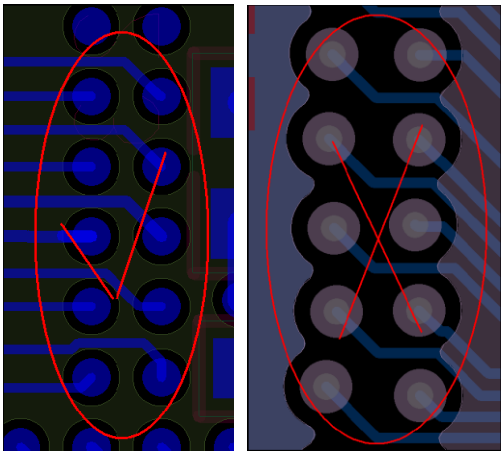
--	Stackup Structure				Impedance Requirements			
Layer	Type	Thickness (mil)		Dk(with Sim Z0)	Impedance spec (Ohms)	Reference layer	Width/space (mil)	Sim Z0(Ohms)
	solder mask	0.5	SM	4.25				
1	TOP	1.6	0.3oz+plating		50±10%	2	4	52.18
					90±10%	2	4.5/7.5	90.03
					100±10%	2	3.8/8.7	98.5
	prepreg	2.9		4				
2	GND	1.2	1.0oz					
	core	50.0		4.5				
3	VCC	1.2	1.0oz					
	prepreg	2.9		4				
4	BOTTOM	1.6	0.3oz+plating		50±10%	3	4	52.18
					90±10%	3	4.5/7.5	90.03
					100±10%	3	3.8/8.7	98.5
	solder mask	0.5	SM	4.25				
	Board thickness:	62.4						

2	走线宽度
	单端：4mil。
	差分：3.8/8.7mil。
	电源和地Fanout线宽：≥8mil。

3	间距
	单端：数据线与线的间距（Air Gap）≥8mil 地址控制线的间距大部分（Air Gap）≥8mil,小部分间距>=6mil,此部分主要集中于T点处，见下图

	
	差分线：到其他网络走线间距≥12mil。
	电源与地：到其他网络走线的间距≥15mil。
	VREF：到其他网络走线的间距≥15mil。
	BGA区域里：线与线4mil；线与SMD PIN 4mil；线与过孔4mil。
4	**拓扑**
	DQ：点对点
	DQS、DQSB：点对点
	对于时钟： C,D,E,F < 500mil， C - D < +/- 50mil， E - F < +/- 50mil， G,H < 800mil， G - H < +/- 50mil。

	
	对于地址控制： |A-B|<=50mil，|C-D|<=50mil。 
5	**等长**
	DQ0-7：相对于DQS0、DQSB0做等长，误差范围为≤90mil。 DQ8-15：相对于DQS1、DQSB1做等长，误差范围为≤90mil。 DQ16-23：相对于DQS2、DQSB2做等长，误差范围为≤90mil。 DQ24-31：相对于DQS3、DQSB3做等长，误差范围为≤90mil。
	DQSx、DQSBx: 相对于CK/CKB信号做等长，误差范围为≤900mil。
	Ax、BAx、CAS、RAS、WE、CSx、ODTx、CKEx： 相对于CK/CKB信号做等长，误差范围为≤800mil。
	DQSx与DQSBx等长，等长误差范围为≤10mil。 CK与CKB等长，等长误差范围为≤10mil。
	信号线做等长时要考虑过孔长度的影响
6	**电源、地平面**

	平面比较完整，调整好过孔的位置、间距，减少对电源、地平面的破坏。平面断开处用走线连接 
	电源、地平面同时也是信号的参考层要求，不能有信号线的参考层被割断的现象 
7	**滤波电容：**
	对于单面布局：尽量靠近电源PIN放置，每个电容至少各一个电源过孔和地过孔。

1. Declaration

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