Allwinner Technology

A33 Datasheet

Quad-Core Mobile Application Processor

Version 1.2

Jan. 20, 2015

REVISION HISTORY

Version	Date	Description
1.0	May.21, 2014	Initial release version
1.1	Sep 22,2014	Modify GPIO Multiplexing Functions
1.2	Jan 20,2015	Modify feature and block diagram

DECLARATION

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1. OVERVIEW

The Allwinner A33 is a remarkably power-efficient quad-core mobile application processor that based on ARM Cortex™-A7 CPU together with Mali400MP2 GPU architecture. It also outperforms its competitors in terms of total system cost, and enables excellent user experience without compromising the battery life.

Main features of A33 include:
CPU architecture: A33 is based on quad-core Cortex™-A7 CPU architecture to deliver superior system performance as well as optimized battery life experience, in that Cortex™-A7 is the most power efficient CPU core ARM's ever developed;
Graphic: A33 adopts the extensively implemented and technically mature Mali400MP2 GPU to provide end users with optimal experience in web browsing, video playback and games; OpenGL ES 2.0 and OpenVG 1.1 standards are supported;
Video Engine: A33 supports high-definition 1080P video processing, and supports various mainstream video standards such as H.264, VP8, MPEG 1/2/4, JPEG/MJPEG, etc;
Display: A33 supports CPU/RGB/LVDS LCD interface up to 1280x800 resolution. Four-lane MIPI DSI (Display Serial Interface) is integrated as well, supporting MIPI DSI V1.01 and MIPI D-PHY V1.00;
Image: A33 supports a parallel CMOS sensor interface up to 5M resolution.

Thanks to its advanced system design and outstanding software optimization, the A33 is capable of providing top-notch system performance with long-lasting battery life experience: in addition to its energy-efficient Cortex™-A7 CPU architecture, advanced fabrication process, video acceleration hardware, DVFS technology support and high system integration, A33 also features a unique Talking Standby Mode where the processor can be inactive during voice calls to provide end users with ultra-long battery life experience. Additionally, Allwinner A33 features high system integration with a wide range of integrated I/Os like 4-lane MIPI DSI, LVDS, USB OTG,USB HOST, SD/MMC, I2S/PCM, thus significantly reducing system components required in design to simplify product design and reduce total system costs.

2. FEATURE

2.1. CPU Architecture

The quad-core A33 platform is based on ARM's Cortex™-A7 CPU architecture.

- ARMv7 ISA standard instruction set plus Thumb-2 and Jazeller RCT
- NEON with SIMD and VFPv4 support
- Support hardware virtualization
- Support LPAE
- Integrated 32KB L1 instruction cache and 32KB L1 data cache for each CPU
- Shared 512KB L2 cache
- Support DVFS with independent power domain

2.2. GPU Architecture

- ARM Mali400MP2 GPU
- Support OpenGL ES 2.0 / OpenVG 1.1 standard

2.3. Memory Subsystem

Boot ROM

- Support system boot from Raw NAND, eMMC , SPI Nor Flash, SD/TF card
- Support system code download through USB OTG

SDRAM

- Support 2GB address space
- Support 16-bit bus width
- Compatible with JEDEC standard DDR3/DDR3L SDRAM
- Clock frequency up to 667MHz
- Support Memory Dynamic Frequency Scale
- Support two ranks
- Support 16 address signal lines and 3 bank signal lines

NAND Flash

- Comply to ONFI 2.3 and Toggle 1.0
- Up to 64-bit ECC per 512 bytes or 1024 bytes
- 8-bit Raw NAND flash controller sharing pin with eMMC
- Up to 2 CE and 2 RB signals
- Support SLC/MLC/TLC NAND and EF-NAND
- Support SDR/ONFI DDR/Toggle DDR NAND

SD/MMC Interface

- Up to three SD/MMC controllers
- Comply to eMMC standard specification V4.41, SD physical layer specification V2.0, SDIO card specification V2.0
- 1-bit or 4-bit data bus transfer mode for SD and SDIO cards up to 50MHz
- 1-bit,4-bit or 8-bit data bus transfer mode for MMC cards up to 50MHz in SDR modes

2.4. System Peripheral

Timer
- Support two timers: clock source can be switched over 24MHz and 32768Hz
- Support two 33-bit AVS counters
- Support one 64-bit system counter from 24MHz
- Support watchdog to generate reset signal or interrupts

High Speed Timer
- Clock source is fixed to AHB1, and the pre-scale ranges from 1 to 16
- Support one 56-bit counter

RTC
- Timer,Calendar,Alarm
- Support full clock features: second/minute/hour/day/month/year(with leap year)
- Support 32768Hz clock fanout

GIC
- Support 16 SGIs, 16 PPIs and 128 SPIs
- Support ARM architecture security extensions
- Support ARM architecture virtualization extensions
- Support single processor and multiprocessor environments

DMA
- 8-channel DMA
- Support data width of 8/16/32 bits
- Support linear and IO address modes
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

CCU
- 11 PLLs
- 24MHz oscillator, a 32768Hz oscillator and an on-chip RC oscillator
- Support clock gating control for individual components
- Clock generation, clock division, clock output

PWM
- Up to 2 PWM outputs
- Support cycle mode and pulse mode
- The pre-scale is from 1 to 16

Security System
- Support Symmetrical Algorithm: AES, DES, TDES(3DES)
- Support Hash Algorithm:SHA-1, MD5
- Support 160-bits hardware PRNG with 175-bits seed
- Support ECB, CBC, CTR modes for DES/3DES
- Support ECB, CBC, CTR, CTS modes for AES
- Support 128-bits, 192-bits and 256-bits key size for AES
- 32-words RX FIFO and 32-words TX FIFO for high speed application
- Support CPU mode and DMA mode

2.5. Display Subsystem

Display Engine

- Four movable layers, each layer size up to 2048x2048 pixels
- Ultra-Scaling engine
  -- 4-tap scale filter in horizontal and vertical
  -- Support input size up to 2048x2048 resolution and output size up to 1280x1280 resolution
- Support multiple image input formats: 1/2/4/8-bpp mono/palette,16/24/32-bpp color, YUV444/420/422/ 411
- Support alpha blending/color key/gamma
- Support output color correction:luminance/hue/saturation,etc
- Support Saturation Enhancement and Dynamic Range Control
- Support real time write back function

Video Output

- Support RGB/CPU/LVDS LCD interface up to 1280x800 resolution
- Integrated 4-lane MIPI DSI interface up to 1280x800 resolution
  -- Support MIPI DSI V1.01 and D-PHY V1.00
  -- Support command mode and video mode (non-burst mode with sync pulses, non-burst mode with sync event and burst mode)
  -- Support pixel format:RGB888,RGB666,loosely RGB666 and RGB565
- Dither function from RGB666/RGB565 to RGB888

2.6. Video Engine

Video Decoding

- Support video playback up to 1920x1080@60ps
- Support multi-format video playback, including MPEG1/2, MPEG4 SP/ASP GMC, WMV9/VC1, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP8, JPEG/MJPEG, etc

Video Encoding

- Support H.264 HP video encoding up to 1920x1080@60fps
- JPEG baseline: picture size up to 4080x4080
- Support Alpha blending
- Support thumb generation
- 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio

2.7. Video Input

CSI

- Support parallel camera sensor
- Support 8bit CCIR656 protocol
- Maximum still capture resolution to 5M
- Maximum video capture resolution to 1080p@30fps

2.8. Audio Subsystem

Analog Audio Codec

- Support stereo audio DAC
  -- Up to 100dB SNR
  -- 8KHz to 192KHz DAC sample rate
- Stereo audio ADC

-- Up to 96dB SNR
-- 8KHz ~ 48KHz ADC sample rate
- Support four analog audio inputs
-- Two microphone differential inputs for main mic and headphone mic
-- One differential phone input for modem
-- One stereo line-in input for FM
- Support two analog audio outputs
- -- One stereo or differential capless headphone output
- -- One differential earpiece output
- Support talking standby mode, where the application processor remains inactive during voice call application
- Support Dynamic Range Controller adjusting the DAC playback output(DRC)
- Support Automatic Gain Control adjusting the ADC recording output(AGC)
- Two PCM interface connected with BB and BT

Digital Audio
- Support two I2S/PCM compliant digital audio interfaces for modem and BT
- I2S or PCM configured by software
- Support 3 I2S Data formats: Standard I2S,Left Justified and Right Justified
- I2S supports 2 channels output and 2 channels input
- PCM supports 8/16-bit word length, 8-bit u-law and A-law compress sample
- Sample rate from 8KHz to 192KHz
- Support 16,20,24bits audio data resolutions
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive

2.9. External Peripherals

USB 2.0 OTG
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
- Support High-Speed (HS, 480-Mbps) and Full-Speed (FS, 12-Mbps) in Device mode
- Support up to 10 user-configurable endpoints for Bulk, Isochronous, Control and Interrupt
- Support the embedded DMA

USB Host
- EHCI/OHCI-compliant hosts
- USB2.0 PHY and HSIC
- Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps) Device
- An internal DMA Controller for data transfer with memory

KEYADC
- 6-bit resolution
- Support single key, normal key and continuous key

UART
- Five UART controllers
- FIFO size up to 64 bytes
- Support speed up to 3MHz
- Compliant with industry-standard 16550 UARTs
- Support Infrared Data Association(IrDA) 1.0 SIR

SPI
- One SPI controller
- Master/Slave configurable
- Full-duplex synchronous serial interface
- Two 64-Bytes FIFO for SPI-TX and SPI-RX operation

- DMA-based or interrupt-based operation
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable

TWI

- Up to four TWIs(Two Wire Interface) controllers
- One dedicated TWI for CSI
- Support Standard mode(up to 100K bps) and Fast mode(up to 400K bps)
- Master/Slave configurable
- Allows 10-bits addressing transactions

RSB™(Reduced Serial Bus)

- Speed up to 20MHz with lower power consumption
- Support Push-Pull bus
- Support Host mode
- Support multiple devices
- Programmable output delay of CD signal
- Parity check for address and data transmission

2.10. Package

- FBGA 282 balls,0.80mm ball pitch, 14 x 14 x 1.4-mm

3. BLOCK DIAGRAM

The following figure shows the block diagram of A33 processor.

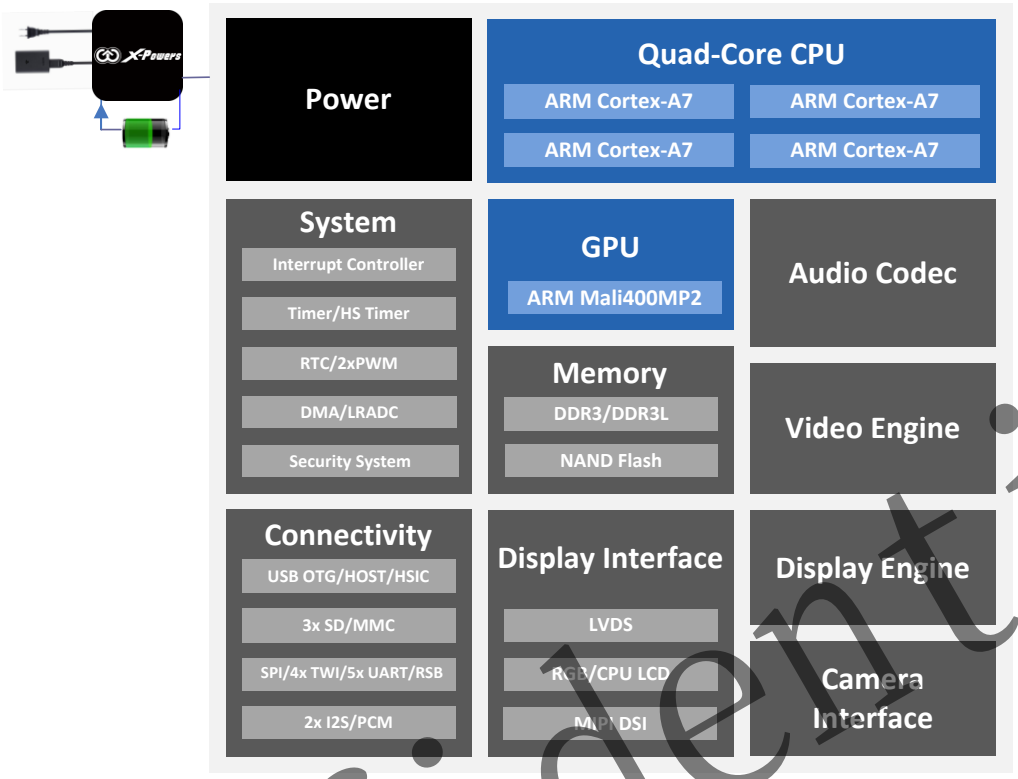


Figure 3-1. A33 Block Diagram

4. PIN DESCRIPTION

4.1. PIN CHARACTERISTICS

Table 4-1 lists the characteristics of A33 Pins from seven aspects:BALL#,Pin Name,Default Function,Type,Reset State,Default Pull Up/Down,and Buffer Strength.

NOTES

1) **Default Function** defines the default function of each pin,especially for pins with multiplexing functions;
2) **Type** defines the signal direction: I (Input), O (Output), I/O(Input/Output), OD(Open Drain),A (Analog),AI(Analog Input),AO(Analog Output),AIO (Analog Input/Output),P (Power), G (Ground);
3) **Reset State** defines the state of the terminal at reset: Z for high-impedance ;
4) **Default Pull Up/Down** defines the presence of an internal pull up or pull down resister. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;
5) **Buffer Strength** defines drive strength of the associated output buffer. It is tested in the condition that VCC= 3.3V, strength=MAX;

Table 4-1. Pin Characteristics

Ball#	Pin Name©	Default Function©	Type©	Reset State©	Default Pull Up/Down©	Buffer Strength© (mA)
DRAM						
E4	DA0	DRAM	O	Z	-	-
D1	DA1	DRAM	O	Z	-	-
F2	DA2	DRAM	O	Z	-	-
H3	DA3	DRAM	O	Z	-	-
D2	DA4	DRAM	O	Z	-	-
F1	DA5	DRAM	O	Z	-	-
A1	DA6	DRAM	O	Z	-	-
G4	DA7	DRAM	O	Z	-	-
B1	DA8	DRAM	O	Z	-	-
F4	DA9	DRAM	O	Z	-	-
E2	DA10	DRAM	O	Z	-	-
C2	DA11	DRAM	O	Z	-	-
E1	DA12	DRAM	O	Z	-	-
F3	DA13	DRAM	O	Z	-	-
C1	DA14	DRAM	O	Z	-	-
E3	DA15	DRAM	O	Z	-	-
J3	DBA0	DRAM	O	Z	-	-
K4	DBA1	DRAM	O	Z	-	-
H4	DBA2	DRAM	O	Z	-	-
M3	DCAS	DRAM	O	Z	-	-
G1	DCK	DRAM	O	Z	-	-
G2	DCKB	DRAM	O	Z	-	-
J4	DCKE	DRAM	O	Z	-	-
N7	DCKE1	DRAM	O	Z	-	-
N3	DCS	DRAM	O	Z	-	-
N5	DCS1	DRAM	O	Z	-	-

Ball#	Pin Name[①]	Default Function[②]	Type[③]	Reset State[④]	Default Pull Up/Down[⑤]	Buffer Strength[⑥] (mA)
M1	DQ0	DRAM	I/O	Z	-	-
M2	DQ1	DRAM	I/O	Z	-	-
L1	DQ2	DRAM	I/O	Z	-	-
L2	DQ3	DRAM	I/O	Z	-	-
J1	DQ4	DRAM	I/O	Z	-	-
J2	DQ5	DRAM	I/O	Z	-	-
H1	DQ6	DRAM	I/O	Z	-	-
H2	DQ7	DRAM	I/O	Z	-	-
U3	DQ8	DRAM	I/O	Z	-	-
U1	DQ9	DRAM	I/O	Z	-	-
U2	DQ10	DRAM	I/O	Z	-	-
T2	DQ11	DRAM	I/O	Z		
R2	DQ12	DRAM	I/O	Z	-	-
P1	DQ13	DRAM	I/O	Z	-	-
P2	DQ14	DRAM	I/O	Z	-	-
N1	DQ15	DRAM	I/O	Z	-	-
T3	DQM1	DRAM	O	Z	-	-
N2	DQM0	DRAM	O	Z	-	-
R1	DQS1	DRAM	I/O	Z	-	-
T1	DQS1B	DRAM	I/O	Z	-	-
K2	DQS0	DRAM	I/O	Z	-	-
K1	DQS0B	DRAM	I/O	Z	-	-
L3	DODT	DRAM	O	Z	-	-
L7	DODT1	DRAM	O	Z	-	-
L4	DRAS	DRAM	O	Z	-	-
G3	DRST	DRAM	O	Z	-	-
M4	DVREF	DRAM	P	Z	-	-
K3	DWE	DRAM	O	Z	-	-
R3	DZQ	DRAM	A	Z	-	-
H5，J5，K5，L5，H6，J6	VCC-DRAM	POWER	P	-	-	-
P3	VDD-DLL	POWER	P	-	-	-
GPIO B						
G17	PB0	GPIO	I/O	Z	NO PULL	20
G16	PB1	GPIO	I/O	Z	NO PULL	20
F17	PB2	GPIO	I/O	Z	NO PULL	20
F16	PB3	GPIO	I/O	Z	NO PULL	20
G14	PB4	GPIO	I/O	Z	NO PULL	20
G15	PB5	GPIO	I/O	Z	NO PULL	20
F14	PB6	GPIO	I/O	Z	NO PULL	20
F15	PB7	GPIO	I/O	Z	NO PULL	20
GPIO C						

Ball#	Pin Name[0]	Default Function[2]	Type[0]	Reset State[0]	Default Pull Up/Down[0]	Buffer Strength[0] (mA)
D12	PC0	GPIO	I/O	Z	NO PULL	20
C12	PC1	GPIO	I/O	Z	NO PULL	20
C11	PC2	GPIO	I/O	Z	NO PULL	20
D11	PC3	GPIO	I/O	Z	Pull-up	20
B11	PC4	GPIO	I/O	Z	Pull-up	20
C10	PC5	GPIO	I/O	Z	NO PULL	20
D10	PC6	GPIO	I/O	Z	Pull-up	20
A12	PC7	GPIO	I/O	Z	Pull-up	20
A11	PC8	GPIO	I/O	Z	NO PULL	20
B10	PC9	GPIO	I/O	Z	NO PULL	20
A10	PC10	GPIO	I/O	Z	NO PULL	20
B9	PC11	GPIO	I/O	Z	NO PULL	20
A9	PC12	GPIO	I/O	Z	NO PULL	20
B8	PC13	GPIO	I/O	Z	NO PULL	20
A8	PC14	GPIO	I/O	Z	NO PULL	20
B7	PC15	GPIO	I/O	Z	NO PULL	20
A7	PC16	GPIO	I/O	Z	NO PULL	20
GPIO D						
R12	PD2	GPIO	I/O	Z	NO PULL	20
P12	PD3	GPIO	I/O	Z	NO PULL	20
R11	PD4	GPIO	I/O	Z	NO PULL	20
P11	PD5	GPIO	I/O	Z	NO PULL	20
R10	PD6	GPIO	I/O	Z	NO PULL	20
P10	PD7	GPIO	I/O	Z	NO PULL	20
R9	PD10	GPIO	I/O	Z	NO PULL	20
P9	PD11	GPIO	I/O	Z	NO PULL	20
R8	PD12	GPIO	I/O	Z	NO PULL	20
P8	PD13	GPIO	I/O	Z	NO PULL	20
R7	PD14	GPIO	I/O	Z	NO PULL	20
P7	PD15	GPIO	I/O	Z	NO PULL	20
U11	PD18	GPIO	I/O	Z	NO PULL	20
T11	PD19	GPIO	I/O	Z	NO PULL	20
U10	PD20	GPIO	I/O	Z	NO PULL	20
T10	PD21	GPIO	I/O	Z	NO PULL	20
U9	PD22	GPIO	I/O	Z	NO PULL	20
T9	PD23	GPIO	I/O	Z	NO PULL	20
U8	PD24	GPIO	I/O	Z	NO PULL	20
T8	PD25	GPIO	I/O	Z	NO PULL	20
U7	PD26	GPIO	I/O	Z	NO PULL	20
T7	PD27	GPIO	I/O	Z	NO PULL	20
M11，N11	VCC-PD	POWER	P	-	-	-
GPIO E						

Ball#	Pin Name[①]	Default Function[②]	Type[③]	Reset State[④]	Default Pull Up/Down[⑤]	Buffer Strength[⑥] (mA)
C5	PE0	GPIO	I/O	Z	NO PULL	20
D5	PE1	GPIO	I/O	Z	NO PULL	20
C6	PE2	GPIO	I/O	Z	NO PULL	20
D6	PE3	GPIO	I/O	Z	NO PULL	20
A6	PE4	GPIO	I/O	Z	NO PULL	20
B6	PE5	GPIO	I/O	Z	NO PULL	20
A5	PE6	GPIO	I/O	Z	NO PULL	20
B5	PE7	GPIO	I/O	Z	NO PULL	20
A4	PE8	GPIO	I/O	Z	NO PULL	20
B4	PE9	GPIO	I/O	Z	NO PULL	20
A3	PE10	GPIO	I/O	Z	NO PULL	20
B3	PE11	GPIO	I/O	Z	NO PULL	20
A2	PE12	GPIO	I/O	Z	NO PULL	20
B2	PE13	GPIO	I/O	Z	NO PULL	20
C3	PE14	GPIO	I/O	Z	NO PULL	20
D3	PE15	GPIO	I/O	Z	NO PULL	20
C4	PE16	GPIO	I/O	Z	NO PULL	20
D4	PE17	GPIO	I/O	Z	NO PULL	20
GPIO F						
D9	PF0	GPIO	I/O	Z	NO PULL	20
C9	PF1	GPIO	I/O	Z	NO PULL	20
D8	PF2	GPIO	I/O	Z	NO PULL	20
C8	PF3	GPIO	I/O	Z	NO PULL	20
D7	PF4	GPIO	I/O	Z	NO PULL	20
C7	PF5	GPIO	I/O	Z	NO PULL	20
GPIO G						
A15	PG0	GPIO	I/O	Z	NO PULL	20
B15	PG1	GPIO	I/O	Z	NO PULL	20
A14	PG2	GPIO	I/O	Z	NO PULL	20
B14	PG3	GPIO	I/O	Z	NO PULL	20
A13	PG4	GPIO	I/O	Z	NO PULL	20
B13	PG5	GPIO	I/O	Z	NO PULL	20
A17	PG6	GPIO	I/O	Z	NO PULL	20
B17	PG7	GPIO	I/O	Z	NO PULL	20
B16	PG8	GPIO	I/O	Z	NO PULL	20
A16	PG9	GPIO	I/O	Z	NO PULL	20
C17	PG10	GPIO	I/O	Z	NO PULL	20
C16	PG11	GPIO	I/O	Z	NO PULL	20
C15	PG12	GPIO	I/O	Z	NO PULL	20
C14	PG13	GPIO	I/O	Z	NO PULL	20
GPIO H						
D17	PH0	GPIO	I/O	Z	NO PULL	20

Ball#	Pin Name[©]	Default Function[©]	Type[©]	Reset State[©]	Default Pull Up/Down[©]	Buffer Strength[©] (mA)
D16	PH1	GPIO	I/O	Z	NO PULL	20
D15	PH2	GPIO	I/O	Z	NO PULL	20
D14	PH3	GPIO	I/O	Z	NO PULL	20
D13	PH4	GPIO	I/O	Z	NO PULL	20
C13	PH5	GPIO	I/O	Z	NO PULL	20
E17	PH6	GPIO	I/O	Z	NO PULL	20
E16	PH7	GPIO	I/O	Z	NO PULL	20
E15	PH8	GPIO	I/O	Z	NO PULL	20
E14	PH9	GPIO	I/O	Z	NO PULL	20
GPIO L						
P16	PL0	GPIO	I/O	Z	Pull-up	20
P15	PL1	GPIO	I/O	Z	Pull-up	20
U14	PL2	GPIO	I/O	Z	NO PULL	20
T14	PL3	GPIO	I/O	Z	NO PULL	20
R14	PL4	GPIO	I/O	Z	NO PULL	20
P14	PL5	GPIO	I/O	Z	NO PULL	20
U13	PL6	GPIO	I/O	Z	NO PULL	20
T13	PL7	GPIO	I/O	Z	NO PULL	20
R13	PL8	GPIO	I/O	Z	NO PULL	20
P13	PL9	GPIO	I/O	Z	NO PULL	20
U12	PL10	GPIO	I/O	Z	NO PULL	20
T12	PL11	GPIO	I/O	Z	NO PULL	20
System Control						
N14	NMI	-	I	Z	-	-
P17	RESET	-	I	Z	-	-
Audio Codec						
M16	MIC1N	-	A	-	-	-
M17	MIC1P	-	A	-	-	-
N16	MIC2N	-	A	-	-	-
N17	MIC2P	-	A	-	-	-
J15	LINEINR	-	A	-	-	-
H15	LINEINL	-	A	-	-	-
K16	VRA1	-	A	-	-	-
K17	VRA2	-	A	-	-	-
L17	VRP	-	A	-	-	-
L16	AVCC	-	P	-	-	-
N15	PHONEOUTN	-	A	-	-	-
M15	PHONEOUTP	-	A	-	-	-
K15	PHONEINN	-	A	-	-	-
L15	PHONEINP		A	-	-	-
J14	HBIAS		A	-	-	-
K14	MBIAS	-	A	-	-	-

Ball#	Pin Name[9]	Default Function[2]	Type[8]	Reset State[8]	Default Pull Up/Down[5]	Buffer Strength[5] (mA)
H13	AGND	-	G	-	-	-
J16	HPOUTR	-	A	-	-	-
J17	HPOUTL	-	A	-	-	-
H14	HPCOM	-	A	-	-	-
H16	HPCOMFB	-	A	-	-	-
H17	HPVCCBP	-	P	-	-	-
K13	HPVCCIN	-	P	-	-	-
USB						
T16	USB-DM0	-	A	-	-	-
T17	USB-DP0	-	A	-	-	-
U16	USB-DM1	-	A	-	-	-
U17	USB-DP1	-	A	-	-	-
L12	VCC-USB	-	P	-	-	-
HSIC						
U15	HSIC-DAT	-	A	-	-	-
T15	HSIC-STR	-	A	-	-	-
N12	VCC-HSIC	-	P	-	-	-
ADC						
L14	LRADC0	-	A	-	-	-
DSI						
U5	DSI-CKN	-	A	-	-	-
T5	DSI-CKP	-	A	-	-	-
R4	DSI-D0N	-	A	-	-	-
R5	DSI-D1N	-	A	-	-	-
U6	DSI-D2N	-	A	-	-	-
R6	DSI-D3N	-	A	-	-	-
P4	DSI-D0P	-	A	-	-	-
P5	DSI-D1P	-	A	-	-	-
T6	DSI-D2P	-	A	-	-	-
P6	DSI-D3P	-	A	-	-	-
N6	VCC-DSI	-	P	-	-	-
CLOCK						
R17	X32KIN	-	A	-	-	-
R16	X32KOUT	-	A	-	-	-
R15	X32KFOUT	-	A	-	-	-
M13	RTCVIO	-	A	-	-	-
M12	VCC-RTC	-	P	-	-	-
U4	X24MI	-	A	-	-	-
T4	X24MOUT	-	A	-	-	-
M5	VCC-PLL	-	P	-	-	-
Power						
M8	VCC-EFUSE	-	P	-	-	-

Ball#	Pin Name[①]	Default Function[②]	Type[③]	Reset State[④]	Default Pull Up/Down[⑤]	Buffer Strength[⑥] (mA)
M14	VDD-CPUS	-	P	-	-	-
E5,E6,E7,F5,F6,F7,G5,G6	VDD-CPU	-	P	-	-	-
E8,E9,E10,K6,L6,M6,M7, N8,N9,N10	VDD-SYS	-	P	-	-	-
E11,E12,F11,F12,G12	VCC-IO	-	P	-	-	-
N4,F8,F9,F10,G7,G8,G9, G10,G11,H7,H8,H9,H10, H11,H12,J7,J8,J9,J10,J11 ,J12,K7,K8,K9,K10,K11,K 12,L8,L9,L10,L11,M9, M10	GND	-	G	-	-	-

4.2. GPIO MULTIPLEXING FUNCTIONS

The following table provides a description of the A33 GPIO multiplexing functions.

Table 4-2. Multiplexing Functions

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function 2	Function3	Function 4
PB0	GPIO	I/O	DIS	Z	UART2-TX	UART0-TX	PB-EINT0
PB1		I/O	DIS	Z	UART2-RX	UART0-RX	PB-EINT1
PB2		I/O	DIS	Z	UART2-RTS	-	PB-EINT2
PB3		I/O	DIS	Z	UART2-CTS	-	PB-EINT3
PB4		I/O	DIS	Z	PCM0-SYNC	AIF2-SYNC	PB-EINT4
PB5		I/O	DIS	Z	PCM0-BCLK	AIF2-BCLK	PB-EINT5
PB6		I/O	DIS	Z	PCM0-DOUT	AIF2-DOUT	PB-EINT6
PB7		I/O	DIS	Z	PCM0-DIN	AIF2-DIN	PB-EINT7
PC0	GPIO	I/O	DIS	Z	NAND-WE	SPI0-MOSI	-
PC1		I/O	DIS	Z	NAND-ALE	SPI0-MISO	-
PC2		I/O	DIS	Z	NAND-CLE	SPI0-CLK	-
PC3		I/O	DIS	Pull-up	NAND-CE1	SPI0-CS	-
PC4		I/O	DIS	Pull-up	NAND-CE0	-	-
PC5		I/O	DIS	Z	NAND-RE	SDC2-CLK	-
PC6		I/O	DIS	Pull-up	NAND-RB0	SDC2-CMD	-
PC7		I/O	DIS	Pull-up	NAND-RB1	-	-
PC8		I/O	DIS	Z	NAND-DQ0	SDC2-D0	-
PC9		I/O	DIS	Z	NAND-DQ1	SDC2-D1	-
PC10		I/O	DIS	Z	NAND-DQ2	SDC2-D2	-
PC11		I/O	DIS	Z	NAND-DQ3	SDC2-D3	-
PC12		I/O	DIS	Z	NAND-DQ4	SDC2-D4	-
PC13		I/O	DIS	Z	NAND-DQ5	SDC2-D5	-
PC14		I/O	DIS	Z	NAND-DQ6	SDC2-D6	-
PC15		I/O	DIS	Z	NAND-DQ7	SDC2-D7	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function 2	Function3	Function 4
PC16		I/O	DIS	Z	NAND-DQS	SDC2-RST	-
PD2	GPIO	I/O	DIS	Z	LCD-D2	SDC1-CLK	-
PD3		I/O	DIS	Z	LCD-D3	SDC1-CMD	-
PD4		I/O	DIS	Z	LCD-D4	SDC1-D0	-
PD5		I/O	DIS	Z	LCD-D5	SDC1-D1	-
PD6		I/O	DIS	Z	LCD_D6	SDC1-D2	-
PD7		I/O	DIS	Z	LCD-D7	SDC1-D3	-
PD10		I/O	DIS	Z	LCD-D10	UART1-TX	-
PD11		I/O	DIS	Z	LCD-D11	UART1-RX	-
PD12		I/O	DIS	Z	LCD-D12	UART1-RTS	-
PD13		I/O	DIS	Z	LCD-D13	UART1-CTS	-
PD14		I/O	DIS	Z	LCD-D14	-	-
PD15		I/O	DIS	Z	LCD-D15	-	-
PD18		I/O	DIS	Z	LCD-D18	LVDS-VP0	-
PD19		I/O	DIS	Z	LCD-D19	LVDS-VN0	-
PD20		I/O	DIS	Z	LCD-D20	LVDS-VP1	-
PD21		I/O	DIS	Z	LCD-D21	LVDS-VN1	-
PD22		I/O	DIS	Z	LCD-D22	LVDS-VP2	-
PD23		I/O	DIS	Z	LCD-D23	LVDS-VN2	-
PD24		I/O	DIS	Z	LCD-CLK	LVDS-VPC	-
PD25		I/O	DIS	Z	LCD-DE	LVDS-VNC	-
PD26		I/O	DIS	Z	LCD-HSYNC	LVDS-VP3	-
PD27		I/O	DIS	Z	LCD-VSYNC	LVDS-VN3	-
PE0	GPIO	I/O	DIS	Z	CSI-PCLK	-	-
PE1		I/O	DIS	Z	CSI-MCLK	-	-
PE2		I/O	DIS	Z	CSI-HSYNC	-	-
PE3		I/O	DIS	Z	CSI-VSYNC	-	-
PE4		I/O	DIS	Z	CSI-D0	-	-
PE5		I/O	DIS	Z	CSI-D1	-	-
PE6		I/O	DIS	Z	CSI-D2	-	-
PE7		I/O	DIS	Z	CSI-D3	-	-
PE8		I/O	DIS	Z	CSI-D4	-	-
PE9		I/O	DIS	Z	CSI-D5	-	-
PE10		I/O	DIS	Z	CSI-D6	-	-
PE11		I/O	DIS	Z	CSI-D7	-	-
PE12		I/O	DIS	Z	CSI-SCK	TWI2-SCK	-
PE13		I/O	DIS	Z	CSI-SDA	TWI2-SDA	-
PE14		I/O	DIS	Z	-	-	-
PE15		I/O	DIS	Z	-	-	-
PE16		I/O	DIS	Z	-	-	-
PE17		I/O	DIS	Z	-	-	-
PF0	GPIO	I/O	JTAG	Z	SDC0-D1	JTAG-MS1	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function 2	Function3	Function 4
PF1		I/O	JTAG	Z	SDC0-D0	JTAG-DI1	-
PF2		I/O	DIS	Z	SDC0-CLK	UART0-TX	-
PF3		I/O	JTAG	Z	SDC0-CMD	JTAG-DO1	-
PF4		I/O	DIS	Z	SDC0-D3	UART0-RX	-
PF5		I/O	JTAG	Z	SDC0-D2	JTAG-CK1	-
PG0	GPIO	I/O	DIS	Z	SDC1-CLK	-	PG-EINT0
PG1		I/O	DIS	Z	SDC1-CMD	-	PG-EINT1
PG2		I/O	DIS	Z	SDC1-D0	-	PG-EINT2
PG3		I/O	DIS	Z	SDC1-D1	-	PG-EINT3
PG4		I/O	DIS	Z	SDC1-D2	-	PG-EINT4
PG5		I/O	DIS	Z	SDC1-D3	-	PG-EINT5
PG6		I/O	DIS	Z	UART1-TX	-	PG-EINT6
PG7		I/O	DIS	Z	UART1-RX	-	PG-EINT7
PG8		I/O	DIS	Z	UART1-RTS	-	PG-EINT8
PG9		I/O	DIS	Z	UART1-CTS	-	PG-EINT9
PG10		I/O	DIS	Z	PCM1-SYNC	AIF3-SYNC	PG-EINT10
PG11		I/O	DIS	Z	PCM1-BCLK	AIF3-BCLK	PG-EINT11
PG12		I/O	DIS	Z	PCM1-DOUT	AIF3-DOUT	PG-EINT12
PG13		I/O	DIS	Z	PCM1-DIN	AIF3-DIN	PG-EINT13
PH0	GPIO	I/O	DIS	Z	PWM0	-	-
PH1		I/O	DIS	Z	PWM1	-	-
PH2		I/O	DIS	Z	TWI0-SCK	-	-
PH3		I/O	DIS	Z	TWI0-SDA	-	-
PH4		I/O	DIS	Z	TWI1-SCK	-	-
PH5		I/O	DIS	Z	TWI1-SDA	-	-
PH6		I/O	DIS	Z	SPI0-CS	UART3-TX	-
PH7		I/O	DIS	Z	SPI0-CLK	UART3-RX	-
PH8		I/O	DIS	Z	SPI0-MOSI	UART3-RTS	-
PH9		I/O	DIS	Z	SPI0-MISO	UART3-CTS	-
PL0	GPIO	I/O	DIS	Pull-up	S-RSB-SCK	S-TWI-SCK	S-PL-EINT0
PL1		I/O	DIS	Pull-up	S-RSB-SDA	S-TWI-SDA	S-PL-EINT1
PL2		I/O	DIS	Z	S-UART-TX	-	S-PL-EINT2
PL3		I/O	DIS	Z	S-UART-RX	-	S-PL-EINT3
PL4		I/O	DIS	Z	S-JTAG-MS	-	S-PL-EINT4
PL5		I/O	DIS	Z	S-JTAG-CK	-	S-PL-EINT5
PL6		I/O	DIS	Z	S-JTAG-DO	-	S-PL-EINT6
PL7		I/O	DIS	Z	S-JTAG-DI	-	S-PL-EINT7
PL8		I/O	DIS	Z	S-TWI-SCK	-	S-PL-EINT8
PL9		I/O	DIS	Z	S-TWI-SDA	-	S-PL-EINT9
PL10		I/O	DIS	Z	S-PWM	-	S-PL-EINT10
PL11		I/O	DIS	Z	-	-	S-PL-EINT11

4.3. DETAILED PIN/SIGNAL DESCRIPTION

Table 4-3 shows the detailed function of every pin/signal based on the different interface.

Table 4-3. Detailed Pin Description

Pin/Signal Name	Description	Type
DRAM		
DQ[15:0]	DRAM bidirectional data line to the memory device	I/O
DQS[1:0]	DRAM active-high bidirectional data strobes to the memory device	I/O
DQSB[1:0]	DRAM active-low bidirectional data strobes to the memory device	I/O
DCK	DRAM active-high clock signal to the memory device	O
DCKB	DRAM active-low clock signal to the memory device	O
DCKE[1:0]	DRAM clock enable signal to the memory device for two chip select	O
DA[15:0]	DRAM address signal to the memory device	O
DWE	DRAM write enable strobe to the memory device	O
DCAS	DRAM column address strobe to the memory device	O
DRAS	DRAM row address strobe to the memory device	O
DCS[1:0]	DRAM chip select signal to the memory device	O
DBA[2:0]	DRAM bank address signal to the memory device	O
DODT[1:0]	DRAM On-Die Termination output signal for two chip select	O
DRST	DRAM reset signal to the memory device	O
DZQ	DRAM ZQ Calibration	A
DVREF	DRAM Reference Input	P
VCC-DRAM	DRAM Power Supply	P
VDD-DLL	DLL Power Supply	P
System Control		
NMI	Non-Maskable Interrupt	I
RESET	Reset Signal	I
USB		
USB-DM0	USB2.0 Differential Data Signal	AIO
USB-DP0		AIO
USB-DM1	USB2.0 Differential Data Signal	AIO
USB-DP1		AIO
VCC-USB	USB2.0 Analog Voltage	P
HSIC		
VCC12-HSIC	HSIC Voltage	P
HSIC-STR	USB HSIC Strobe Signal	AIO
HSIC-DAT	USB HSIC Data Signal	AIO
ADC		
LRADC0	Key Input	AI
Audio Codec		
PHONEOUTN	Phone Differential Output Signal	AO
PHONEOUTP		AO

Pin/Signal Name	Description	Type
PHONEINN	Phone Differential Input Signal	AI
PHONEINP		AI
MICINN[2:1]	Microphone Differential Input Signal	AI
MICINP[2:1]		AI
LINEINR	Line-in Right Input	AI
LINEINL	Line-in Left Input	AI
HBIAS	Analog Headphone Bias	AO
MBIAS	Analog Microphone Bias	AO
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
VRP	Reference Voltage	AO
AVCC	Analog Voltage	P
AGND	Analog GND	G
HPOUTR	Headphone Right Channel Output	AO
HPOUTL	Headphone Light Channel Output	AO
HPVCCIN	Headphone Voltage Supply	P
HPVCCBP	Headphone Voltage Bypass	AO
HPCOM	HPCOM Output	AO
HPCOMFB	HPCOM Feedback Input	AI
HPBP	HPVCC Bypass Output	AO
DSI		
DSI-DP0	MIPI DSI Differential Signal	AIO
DSI-DN0		AIO
DSI-DP1	MIPI DSI Differential Signal	AO
DSI-DN1		AO
DSI-DP2	MIPI DSI Differential Signal	AO
DSI-DN2		AO
DSI-DP3	MIPI DSI Differential Signal	AO
DSI-DN3		AO
DSI-CKP	MIPI DSI Differential Clock	AO
DSI-CKN		AO
VCC-DSI	MIPI DSI Voltage	P
CLOCK		
X32KIN	Clock Input Of 32KHz Crystal	AI
X32KOUT	Clock Output Of 32KHz Crystal	AO
X32KFOUT	32KHz Feedback Output	OD
VCC-RTC	RTC Voltage	P
RTC-VIO	Internal LDO Output	P
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
VCC-PLL	PLL Analog Voltage	P
SD /MMC(x=[2:0])		
SDCx-CMD	SDx/MMCx/SDIOx Command Signal	I/O

Pin/Signal Name	Description	Type
SDCx-CLK	SDx/MMCx/SDIOx Clock Signal	O
SDC0-D[3:0]	SD0/MMC0/SDIO0 Data Signal	I/O
SDC1-D[3:0]	SD1/MMC1/SDIO1 Data Signal	I/O
SDC2-D[7:0]	SD2/MMC2/SDIO2 Data Signal	I/O
SDC2-RST	SD2/MMC2/SDIO2 Reset Signal	O
NAND FLASH		
NAND-DQ[7:0]	NAND Flash Data Signal	I/O
NAND-DQS	NADN Flash Data Strobe Signal	I/O
NAND-WE	NAND Flash Write Enable	O
NAND-RE	NAND Flash Read Enable	O
NAND-ALE	NAND Flash Address Latch Enable	O
NAND-CLE	NAND Flash Command Latch Enable	O
NAND-CE[1:0]	NAND Flash Chip Select [1:0]	O
NAND-RB[1:0]	NAND Flash Ready/Busy Bit	I
RSB		
S-RSB-SCK	RSB Clock Signal	O
S-RSB-SDA	RSB Data Signal	I/O
Interrupt		
PB-EINT[10:0]	GPIO B Interrupt	I
PG-EINT[13:0]	GPIO G Interrupt	I
S-PL-EINT[12:0]	GPIO L Interrupt	I
PWM		
S_PWM	Pulse Width Modulation output	O
PWM	Pulse Width Modulation output	O
LCD		
LCD0-D[23:0]	LCD Data Signal	O
LCD-CLK	LCD Clock Output	O
LCD-DE	LCD Data Enable	O
LCD-HSYNC	LCD Horizontal SYNC	O
LCD-VSYNC	LCD Vertical SYNC	O
LVDS		
LVDS-VP[3:0]	LVDS Differential Data Signal Output	AO
LVDS-VN[3:0]		AO
LVDS-VPC	LVDS Differential Clock Output	AO
LVDS-VNC		AO
PCM (x=[1:0])		
PCM0-SYNC	I2S/PCM SYNC	I/O
PCMx-CLK	I2S/PCM Clock	I/O
PCMx-DIN	I2S/PCM Data Input	I
PCMx-DOUT	I2S/PCM Data Output	O
CSI		
CSI-PCLK	CSI Pixel Clock	I
CSI-MCLK	CSI Master Clock	O

Pin/Signal Name	Description	Type
CSI-HSYNC	CSI Horizontal SYNC	I
CSI-VSYNC	CSI Vertical SYNC	I
CSI-D[7:0]	CSI Data Signal	I
CSI-SCK	CSI Control Clock Signal	I/O
CSI-SDA	CSI Control Data Signal	I/O
SPI		
SPI0-CS	SPI Chip Select Signal	I/O
SPI0-CLK	SPI Clock	I/O
SPI0-MOSI	SPI Mater Output ,Slave Input	I/O
SPI0-MISO	SPI Master Input ,Slave Output	I/O
UART (x=[3:0])		
UARTx-CTS	UART Data Clear to Send	I
UARTx-RTS	UART Data Request to Send	O
UARTx-TX	UART Data Transmit	O
UARTx-RX	UART Data Receive	I
S-UART-TX	UART Data Transmit	O
S-UART-RX	UART Data Receive	I
TWI (x=[2:0])		
TWIx-SCK	TWI Clock Signal	I/O
TWIx-SDA	TWI Data Signal	I/O
S-TWI-SCK	TWI Clock Signal	I/O
S-TWI-SDA	TWI Data Signal	I/O

5. ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Functional operation of the device at these or any other conditions beyond the absolute maximum ratings listed in Table 5-1 can cause permanent damage to the device.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	MIN	Max	Unit
T_{STG}	Storage Temperature	-40	125	°C
$I_{I/O}$	In/Out current for input and output	-40	40	mA
VCC-IO	Power Supply for I/O	-0.3	3.6	V
VDD-DLL	Power Supply for DLL	-0.3	2.75	V
VCC-DRAM	Power Supply for DDR3/DDR3L	-0.3	1.65	V
VCC-PLL	Power Supply for PLL	-0.3	3.6	V
VCC-RTC	Power Supply for RTC	-0.3	3.6	V
AVCC	Power Supply for Analog Part	-0.3	3.6	V
VCC-USB	Power Supply for USB	-0.3	3.6	V
VCC-DSI	Power Supply for MIPI-DSI	-0.3	3.6	V
VDD-CPU	Power Supply for CPU	-0.3	1.5	V
VDD-SYS	Power Supply for System	-0.3	1.5	V

5.2. RECOMMENDED OPERATING CONDITIONS

All A33 modules are used under the operating Conditions contained in Table 5-2.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
VCC-IO	Power Supply for I/O	1.7	1.8~3.3	3.6	V
VDD-DLL	Power Supply for DLL	2.35	2.5	2.65	V
VCC-DRAM	Power Supply for DDR3L	1.283	1.35	1.45	V
	Power Supply for DDR3	1.425	1.5	1.575	V
VCC-PLL	Power Supply for PLL	2.7	3.0	3.3	V
VCC-USB	Power Supply for USB	3.0	3.3	3.45	V
VCC-RTC	Power Supply for RTC	2.7	3.0	3.3	V
AVCC	Power Supply for Analog Part	2.7	3.0	3.3	V
VCC-DSI	Power Supply for MIPI-DSI	2.7	3.3	3.6	V
VDD-CPU	Power Supply for CPU	0.9	1.1	1.4	V
VDD-SYS	Power Supply for System	0.9	1.1	1.4	V

5.3. DC ELECTRICAL CHARACTERISTICS

Table 5-3 summarizes the DC electrical characteristics of A33.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7*VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3*VCC-IO	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ
R_{PD}	Input pull-down resistance	50	100	150	KΩ
V_{HYS}	Hysteresis Voltage	0.1 x VCC-IO	-	-	V
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

The A33 contains two oscillators: a 24MHz oscillator and a 32768Hz oscillator. Each oscillator requires a specific crystal. The A33 device operation requires the following two input clocks:

The 32768Hz frequency is used for low frequency operation.

The 24.000MHz frequency is used to generate the main source clock of the A33 device.

Table 5-4. 24MHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	50	uW
C_L	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
R_S	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–		pF
C_{SHUT}	Shunt capacitance	–	–		pF
R_{BIAS}	Internal bias resistor				MΩ

Table 5-5. 32768Hz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	32768	–	Hz

t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	50	uW
C_L	Equivalent Load capacitance	–	–	–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–	–	–	pF
R_S	Series Resistance(ESR)	–	–	–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–	–	pF
C_{SHUT}	Shunt capacitance	–	–	–	pF
R_{BIAS}	Internal bias resistor	–	–	–	MΩ

5.5. POWER ON AND POWER OFF SEQUENCE

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.Following figure 5-1 and figure 5-2 illustrate the power on and off sequence:

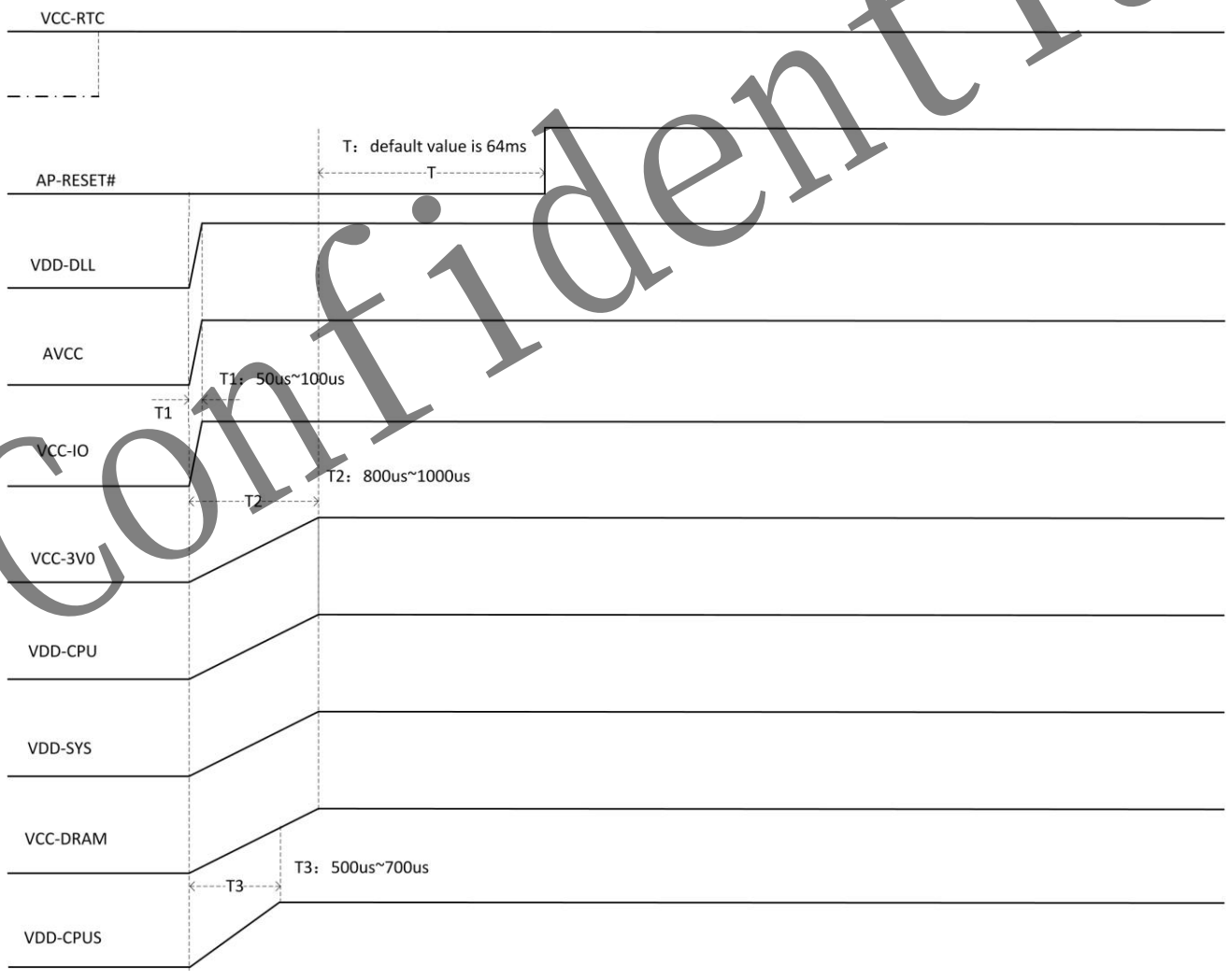


Figure 5-1. Power On Timing

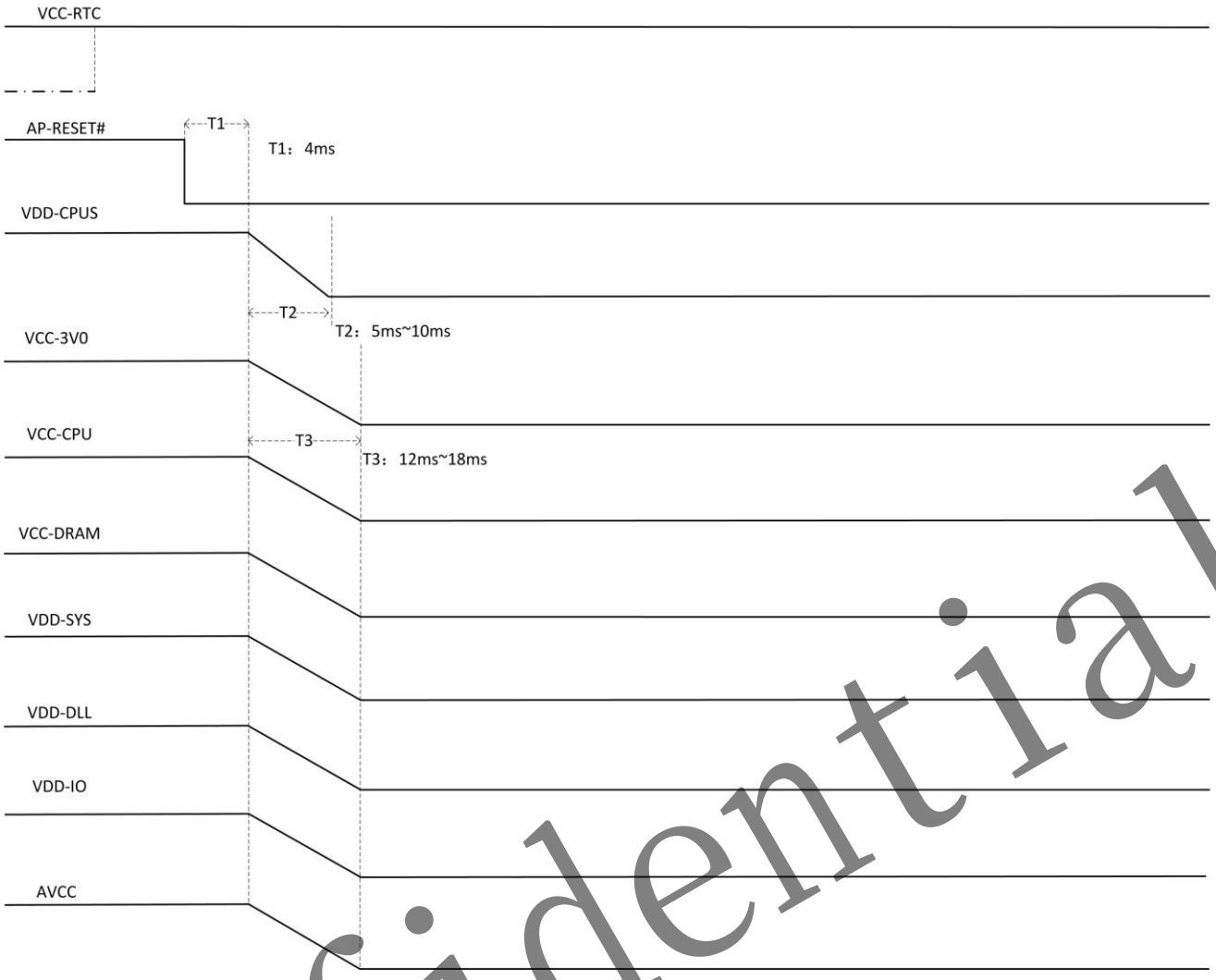


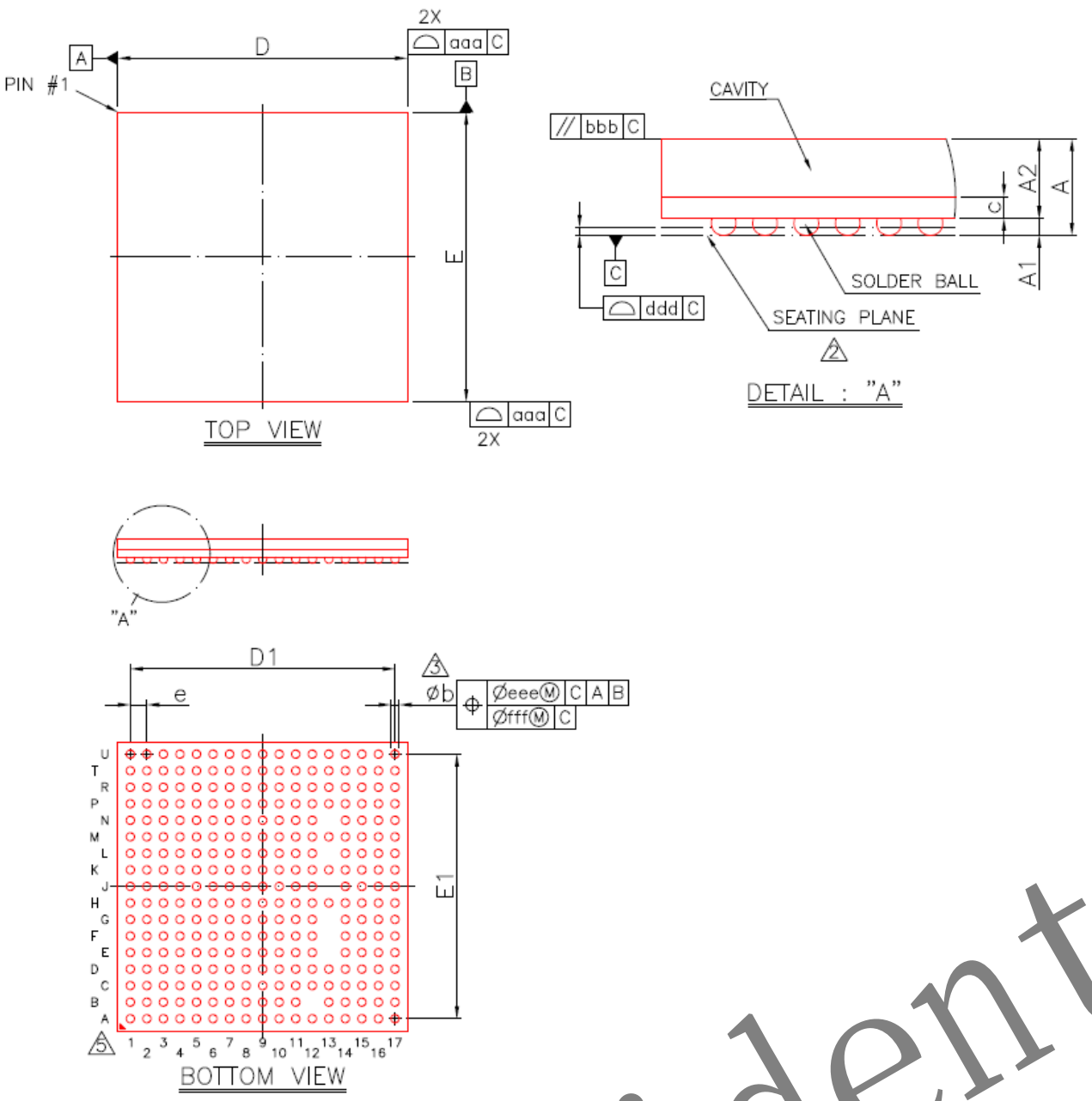
Figure 5-2. Power Down Timing

6. PIN ASSIGNMENT

6.1. PIN MAP

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	DA6	PE12	PE10	PE8	PE6	PE4	PC16	PC14	PC12	PC10	PC8	PC7	PG4	PG2	PG0	PG9	PG6	A
B	DA8	PE13	PE11	PE9	PE7	PE5	PC15	PC13	PC11	PC9	PC4		PG5	PG3	PG1	PG8	PG7	B
C	DA14	DA11	PE14	PE16	PE0	PE2	PF5	PF3	PF1	PC5	PC2	PC1	PH5	PG13	PG12	PG11	PG10	C
D	DA1	DA4	PE15	PE17	PE1	PE3	PF4	PF2	PF0	PC6	PC3	PC0	PH4	PH3	PH2	PH1	PH0	D
E	DA12	DA10	DA15	DA0	VDD-CPU	VDD-CPU	VDD-CPU	VDD-SYS	VDD-SYS	VDD-SYS	VCC-IO	VCC-IO		PH9	PH8	PH7	PH6	E
F	DA5	DA2	DA13	DA9	VDD-CPU	VDD-CPU	VDD-CPU	GND	GND	GND	VCC-IO	VCC-IO		PB6	PB7	PB3	PB2	F
G	DCK	DCKB	DRST	DA7	VDD-CPU	VDD-CPU	GND	GND	GND	GND	GND	VCC-IO		PB4	PB5	PB1	PB0	G
H	DQ6	DQ7	DA3	DBA2	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND	GND	AGND	HPCOM	LINEINL	HPCOMFB	HPVCCBP	H
J	DQ4	DQ5	DBA0	DCKE	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND	GND		HBIAS	LINEINR	HPOUTR	HPOUTL	J
K	DQS0B	DQS0	DWE	DBA1	VCC-DRAM	VDD-SYS	GND	GND	GND	GND	GND	GND	HPVCCIN	MBIAS	PHONEINN	VRA1	VRA2	K
L	DQ2	DQ3	DODT	DRAS	VCC-DRAM	VDD-SYS	DODT1	GND	GND	GND	GND	VCC-USB		LRADC0	PHONEINP	AVCC	VRP	L
M	DQ0	DQ1	DCAS	DVREF	VCC-PLL	VDD-SYS	VDD-SYS	VCC-EFUSE	GND	GND	VCC-PD	VCC-RTC	RTCVIO	VDD-CPUS	PHONEOUTP	MIC1N	MIC1P	M
N	DQ15	DQM0	DCS	GND	DCS1	VCC-DSI	DCKE1	VDD-SYS	VDD-SYS	VDD-SYS	VCC-PD	VCC-HSIC		NMI	PHONEOUTN	MIC2N	MIC2P	N
P	DQ13	DQ14	VDD-DLL	DSI-D0P	DSI-D1P	DSI-D3P	PD15	PD13	PD11	PD7	PD5	PD3	PL9	PL5	PL1	PL0	RESET	P
R	DQS1	DQ12	DZQ	DSI-D0N	DSI-D1N	DSI-D3N	PD14	PD12	PD10	PD6	PD4	PD2	PL8	PL4	X32KFOUT	X32KOUT	X32KIN	R
T	DQS1B	DQ11	DQM1	X24MOUT	DSI-CKP	DSI-D2P	PD27	PD25	PD23	PD21	PD19	PL11	PL7	PL3	HSIC-STR	USB-DM0	USB-DP0	T
U	DQ9	DQ10	DQ8	X24MIN	DSI-CKN	DSI-D2N	PD26	PD24	PD22	PD20	PD18	PL10	PL6	PL2	HSIC-DAT	USB-DM1	USB-DP1	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

6.2. PACKAGE DIMENSION



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.29	---	---	0.051
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D1	---	12.80	---	---	0.504	---
E1	---	12.80	---	---	0.504	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME			17/17			

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERENCE DOCUMENT : JEDEC MO-207

TITLE : 282LD TFBGA (14X14 mm) PACKAGE OUTLINE			
APPR.			
PE. (W/D,B/P,S/RB/G)		DWG NO.	
PD.		REV NO.	
QM.		DATE	
CHK.		DWG.	

COPY CONTROLLED	REV NO	DESCRIPTION	DATE		ALLWINNER TECH	SHT No.
	A	NEW ISSUE.				1/1

REV.A1

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