Self-Checking FSM Design with Observing only FSM Outputs

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Abstract

We deal with the problem of a self-checking FSM design with observing only FSM outputs. We suggest a special PLA description of the FSM behavior that is well suited for a practice. It is established that a factorized multilevel synthesis method applied to this PLA description and followed by the gate implementation provides observing only FSM outputs. We assume that a set of faults considered does not demand introducing additional FSM input lines. We also propose a mathematical tool that makes possible for any synthesis method applied to this special PLA description to clarify a possibility of observing only FSM outputs.

1. Introduction

When we deal with the problem of a self-checking FSM design we consider either a possibility to observe the values of state and output variables of the synchronous sequential circuit (SSC) that realizes FSM [1] or only the values of its output variables [2,3,4]. The latter is preferable as it decreases an overhead that we need for a checker. First such possibility to cut an overhead was pointed out in the paper [2] for a PLA implementation of special FSMs, namely, self-checking Microprogram Control Units and the usual PLA single stuck-at faults. Then in the paper [3] the novel architecture of a self-checking Control Unit (special FSM) design based on FPGA implementation was suggested. Here, also only the values of output variables were observed. In the papers [2,3] the authors assume that a probability of any multiple fault from a set of faults considered is negligible then their self-checking design with observing only FSM outputs is correct. It is standard practice to use the following assumption. Any next fault from a set of faults considered appears after the FSM working area with the foregoing fault has been exhausted. Then undetectable faults can accumulate in the SSC. They can affect the manifestation of a next fault when it appears.

If accumulating undetectable faults from a set considered does not affect the manifestation of a next fault from this set then we call such accumulating as undangerous.

In the paper [4] the authors first tried to study the problem of undangerous accumulating undetectable faults. They at the same time considered more vast class of faults and arbitrary FSMs in comparison with [2,3], in part, they added single stuck-at faults on the SSC input lines. Unfortunately, in this case the additional input variables of SSC are required.

Assume that we did not admit using the additional input variables having restricted a set of faults considered. Is it then possible self-checking design with observing only FSM output lines and undangerous accumulating undetectable faults from this set? This paper gives a positive answer. It is possible if we use a special PLA^{pm} description of the FSM behavior followed by a factorized multilevel synthesis method. PLA^{pm} is simpler then conventional PLA description [2,3] using for a self-checking design. PLA^{pm} is derived from the STG description of FSM after the same weight encoding FSM states followed by changing the 0-value of any state variable for don't care. Output states codes can be either (m,n)-codes or Berger codes.

In this paper we also suggest a mathematical tool that makes possible for any synthesis method applied to the PLA^{pm} description to clarify a possibility of observing only FSM outputs. For this aim we separated a special class of functional faults so called A, B-faults and researched their properties.

2. SSC self-checking design with observing only output lines

We propose to implement the self-checking FSM design using the basic scheme shown in Fig. 1.

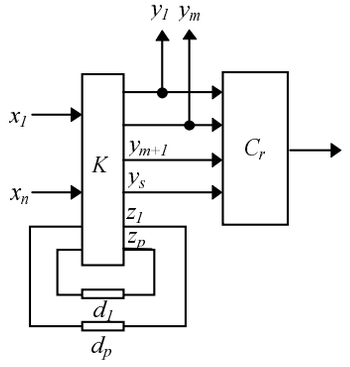

Figure 1. Basic Scheme

We have the STG description of the FSM behavior. After encoding states we obtain its PLA description. Using the multilevel synthesis method [5] followed by a gate implementation we obtain the combinational circuit *K*. This circuit is a combinational part of a synchronous sequential circuit (SSC). We consider single stuck-at faults at the gate poles and single stuck-at faults at the delay flip-flop poles. These latter can be reduced to the single stuck-at faults at the combinational circuit *K* input poles corresponding to the state variables of SSC. Call all faults considered as *V*.

Let the states of FSM be encoded with the codewords of the same weight and outputs be either encoded with the codewords of the same weight or Berger codewords. Then the STG description converts into the PLA description.

Change each 0-value state component from the products of PLA for the symbol "-" (don't care).

Notice this description as PLA^{pm} (Table 1).

Table 1

$x_1x_2x_3$	$z_1z_2z_3z_4$	$z_1z_2z_3z_4$	$y_1y_2y_3y_4y_5y_6y_7$
0 - -	1 - - -	1 0 0 0	0 0 0 1 0 1 1
- 0 -	1- - -	1 0 0 0	0 0 0 1 0 1 1
1 1 -	1- - -	0 1 0 0	1 0 0 1 0 1 0
- - 0	- 1 - -	0 1 0 0	0 0 1 1 0 0 1
- - 1	- 1 - -	0 0 1 0	1 0 1 1 0 0 0
1 0 -	- - 1 -	0 0 1 0	0 1 0 0 0 1 1
0 - -	- - 1 -	0 0 0 1	1 1 0 0 0 0 1
- 1 -	- - 1 -	0 0 0 1	1 1 0 0 0 0 1
- - 0	- - - 1	0 0 0 1	0 1 0 0 1 1 0
- - 1	- - - 1	1 0 0 0	1 1 0 0 1 0 0

Theorem 1. PLA^{pm} preserves the FSM behavior in its working area.

Let *F* be the system of Boolean function, represented by PLA^{pm} and α_1, α_2 be minterms of *F* represented by Boolean vectors of the length *(n+p)*. If for any components $\alpha_{1i}, \alpha_{2i}, i = \overline{(1,(n+p))}$, $\alpha_{1i} \le \alpha_{2i}$ then $\alpha_1 \le \alpha_2$ (010010≤011011).

The condition $\alpha_1 \overset{Z}{\le} \alpha_2$ means that for any component *i* corresponding to the variable from $\{z_1,\ldots,z_p\}$ $\alpha_{1i} \le \alpha_{2i}$ and for any component *j* corresponding to the variable from $\{x_1,\ldots,x_n\}$ $\alpha_{1j} = \alpha_{2j}$.

The system *F* is partially monotonous among *Z* variables if for any pair of Boolean vectors α_1, α so that $\alpha_1 \overset{Z}{\le} \alpha_2$ the condition $F(\alpha_1) \le F(\alpha)$ ($\beta_1 \le \beta_2$, $\beta_1 = F(\alpha_1)$, $\beta_2 = F(\alpha_2)$) takes place.

Theorem 2. PLA^{pm} represents the system *F* of partially monotonous Boolean function among the state variables.

Let F, F_2 be different systems of the same number of functions and variables. If for any α $F_1(\alpha) \le F_2(\alpha)$ then $F_1 \le F_2$, F_2 implicates F.

Introduce notations of A, B-faults.

Consider a partially monotonous among the state variables system *F* and a certain fault *w*. Let F^w be the system corresponding to this fault and F^w be also partially monotonous among the state variables. If $F^w \le F$ (*F* implicates F^w) call the fault as A-fault. If $F \le F^w$ (F^w implicates *F*) call the fault as B-fault.

We have established that if a set of faults consists of only A, B-faults and any next fault from the set appears after the FSM working area with the forgoing fault has been exhausted it is possible to observe only FSM outputs with undangerous accumulating undetectable faults.

We have also cleared up that PLA^{pm} description followed by the multilevel synthesis method [5] gives rise to the above mentioned set *V* of faults so that any fault $v \in V$ is either A-fault or B-fault.

Conclusion

We suggest a mathematical tool (notation A, B-faults and researching their properties) that makes possible for any synthesis methods applied to the PLA^{pm} description and the corresponding set of faults to clarify a possibility of observing only FSM outputs with undangerous accumulating undetectable faults. In this paper we deal with the multilevel synthesis method. We successfully employed the same way for direct PLA implementation of PLA^{pm} and factorized two-level synthesis method.

References

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