

MEMORIA

Memória de 4 GiB

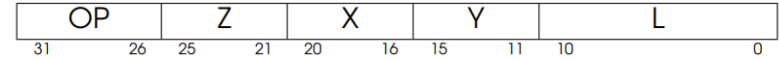
0x00000000	B_1	B_2	B_3	B_4
0x00000004	B_5	B_6	B_7	B_8
⋮	⋮	⋮	⋮	⋮
0xFFFFFFFF8	B_{n-7}	B_{n-6}	B_{n-5}	B_{n-4}
0xFFFFFFFFC	B_{n-3}	B_{n-2}	B_{n-1}	B_n

32 bits (4 bytes)
CUSTO
Capacidade × Custo × Latência

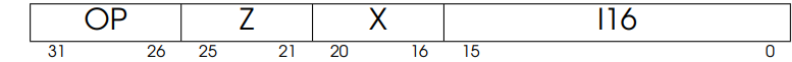
Tipo	Capacidade	Custo	Latência
Imediato	1 ↔ 3 bytes	-	-
SRAM	2 KiB ↔ 32 Mbit	≈US\$ 5.000 / GiB	0,20 ↔ 2 ns
DRAM	1 ↔ 16 GiB	≈US\$ 3 / GiB	≈10 ns

OPERATIONS

- ▶ Formato **U**(OP, Z, X, Y, L)
 - ▶ 6 bits para operação (OP)
 - ▶ 5 bits para operandos (Z, X, Y)
 - ▶ 11 bits para uso livre (L)



- ▶ Formato **F**(OP, Z, X, I16)
 - ▶ 6 bits para operação (OP)
 - ▶ 5 bits para operandos (Z, X)
 - ▶ 16 bits para imediato (I16)

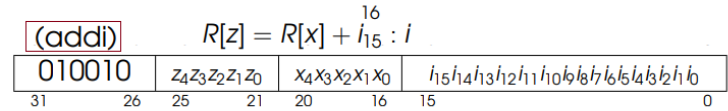


- ▶ Formato **S**(OP, I26)
 - ▶ 6 bits para operação (OP)
 - ▶ 26 bits para imediato (I26)

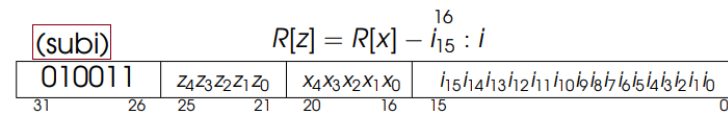


Tipo F:

ADIÇÃO IMEDIATA:



$R[z] = R[x] + i_{15:0}$
 $ZN \leftarrow (R[z] = 0)$
 $SN \leftarrow (R[z]_{31} = 1)$
 $OV \leftarrow (R[x]_{31} = i_{15}) \wedge (R[z]_{31} \neq R[x]_{31})$
 $CY \leftarrow (R[z]_{32} = 1)$



$R[z] = R[x] - i_{15:0}$
 $ZN \leftarrow (R[z] = 0)$
 $SN \leftarrow (R[z]_{31} = 1)$
 $OV \leftarrow (R[x]_{31} \neq i_{15}) \wedge (R[z]_{31} \neq R[x]_{31})$
 $CY \leftarrow (R[z]_{32} = 1)$

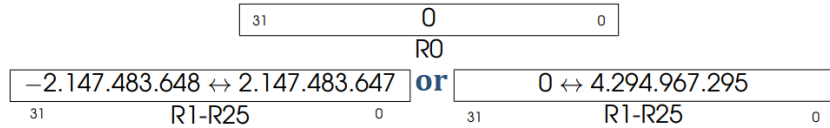
- ▶ Arquitetura Poxim
 - ▶ *Complexity-Reduced Instruction Set Processor* (CRISP)
 - ▶ Didática, hipotética e simples com 32 bits
 - ▶ Memória Von Neumann de 32 KiB
 - ▶ 3 formatos de instruções

CISC tem operando de memória
RISC só usa registradores

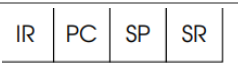
Registrador

Propósito geral (R0-R25)

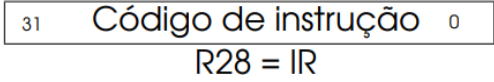
R0 possui valor constante 0 e os demais registradores podem armazenar valores de 32 bits com ou sem sinal



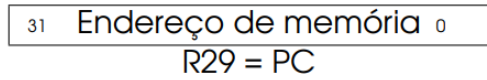
Controle e status (IR, PC, SP, SR)



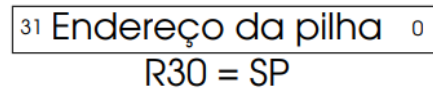
- (IR): armazena a instrução carregada da memória e em execução



- (PC): controla o fluxo de execução da aplicação apontando para as instruções

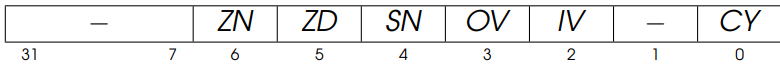


- (SP): referencia o topo da pilha na memória (alocação estática e subrotinas)



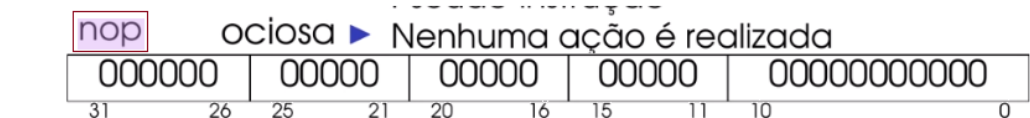
- (SR): controle de configurações e status das operações do processador

Registrador de status (SR) R31 = SR

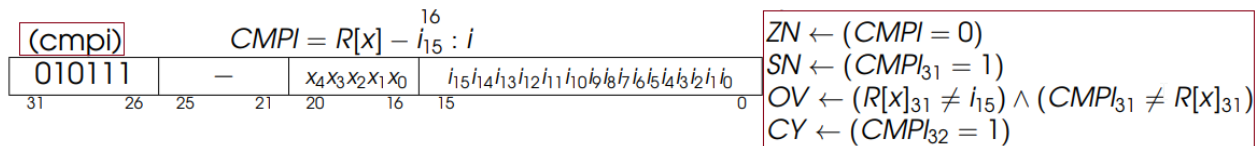
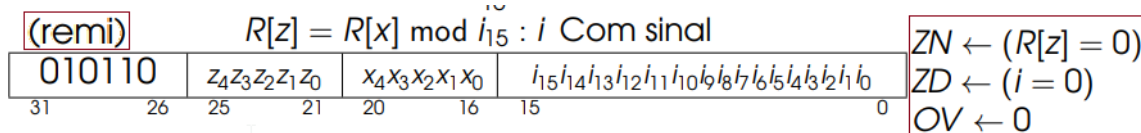
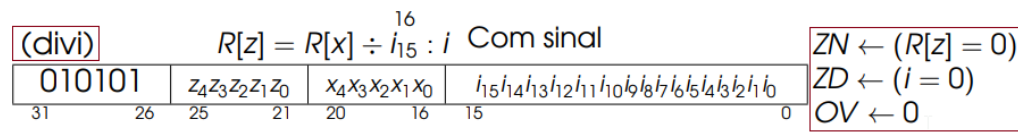
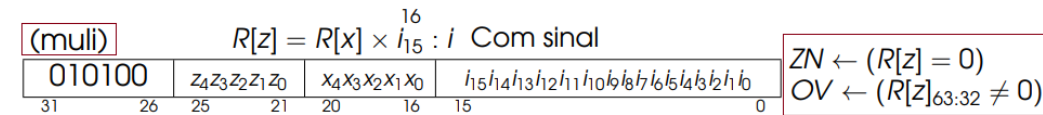


- ▶ ZN (zero): igual a 0
- ▶ ZD (divisão por zero): divisor $B = 0$
- ▶ SN (sinal): sinal negativo
- ▶ OV (overflow): extrapolação de capacidade
- ▶ IV (instrução inválida): código de operação inválido
- ▶ CY (carry): vai a um aritmético

Tipo U:

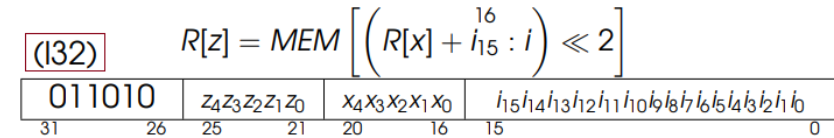
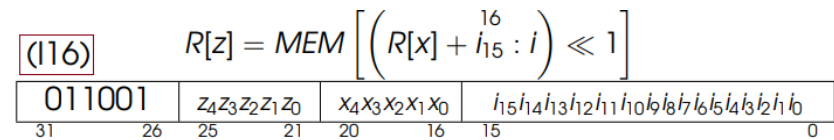
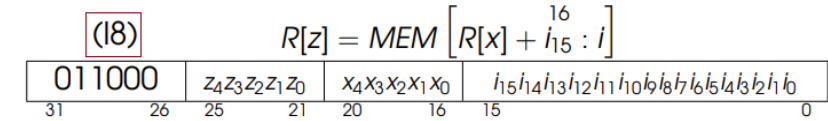


atribuição imediata

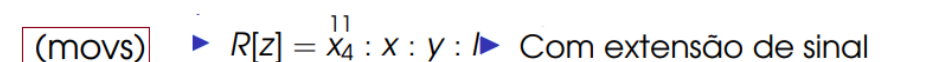
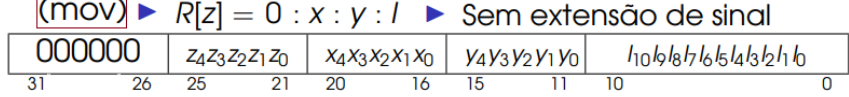
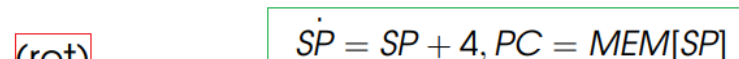
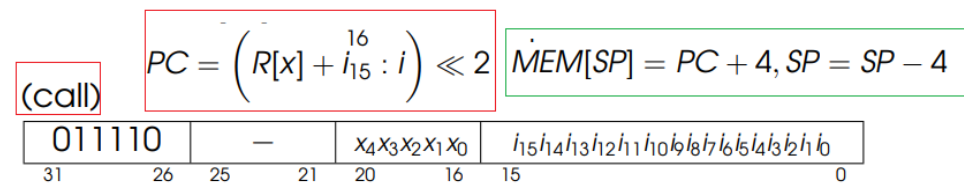
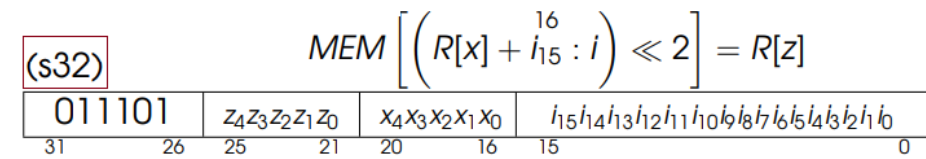
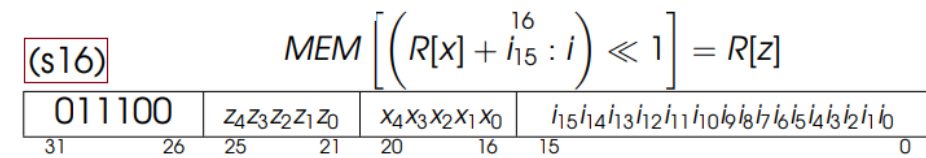
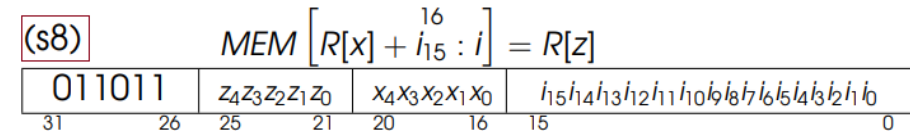


Tipo F:

Operações de leitura/escrita da memória l
8 bits (l8, s8) l 16 bits (l16, s16) l 32 bits (l32, s32)

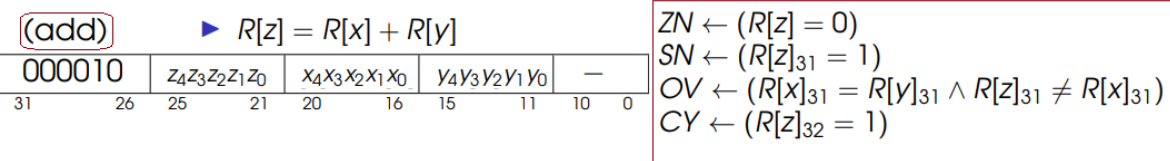


ESCRITA:



com registradores:

adição:



0b00010..

>> 1 = 0b00001..

int instrução;

inteiro = $a_1 a_2 a_3 z_1 z_2 z_3 m_1 m_2$

zr = $a_1 a_2 a_3 z_1 z_2 z_3 m_1 m_2$ & 00011100

$a_1 a_2 a_3 z_1 z_2 z_3 m_1 m_2$

0 0 0 1 1 1 0 0

zrmask = 0 0 0 $z_1 z_2 z_3$ 0 0

= 0 0 0 $z_1 z_2 z_3$ 0 0 >> 2

rz = 0 0 0 0 0 $z_1 z_2 z_3$

opmask =11100000

op = (instrução & opmask) >> 26

rz = (instrução & rzmask) >> 21

rx = (instrução & rxmask) >> 16

add, sub

if op == 0b001: // add

print("ADD, registrador{rz}, registraso rx{rx}")

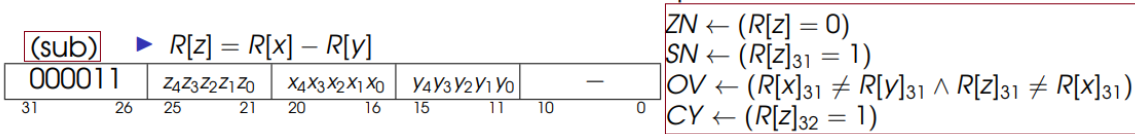
1 and 0 = 0

int op = instrução >> 21

if (OP == 0b00010)

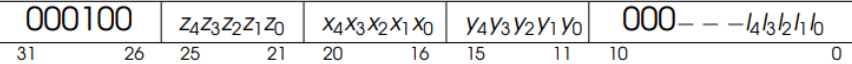
add(z,x,y)

subtração



multiplicação

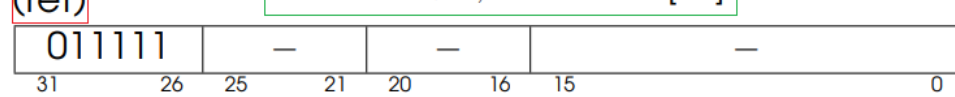
(mul) $R[l_{4:0}] : R[z] = R[x] \times R[y]$ Sem sinal



$ZN \leftarrow (R[l_{4:0}] : R[z] = 0)$
 $CY \leftarrow (R[l_{4:0}] \neq 0)$

(muls) $R[l_{4:0}] : R[z] = R[x] \times R[y]$ Com sinal

$ZN \leftarrow (R[l_{4:0}] : R[z] = 0)$



I Operações de controle de fluxo I

Desvio condicional:

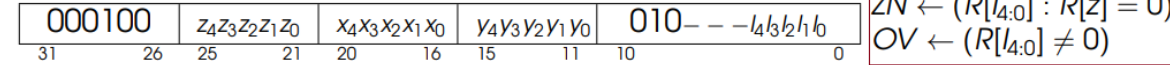
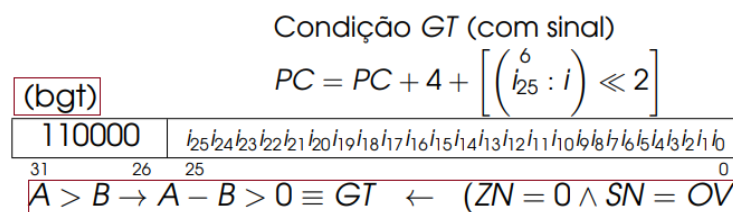
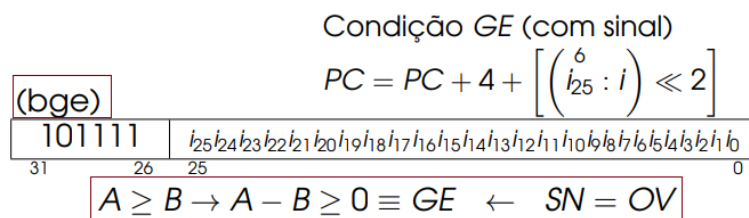
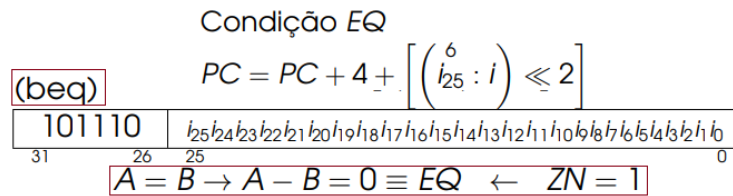
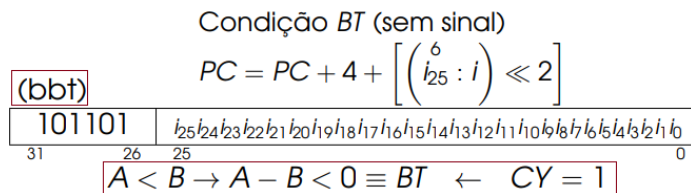
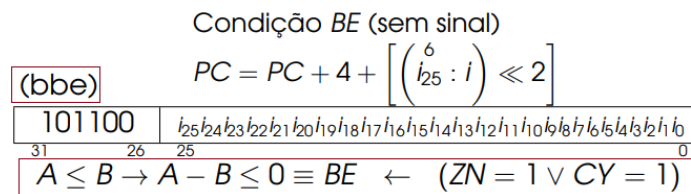
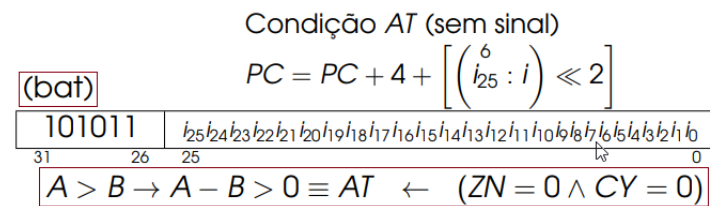
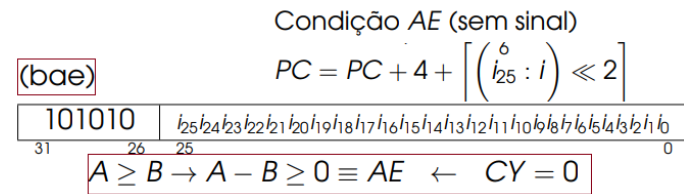
(bae, bat, bbe, bbt, beq, bge, bgt, biv, ble, blt, bne, bni, bnz, bzd)

Desvio incondicional:

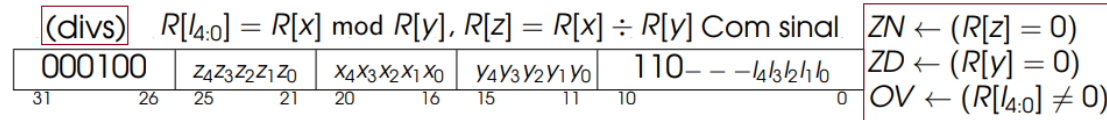
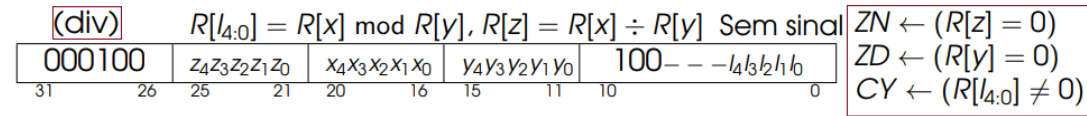
(bun) I Interrupção (int)

Desvio Condicional:

Tipo S:

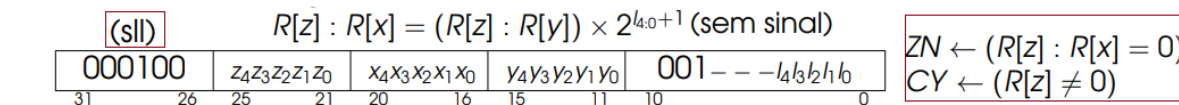


divisão:

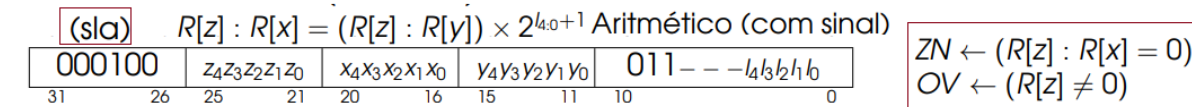


Deslocamento:

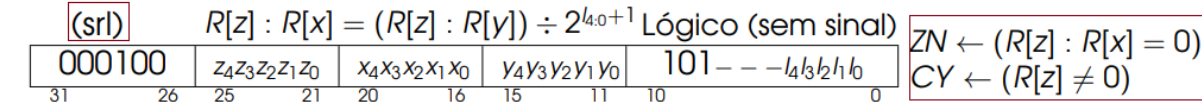
Esquerda lógico:



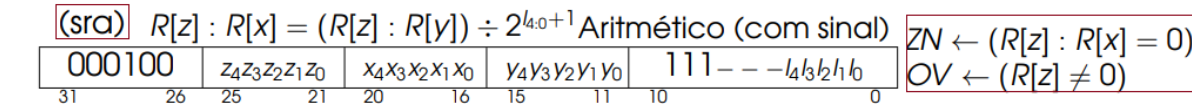
Esquerda aritmetico:



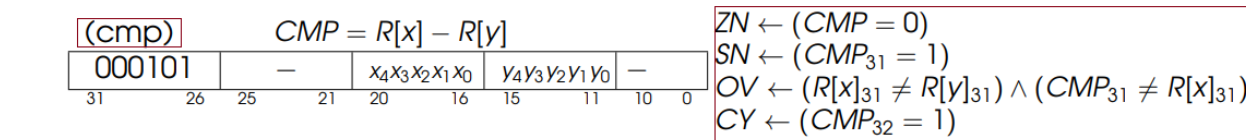
Direito lógico



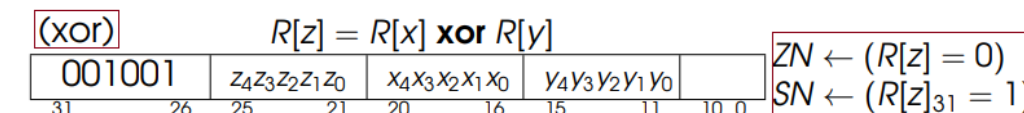
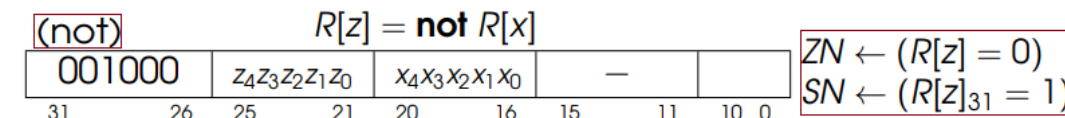
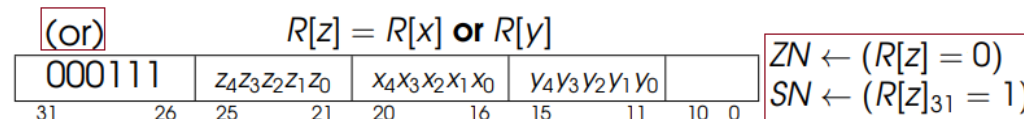
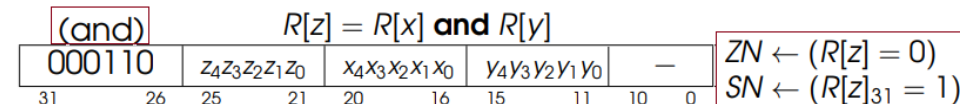
Direito aritmetico



Comparação



BIT A BIT:



FlowControl

