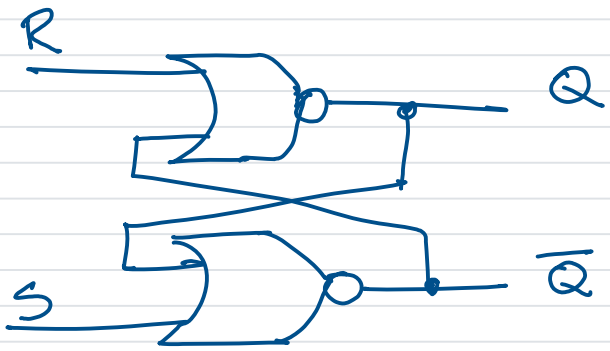
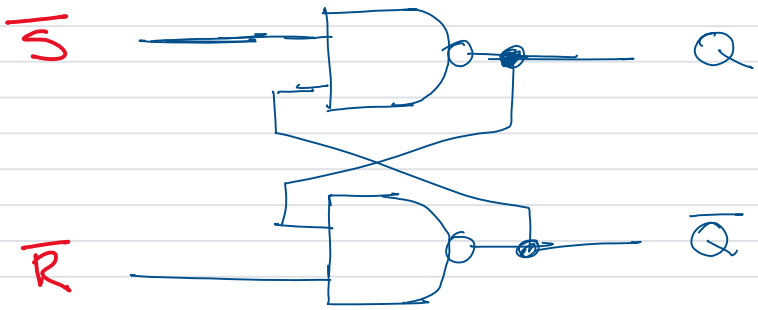
Latch SR (NOR) (Ativo com nível Alto)



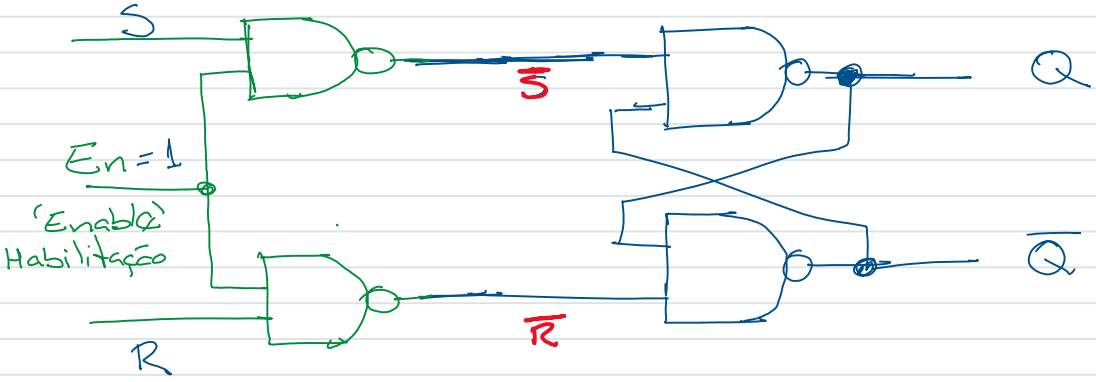
S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	(Memória)
0	1	0	1	(Resetado)
1	0	1	0	(Setado)
1	1	0	0	(Proibido)

LATCH SR (NAND) (Ativo com nível baixo)



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	(Proibido)
0	1	1	0	(Setado)
1	0	0	1	(Resetado)
1	1	Q	$\overline{Q}$	(Memória)

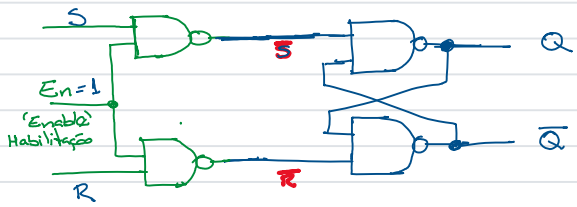
Latch SR Controlado (NAND

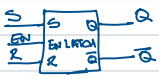


En	S	R	Q	$\overline{Q}$	
0	X	X	Q	$\overline{Q}$	(Memória)
1	0	0	Q	$\overline{Q}$	(Memória)
1	0	1	0	1	(Resetado)
1	1	0	1	0	(Setado)
1	1	1	1	1	(Proibido)

Registrador de Dados

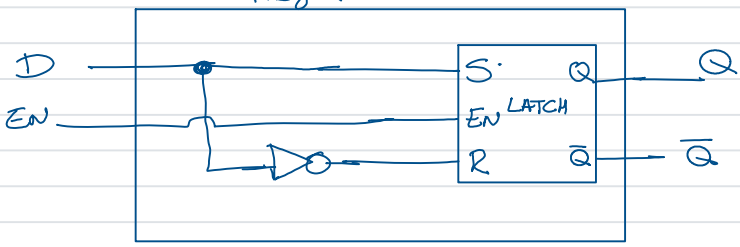
Latch SR Controlado (NAND





En	S	R	Q	$\overline{Q}$	
0	X	X	Q	$\overline{Q}$	(memória)
1	0	0	Q	$\overline{Q}$	
1	0	1	0	1	(resetado)
1	1	0	1	0	(setado)
1	1	1	1	1	(proibido)

Registrador dados 1bit



Registrador de Dados de 8 bits