# Exercises for Architectures of Supercomputers

3<sup>rd</sup> Exercise, 13./14.11.2019

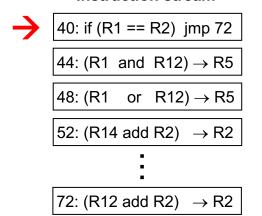




## Timestep n

1.Step	2.Step	3.Step	4.Step	
IF	ID	OF	EX	•••

#### **Instruction stream**



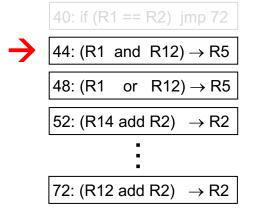
R1:	0	R7:	9
R2:	0	R8:	10
R3:	2	R9:	23
R4:	1	R10:	34
R5:	23	R11:	15
R6:	4	R12:	8



Timestep n+1: Fetching the compare-and-branch instruction

1.Step	2.Step	3.Step	4.Step	
IF	ID	OF	EX	•••
40: if (R1 == R2) jmp 72				

#### **Instruction stream**



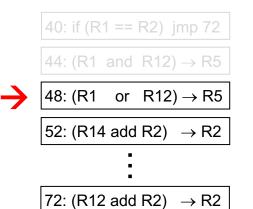
R1:	0	R7:	9
R2:	0	R8:	10
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R5:	23	R11:	15
R6:	4	R12:	8



Timestep n+2: Decoding the compare-and-branch instruction

	1.Step	2.Step	3.Step	4.Step	
	IF	ID	OF	EX	•••
44: (R1 a	nd R12) → R5	40: if (R1 == R2) jmp 72			

#### **Instruction stream**



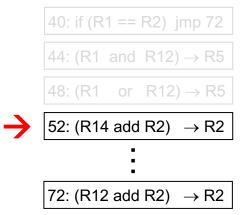
R1:	0	R7:	9
R2:	0	R8:	10
R3:	2	R9:	23
R4:	1	R10:	34
R5:	23	R11:	15
R6:	4	R12:	8



• Timestep n+3: Fetching the instruction's operatnds

1.Step		2.Step	3.Step	4.Step	
IF		ID	OF	EX	•••
48: (R1	or R12) → R5	44: (R1 and R12) → R5	40: if (R1 == R2) jmp 72		

#### **Instruction stream**



R1:	0	R7:	9
R2:	0	R8:	10
R3:	2	R9:	23
R4:	1	R10:	34
R5:	23	R11:	15
R6:	4	R12:	8

72: (R12 add R2)  $\rightarrow$  R2



• Timestep n+3: Fetching the instruction's operatnds

1.Step	2.Step	2.Step 3.Step		
IF	ID	OF	EX	
48: (R1 or R12) → R5	44: (R1 and R12) → R5	40: if (R1 == R2) jmp 72		
	on stream R2) jmp 72	Register	contents	
44: (R1 and	$\begin{array}{c} R12) \rightarrow R5 \\ \hline R12) \rightarrow R5 \end{array}$	R1: 0 R2: 0 R3: 2	R7: 9 R8: 10 R9: 23	
_	d R2) → R2	R4: 1 R5: 23 R6: 4	R10: 34 R11: 15 R12: 8	



#### Timestep n+4

1.Step		2.Step				3.Step	4.Step		
IF			I	D		OF	EX		•
52: (R14 add R2)	→ R2	48: (R1	or	R12) → R5	44: (R1	and R12) $\rightarrow$ R5	40: if (R1 == R2)	jmp 72	

#### **Instruction stream**

40: if (R1 == R2) jmp 72 44: (R1 and R12) → R5 48: (R1 or R12) → R5 52: (R14 add R2) → R2 ...

72: (R12 add R2) → R2

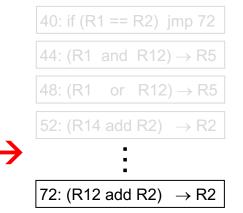
R1:	0	R7:	9
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## Timestep n+4

1.Step	2.Step	3.Step	4.Step	
IF	ID	OF	EX	
52: (R14 add R2) → R2	48: (R1 or R12) → R5	44: (R1 and R12) → R5	40: if (R1 == R2) jmp 72	
			Branch instruction executed	

#### **Instruction stream**



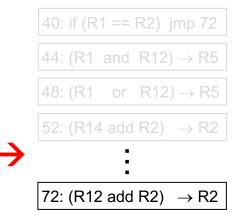
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## Timestep n+4

	1.Step			2.Ste	р		3.Step		4.Step	
	IF			ID			OF		EX	•••
5	2: (R14 add R2)	→ R2	48: (R1	or R	12) → R5	44: (R1	and R12) $\rightarrow$	R5	40: if (R1 == R2) jmp 72	
									Next instruction at address 72!	

#### **Instruction stream**



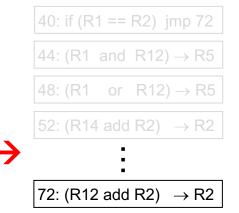
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## Timestep n+4

2

#### **Instruction stream**



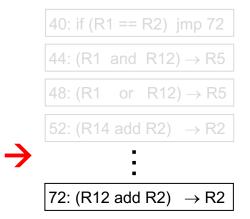
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## Timestep n+4

1.Step	2.Step	3.Step	4.Step	
IF	ID	OF	EX	•••
52: (R14 add R2) → R2	48: (R1 > R12) → R5	44: (R1 and R12) → R5	40: if (R1 == R2) jmp 72	
			Flushing of the pipeline required	

#### **Instruction stream**



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    - Branch-prediction units do a very good job detecting regular branch patterns
      - To prevent the branch-prediction unit from interfering with measurements, we need to "confuse" the unit on purpose by using irregular branches

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- Use an init() function to fill an array (e.g., an integer array)
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- You can then use the data in the array to decide whether to jump or not, e.g.:

```
for (i=0; i<N; ++i) {
   if (A[i] == 0)
      some_code;
   else
      other_code;
}</pre>
```



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  - The function should initialize a variable called result to zero and iterate over the array with the random numbers
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- Hint: Make sure to only use the -O3 compiler option when compiling



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- Question 1: What penalty do you observe for the code that contains branches?



- Next, we will execute the same code without branches
- Write a benchmark\_nobranch() function that does not check the array's values but always adds a value of one to the result variable
- Then, calculate the runtime of one loop iteration of this code
- Question 1: What penalty do you observe for the code that contains branches?
- Question 2: Assuming that the branch-prediction unit correctly predicts the branch-target address 50% of the time (a reasonable assumption, when using evenly distributed random numbers), how many pipeline stages do you think there before the execution stage in the Ivy Bridge microarchitecture?