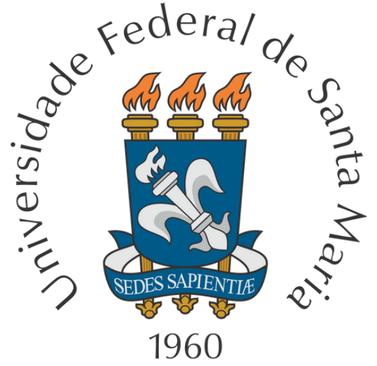
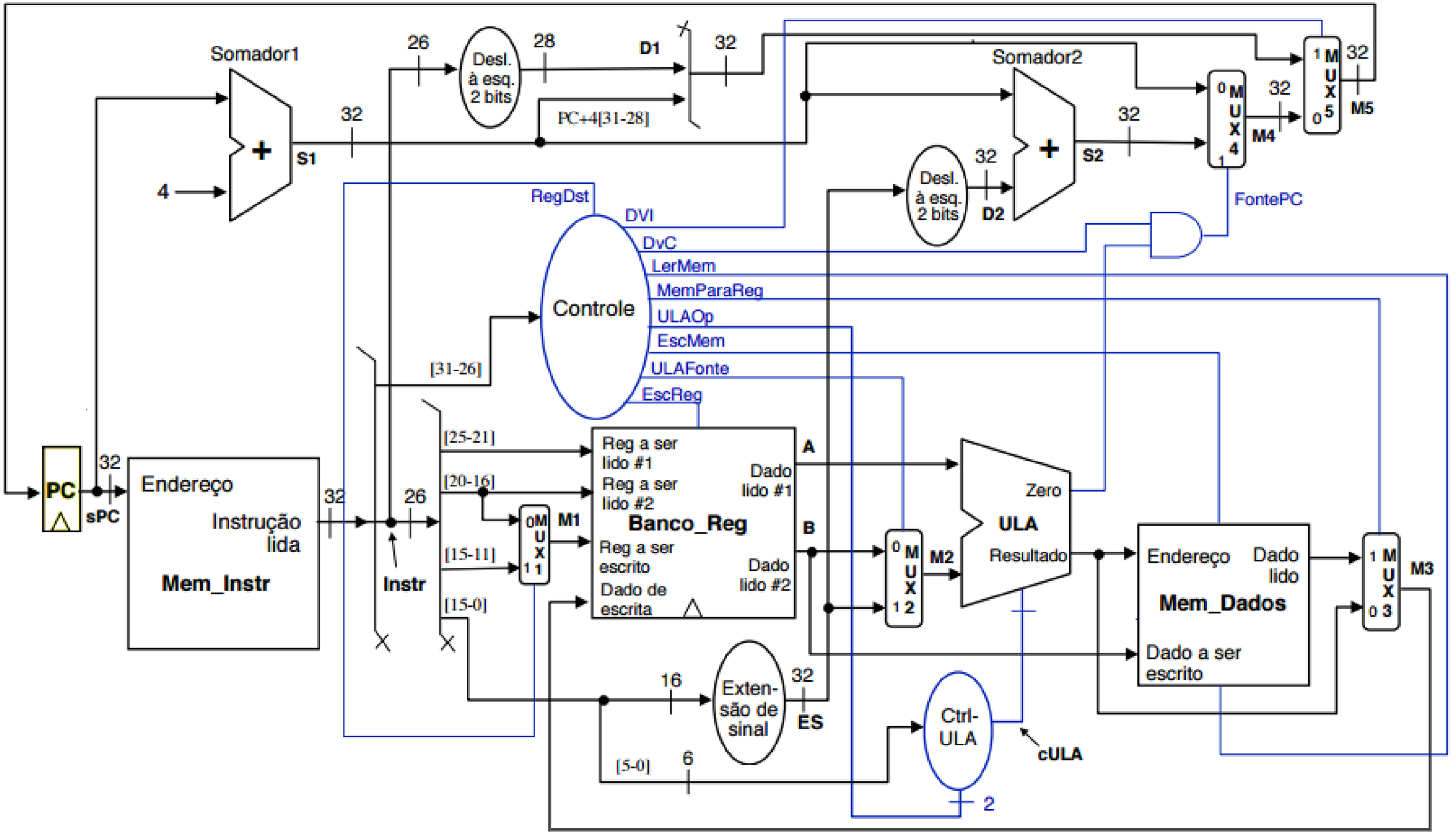
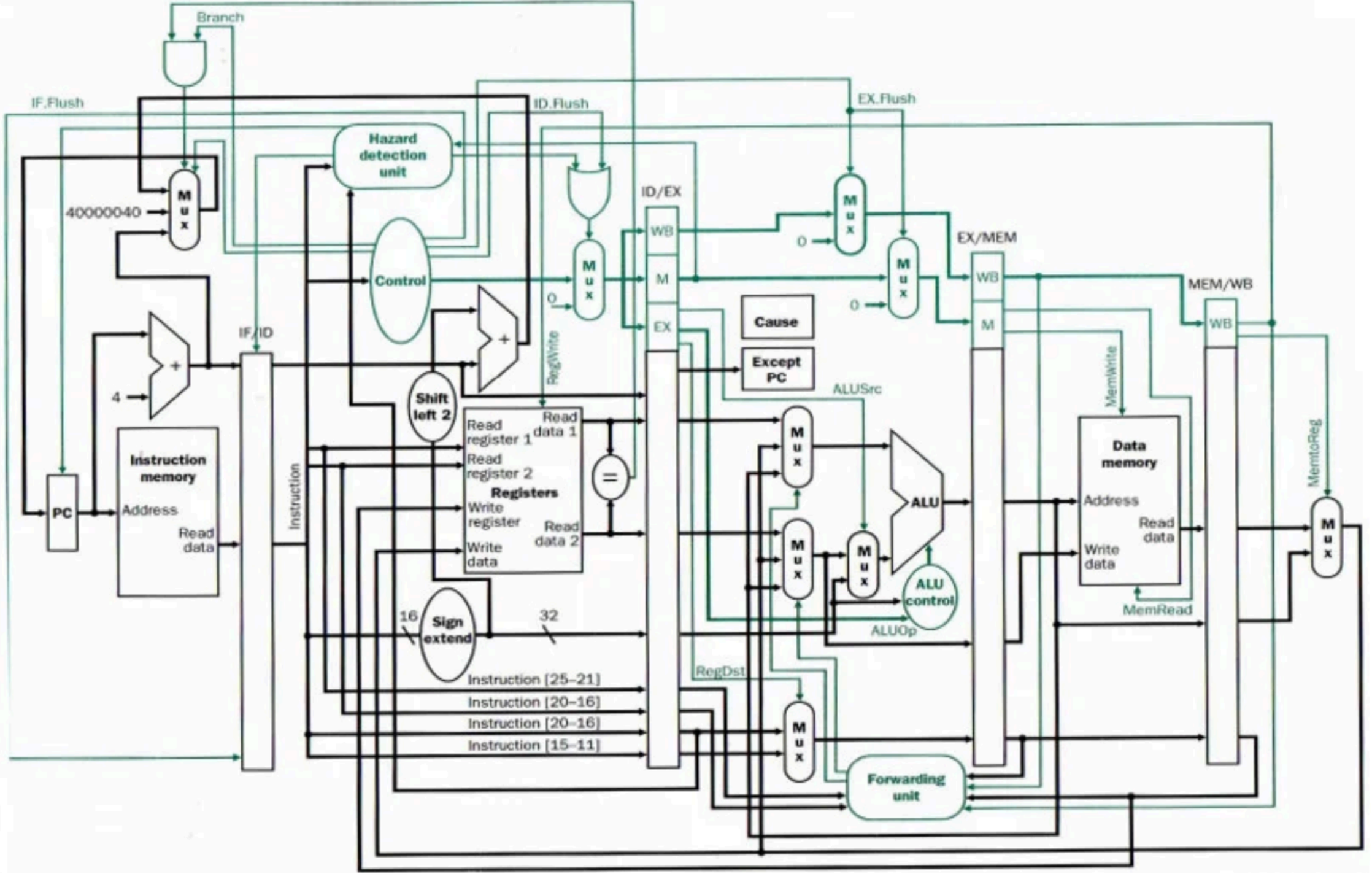


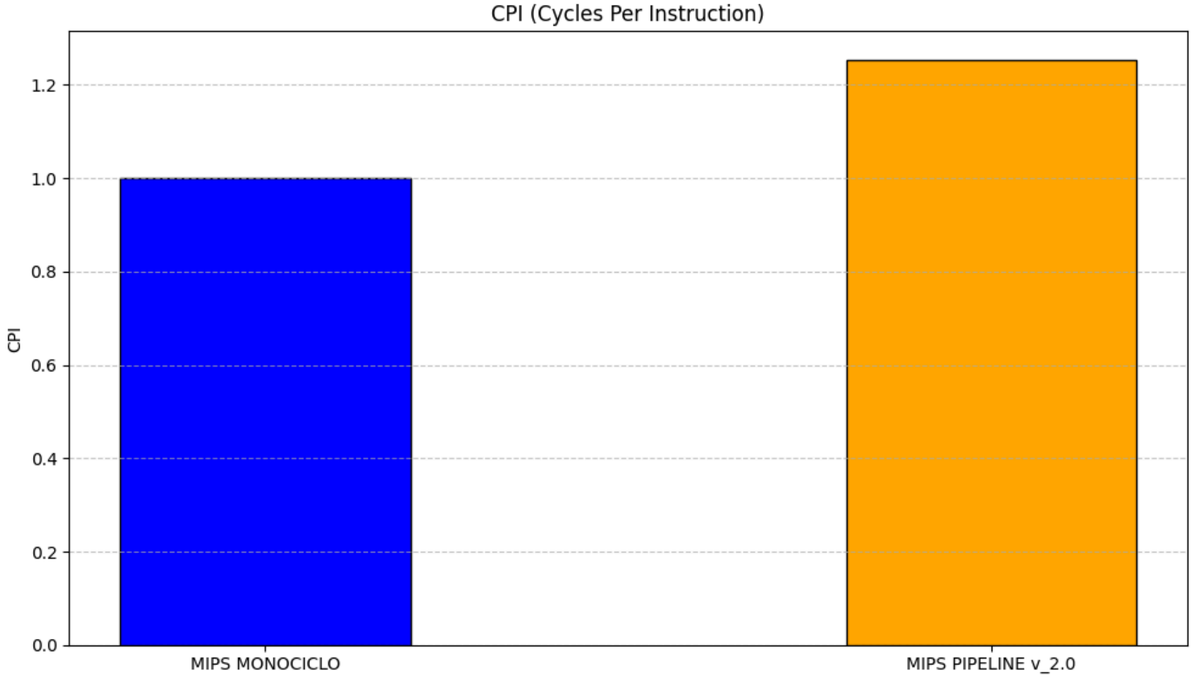

# Trabalho Mips Pipeline

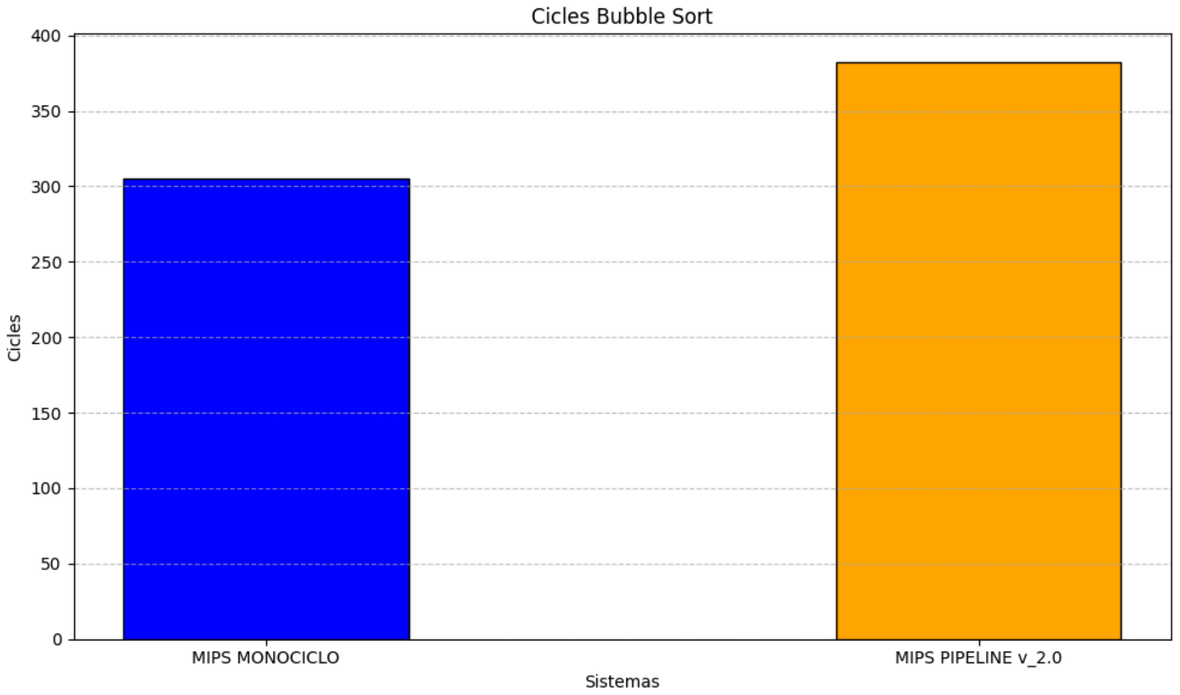
Professor: Mateus Beck Rutzig
Aluno: Bruno Henrique Spies

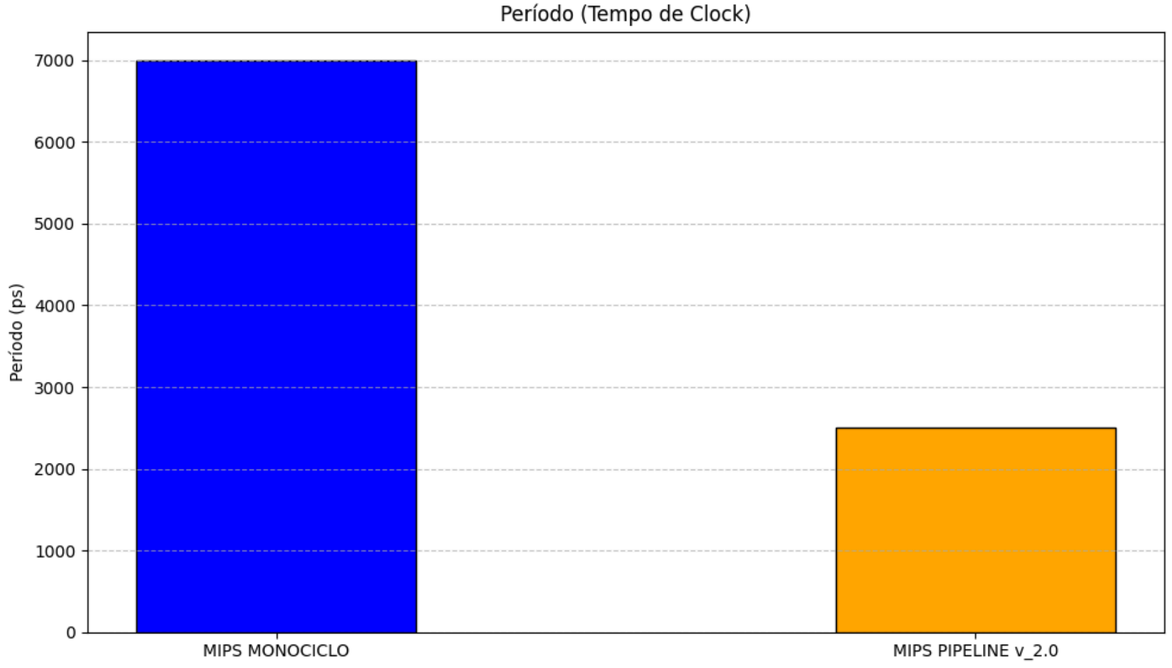

Somador1
4
S1
26
Desl. à esq. 2 bits
28
D1
32
PC+4[31-28]
Somador2
32
S2
Desl. à esq. 2 bits
32
D2
M4
M5
FontePC
RegDst
DVI
DvC
LerMem
MemParaReg
ULAOp
EscMem
ULAFonte
EscReg
Controle
[31-26]
PC
sPC
Endereço
Instrução lida
Mem_Instr
Instr
[25-21]
[20-16]
[15-11]
[15-0]
M1
Reg a ser lido #1
Reg a ser lido #2
Banco_Reg
Reg a ser escrito
Dado de escrita
Dado lido #1
Dado lido #2
A
B
M2
Zero
ULA
Resultado
Endereço
Dado lido
Mem_Dados
Dado a ser escrito
M3
16
Exten-são de sinal
ES
[5-0]
6
Ctrl-ULA
cULA
2

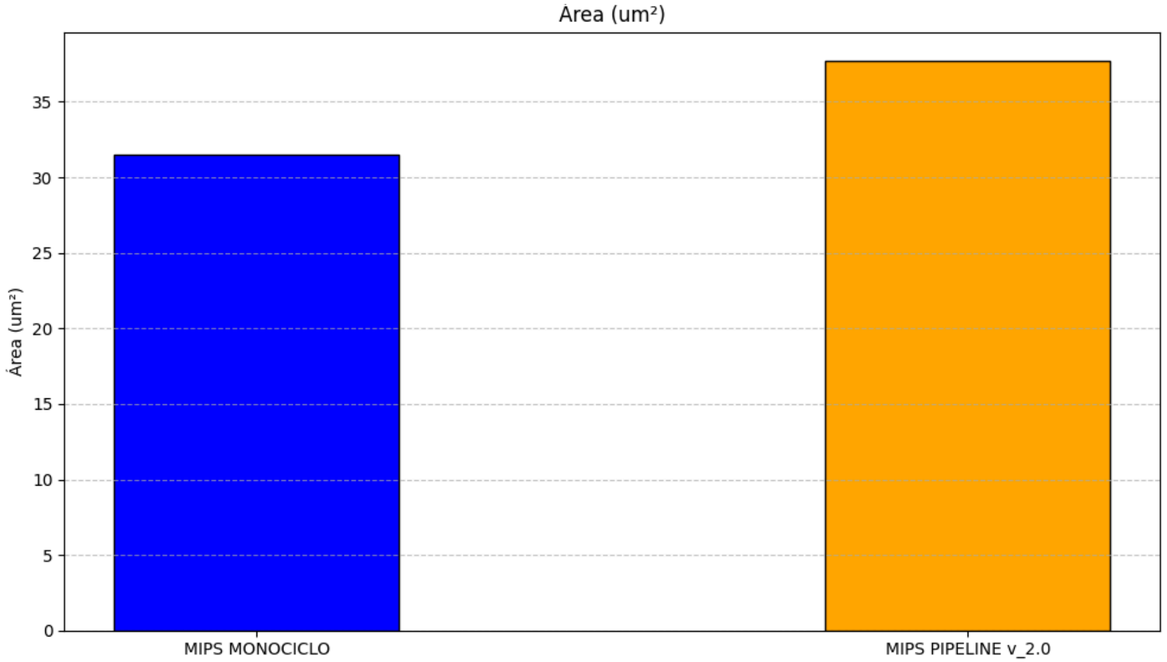

Branch
IF.Flush
ID.Flush
EX.Flush
Hazard detection unit
40000040
M u x
Control
ID/EX
WB
M
EX
EX/MEM
MEM/WB
Cause
Except PC
RegWrite
ALUSrc
MemWrite
MemtoReg
Shift left 2
IF/ID
Instruction
PC
Instruction memory
Address
Read data
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
=
+
4
16
Sign extend
32
ALU
ALU control
ALUOp
RegDst
MemRead
Data memory
Instruction [25–21]
Instruction [20–16]
Instruction [20–16]
Instruction [15–11]
Forwarding unit

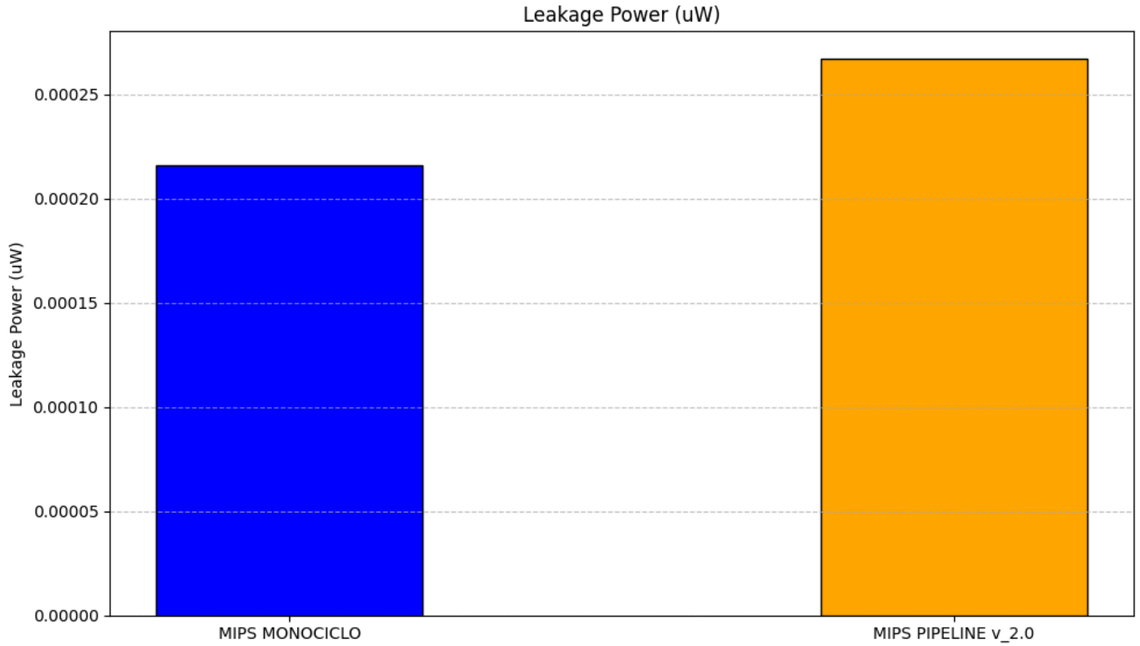
| | Ciclos | CPI | Periodo (ps) | Freq Max (MHz) | Slack (ps) | area ($um^2$) | Laeakage Power (uW) | Total Power (uW) |
|---|---|---|---|---|---|---|---|---|
| MIPS MONOCICLO | 305 | 1 | 7000 | 143 | 4 | 31.512,56 | 2,16E-04 | 5,30E-03 |
| MIPS PIPELINE | 382 | 1,252459 | 2500 | 400 | 1 | 37.725 | 2,67E-04 | 1,93E-02 |

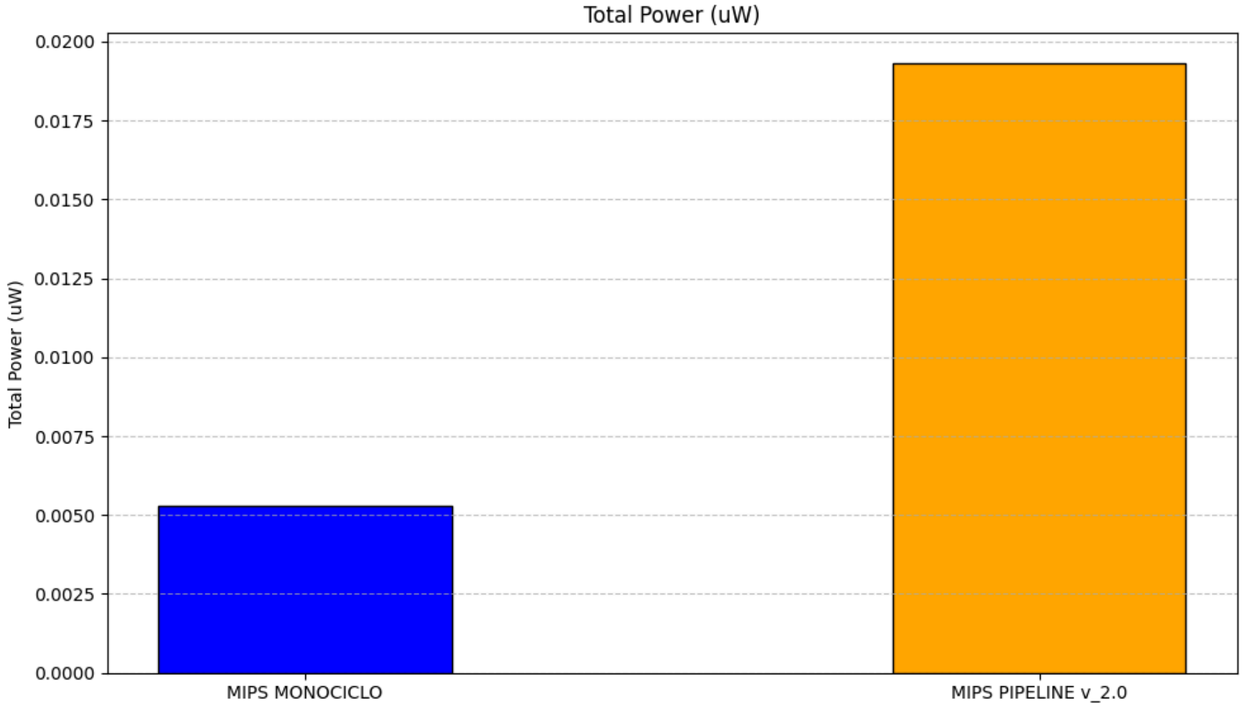

CPI (Cycles Per Instruction)
CPI
0.0
0.2
0.4
0.6
0.8
1.0
1.2
MIPS MONOCICLO
MIPS PIPELINE v_2.0


Cicles Bubble Sort
Cicles
0
50
100
150
200
250
300
350
400
MIPS MONOCICLO
MIPS PIPELINE v_2.0
Sistemas


Período (Tempo de Clock)
Período (ps)
0
1000
2000
3000
4000
5000
6000
7000
MIPS MONOCICLO
MIPS PIPELINE v_2.0


Área (um²)
Área (um²)
0
5
10
15
20
25
30
35
MIPS MONOCICLO
MIPS PIPELINE v_2.0

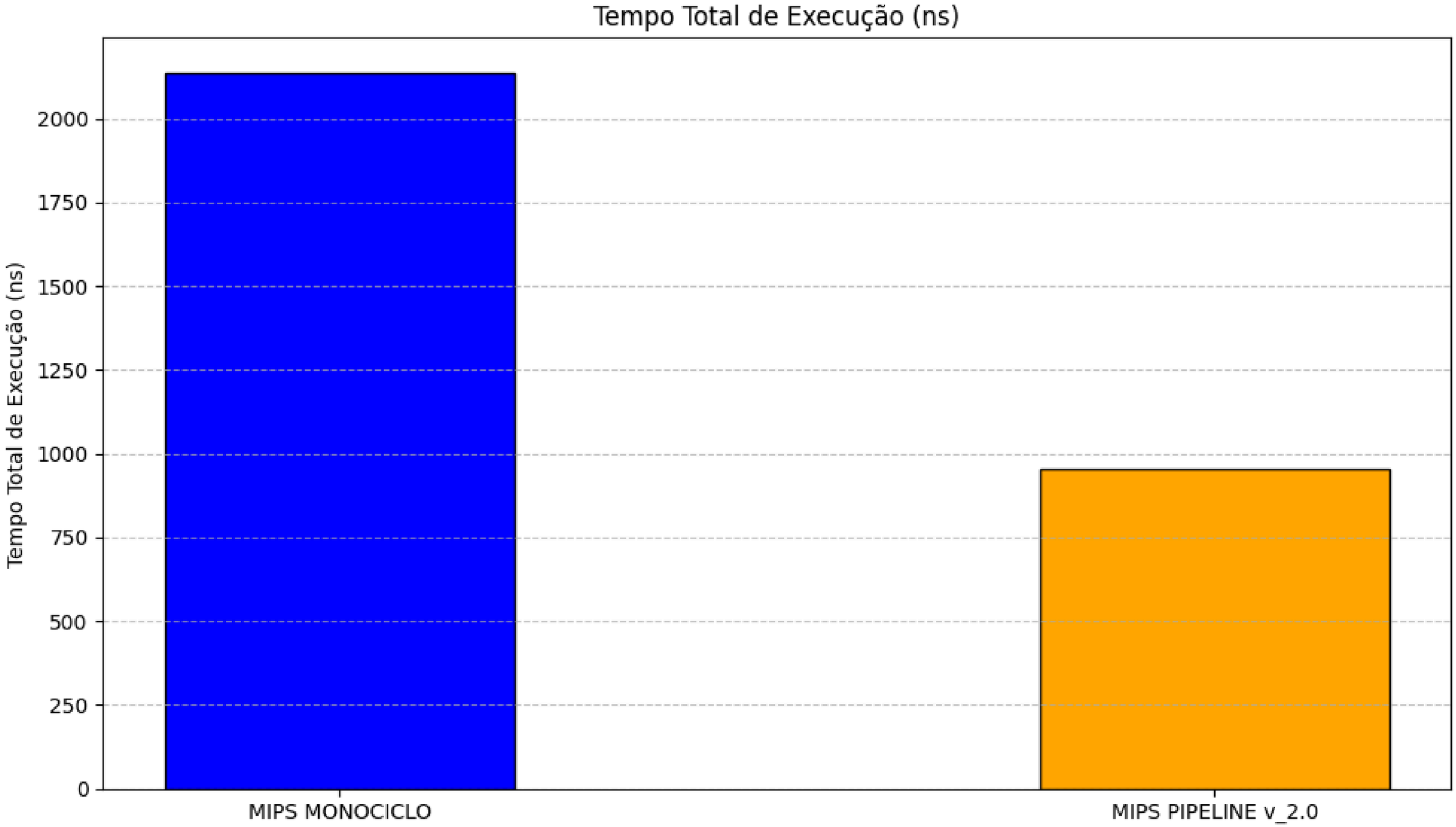

Leakage Power (uW)
Leakage Power (uW)
0.00000
0.00005
0.00010
0.00015
0.00020
0.00025
MIPS MONOCICLO
MIPS PIPELINE v_2.0


Total Power (uW)
Total Power (uW)
0.0000
0.0025
0.0050
0.0075
0.0100
0.0125
0.0150
0.0175
0.0200
MIPS MONOCICLO
MIPS PIPELINE v_2.0

# Tempo Total:

**Monociclo: 305 ciclos X 7000ps =  2135 ns**

**Pipeline: 382 ciclos X 2500ps =  955 ns**


Tempo Total de Execução (ns)
Tempo Total de Execução (ns)
2000
1750
1500
1250
1000
750
500
250
0
MIPS MONOCICLO
MIPS PIPELINE v_2.0