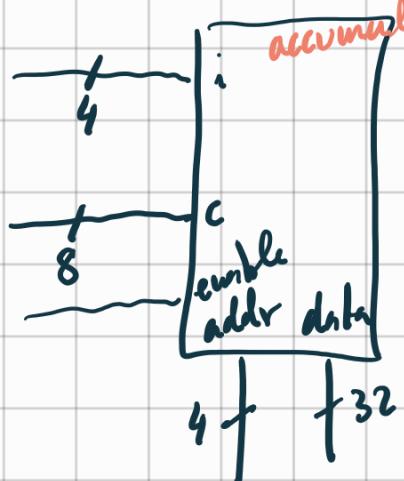


AAD 2024-11-18

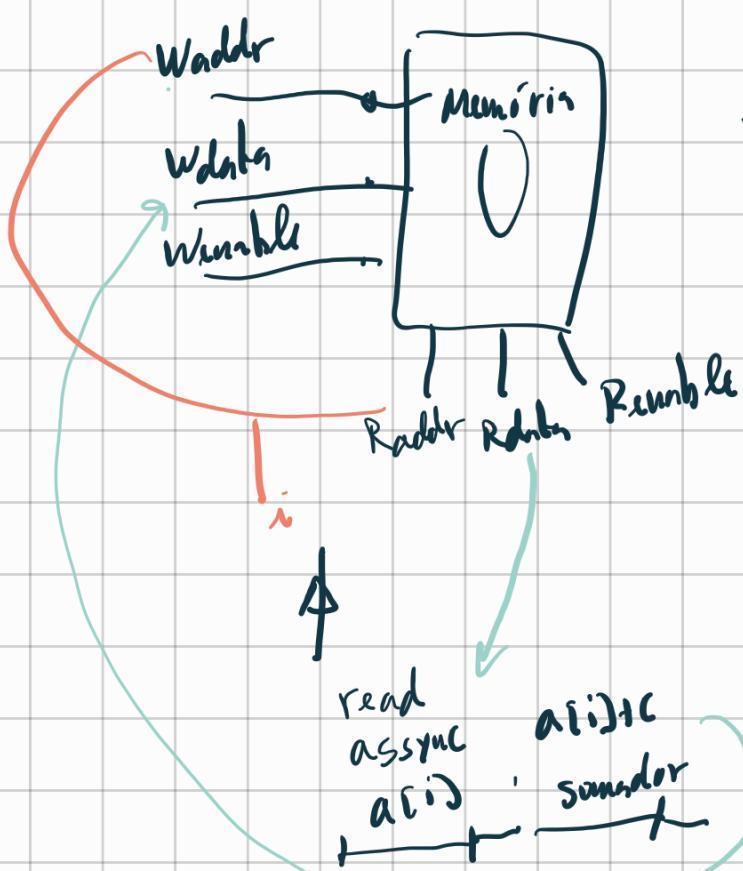
$a[i] += c;$       *unsigned int a[16];  
                  char c;*

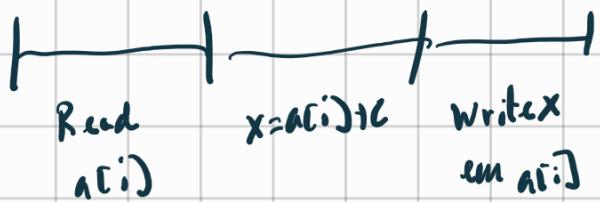
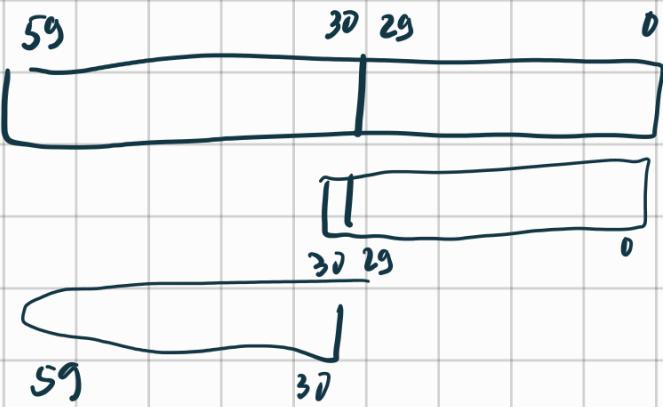


*if (ewable)  
 $a[i] += c;$*

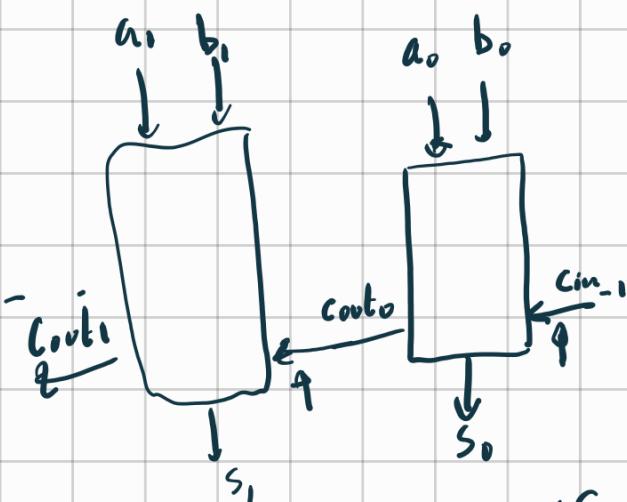
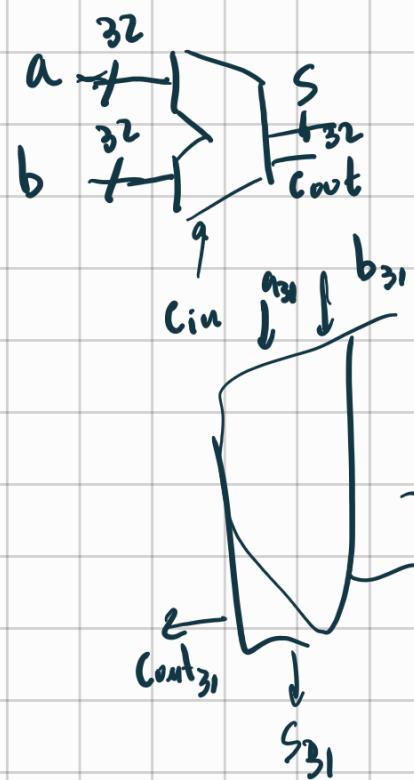
VHDL

$data = a[addr]$





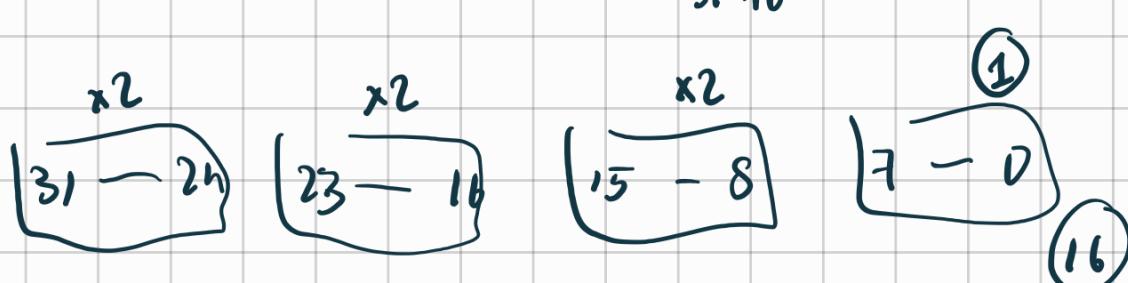
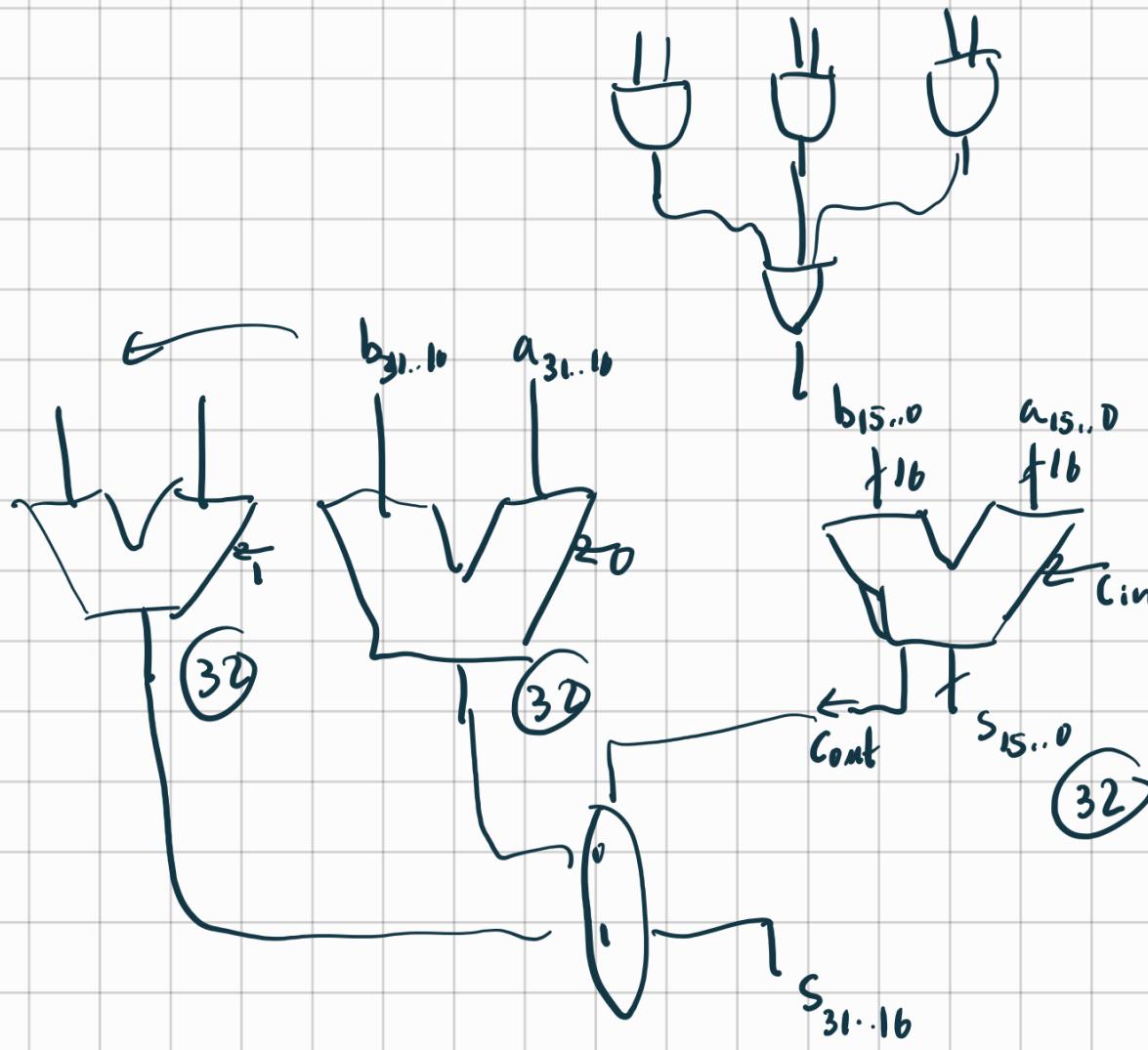
Read      Modify      Write



$$2 \cdot (cout_0 + s_0) = a_0 + b_0 + cin_{n-1}$$

$s = a \text{ xor } b \text{ xor } \text{cin} ;$

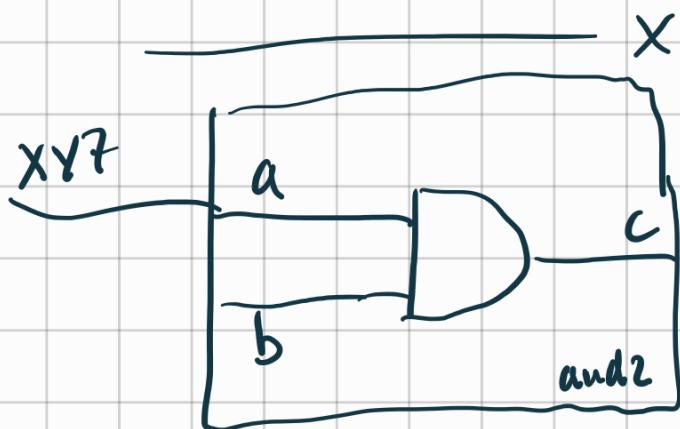
$e_{\text{out}} = (\text{a and } b) \text{ or } (\text{a and } \text{cin}) \text{ or } (\text{b and } \text{cin})$



$a \ll b$   
 $a \gg b$

barrel  
shifter

$a \ll\ll b$  (rotate)  
 $a \gg\gg b$

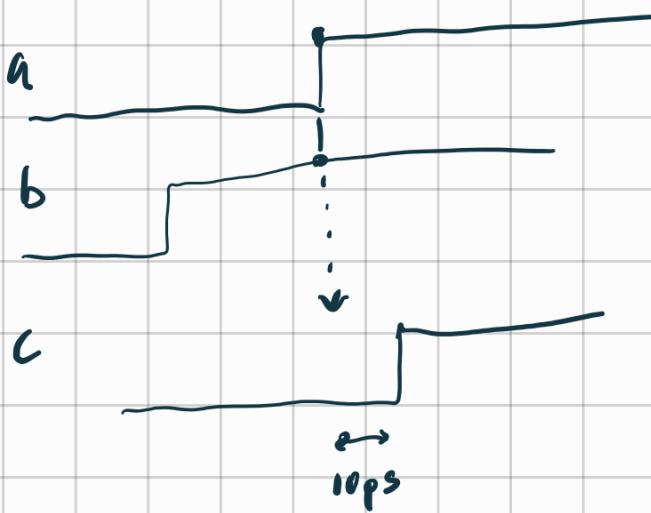


$x$

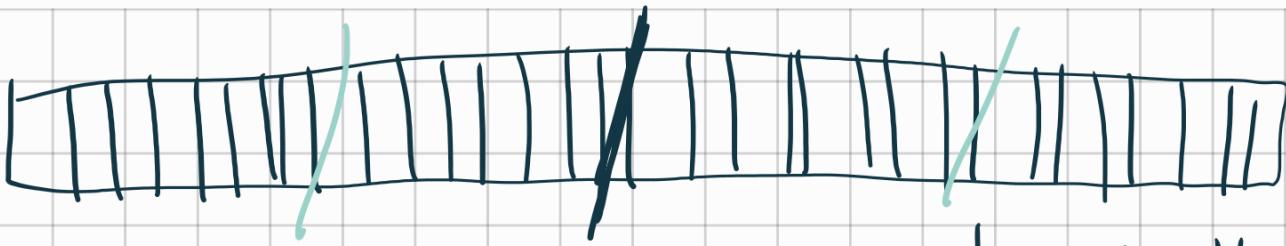
$0 \rightarrow \text{falso}$   
 $1 \rightarrow \text{verdadeir.}$

$a$	$b$	$a \text{ und } b$
0	0	0
0	1	0
1	0	0
1	1	1

$a \Rightarrow xyz;$   
 $b \Rightarrow$



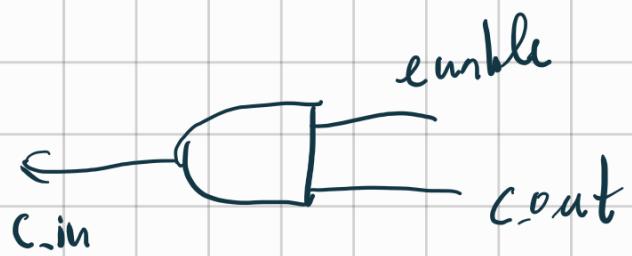
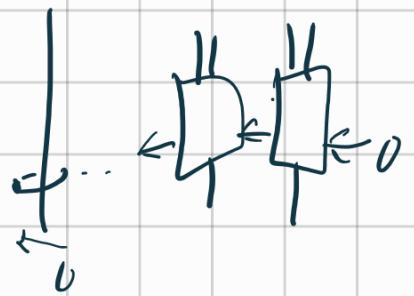
$b \leq a \text{ and not } a;$



SIMD

32 bits

$2 \times 16 \text{ bits}$   
 $4 \times 8 \text{ bits}$



$$\begin{array}{c}
 \overbrace{\quad\quad\quad}^X \\
 |S| \quad \underbrace{\text{midulo}}_{b_3 \ b_2 \ b_1 \ b_0} \\
 \end{array}
 \quad
 \begin{array}{c}
 \overbrace{\quad\quad\quad}^X \\
 (-1)^3 \times \underbrace{\text{midulo}}_{2^3 \cdot b_3 + 2^2 \cdot b_2 + 2 \cdot b_1 + b_0} \\
 \end{array}$$

$b_3 \ b_2 \ b_1 \ b_0$

unsigned

$$2^3 \cdot b_3 + 2^2 \cdot b_2 + 2^1 \cdot b_1 + 2^0 \cdot b_0$$

Signed

$$-2^3 \cdot b_3 + 2^2 \cdot b_2 + 2^1 \cdot b_1 + 2^0 \cdot b_0$$



$$-2^3 \cdot b_3 = -2^4 \cdot b_3 + 2^3 \cdot b_3$$

$$= -2^5 \cdot b_3 + 2^4 \cdot b_3 + 2^3 \cdot b_3$$

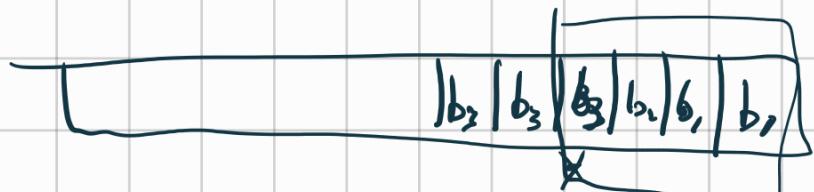
Signed       $-2^4 \cdot b_3 + \boxed{2^3 b_3 + 2^2 b_2 + 2^1 \cdot b_1 + 2^0 \cdot b_0}$

Unsigned

unsigned



Signed



$$-2^{n+1} + 2^n = -2^n$$

~~X~~ +

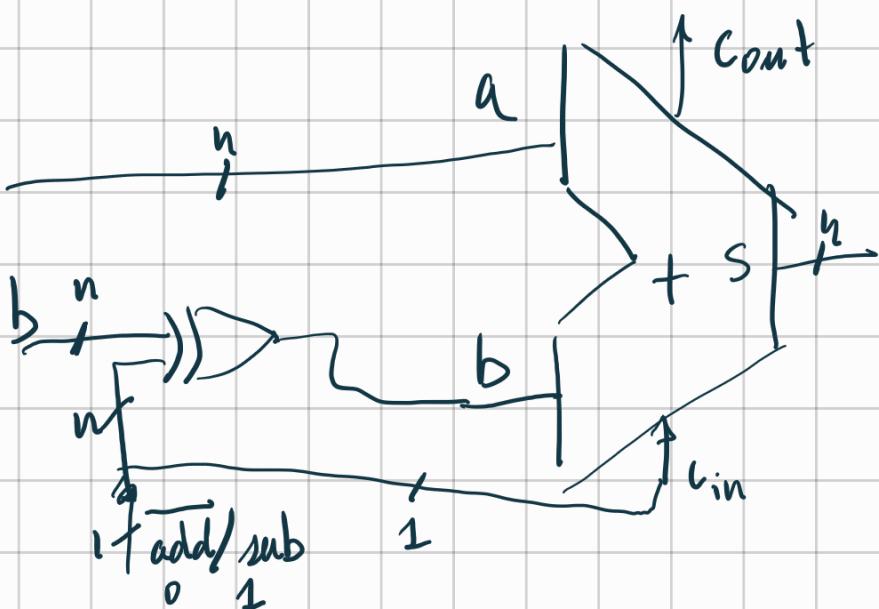
+ ~~X~~

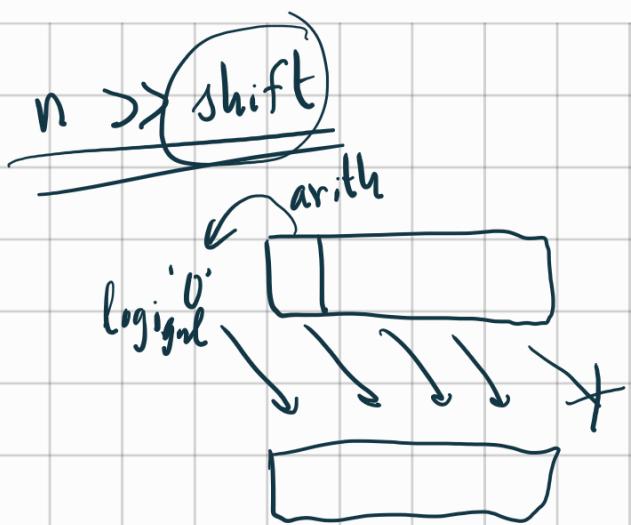
$$a - b = a - b + 2^n = a + \boxed{(2^{n-1}) - b} + 1$$

$\overline{b}$

$$\begin{array}{r}
 2^{-1} & 1 & 1 & 1 & 1 \\
 b & 0 & 1 & 1 & 0 \\
 \hline
 \overline{b} & 1 & 0 & 0 & 1
 \end{array}$$

A V





shift

