Arquiteturas de Alto Desempenho 2024/2025

Practical class AAD P11 (2024-12-02 and 2024-12-03)

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1 Objectives

Simulate some simple sequential circuits described using VHDL.

2 Exercise 1: D-type flip-flop

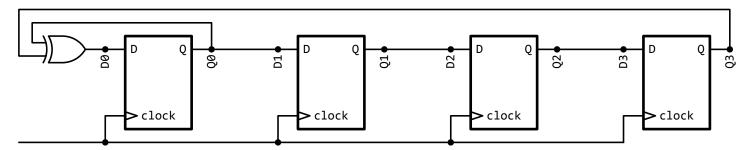
The D-type flip-flop is one of the most useful digital circuits. It can be used to store one bit of information. The file d_flip_flop.vhd contains a VLDH description of a simple D-type flip-flop. Study it. File ex1_tb.vhd contains a test bench that can be used to generate waveforms that ilustrate how the flip-flop works. Load both to edaplayground.com and run the simulation. As as alternative, if you have ghdl just do

\$ make ex1.vcd

\$ gtkwave ex1.vcd

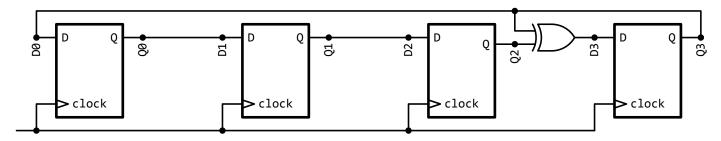
3 Execcise 2: more complex circuits using flip-flops

Create a VHDL entity that implements the following digital circuit.



Staring with all flip-flops in the '1' state, simulate the circuit for 50 clock cycles.

Repeat the above but for this other circuit.



4 Exercise 3: dual-port memory

The file dual_port_memory.vhd contains the description of a dual port memory. It provides four implementations (arquitectures): either the reads are synchrounous or they are asynchronous, and either the reads real old data when the read address is equal to the write address or they read the new data. Study it with extra care. File ex3_tb.vhd contains a test bench that can be used to generate waveforms that ilustrate how the dual port memory works. Load both to edaplayground.com and run the simulation. As as alternative, if you have ghdl just do

- \$ make ex3.vcd
- \$ gtkwave ex3.vcd

In the second practical assignment you will need to adapt the dual port entity to your needs, so study with extra care.

Advice: in order to make the simulation easier to understand, use first very small delays. In particular, edit the file dual_port_memory.vhd in order to make the delays at least 10 times smaller. For example, replace "500 ps" by "50 ps".