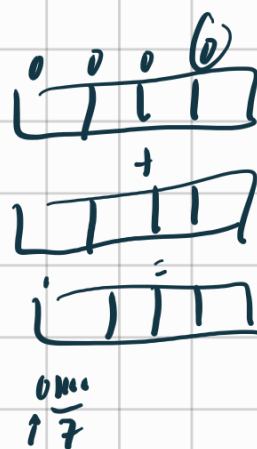
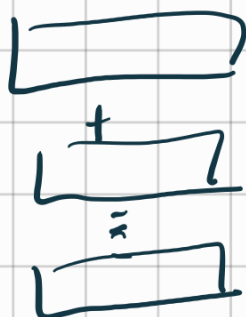


SIMD

Single - Instruction Multiple Data

32 bits

add



(a & 0b010011)  
↑ ↑

a 1 0b010011  
↑ ↑

\_\_\_\_\_ x \_\_\_\_\_ x \_\_\_\_\_

Intel/AMD

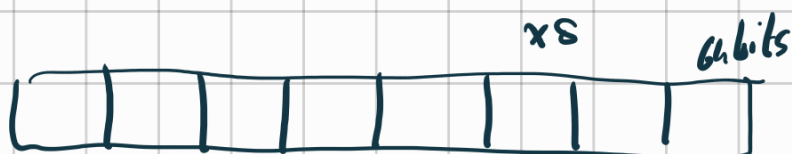
mmx 64 bits

xmm 128 bits

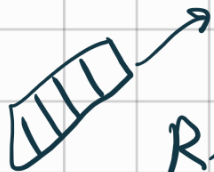
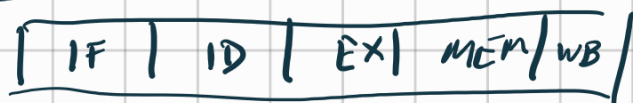
yymm 256 bits

zmm 512 bits

8 doubles  
16 float

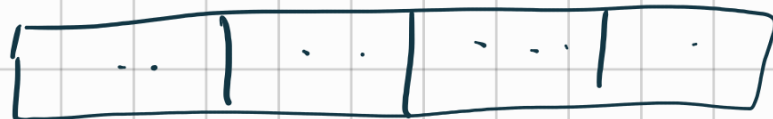


CUDA (Nvidia, AMD)



Registers ↓

1024 bits = 32 × 32 bits



← warp

