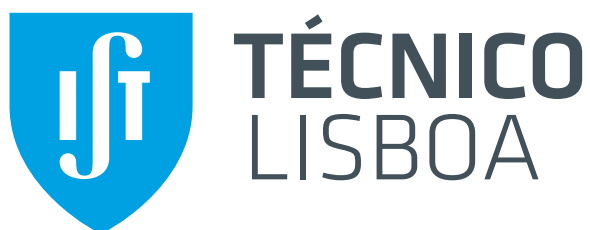


Circuit Theory and Electronics Fundamentals

Instituto Superior Técnico, University of Lisbon



Laboratory 2

MeAer

Dinis Salgado, 90560

Bruno Santos, 98460

Laura Cebola, 98464

April 08, 2021

Contents

1	Introduction	3
2	Theoretical Analysis	3
2.1	Computation of the voltages in all nodes and currents in all branches for $t < 0$; . . .	3
2.2	Determination of the equivalent resistance (R_{eq}) as seen from the capacitor terminals	5
2.3	Computation of the natural solution $v_{6n}(t)$, in the interval $[0, 20]$ ms	6
2.4	Computation of the forced solution $v_{6n}(t)$, in the interval $[0, 20]$ ms	7
2.5	Computation of the final total solution $v_6(t)$	8
2.6	Frequency Responses	9
3	Simulation Analysis	11
3.1	Operating Point Analysis for $t < 0$	11
3.2	Operating Point Analysis for $v_s(t) = 0$	11
3.3	Simulation of the natural response of the circuit	12
3.4	Simulation of the natural and forced response of the circuit	12
3.5	Simulation of the frequency response in node 6	13
4	Conclusion	14

1 Introduction

The objective of this laboratory assignment is to study a circuit containing a sinusoidal voltage source V_S connected to seven resistors, R , a dependent voltage source, V_d , a dependent current source I_b and a capacitor C . The circuit can be seen in Figure 1.

In Section 2, a theoretical analysis of the circuit is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

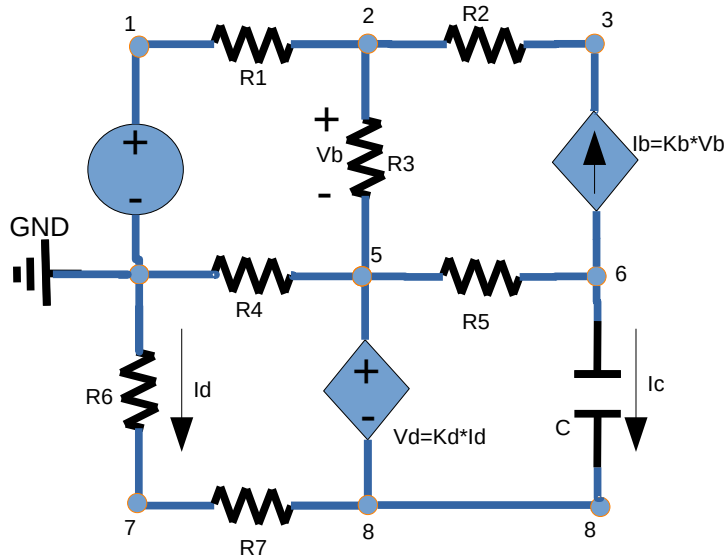


Figure 1: Given circuit.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically, in terms of its time and frequency responses.

2.1 Computation of the voltages in all nodes and currents in all branches for $t < 0$;

We can apply the node method, that is based in the Kirchhoff's Current Law (KCL) and in the Ohm's Law, to analyse circuits. According to this method, KCL is applied in nodes that aren't connected to voltage sources and the currents flowing into a node must add up to zero, which means that the algebraic sum of currents that enters into a node equals to the algebraic sum of currents that exits that node. In nodes related by voltage sources, additional equations are applied. For $t < 0$ the capacitor acts like an open circuit, so there is no current flow, in the branch containing the capacitor.

So, applying KCL for node 1, we have:

$$V_1 - V_0 = V_s \quad (1)$$

Node 2:

$$(V_3 - V_2) \times G_2 = (V_2 - V_1) \times G_1 + (V_2 - V_5) \times G_3 \quad (2)$$

Node 3:

$$(V_3 - V_2) \times G_2 = K_b \times (V_2 - V_5) \quad (3)$$

Node 6:

$$(V_5 - V_6) \times G_5 = K_b \times (V_2 - V_5) \quad (4)$$

And node 7:

$$(V_0 - V_7) \times G_6 = (V_7 - V_8) \times G_7 \quad (5)$$

The additional equations are:

$$V_5 - V_8 = -K_d \times (V_7) \times G_6 \quad (6)$$

$$(V_2 - V_5) \times G_3 - (V_5 - V_0) \times G_4 - (V_5 - V_6) \times G_5 + (V_7 - V_8) \times G_7 = 0 \quad (7)$$

The equation (7) are obtained using the voltage drop between the voltage source. The last equation was derived using a super-node that contains the dependent voltage source. Applying the node law, the sum of currents that enter the dependent voltage source is equal to the sum of currents that leaves it.

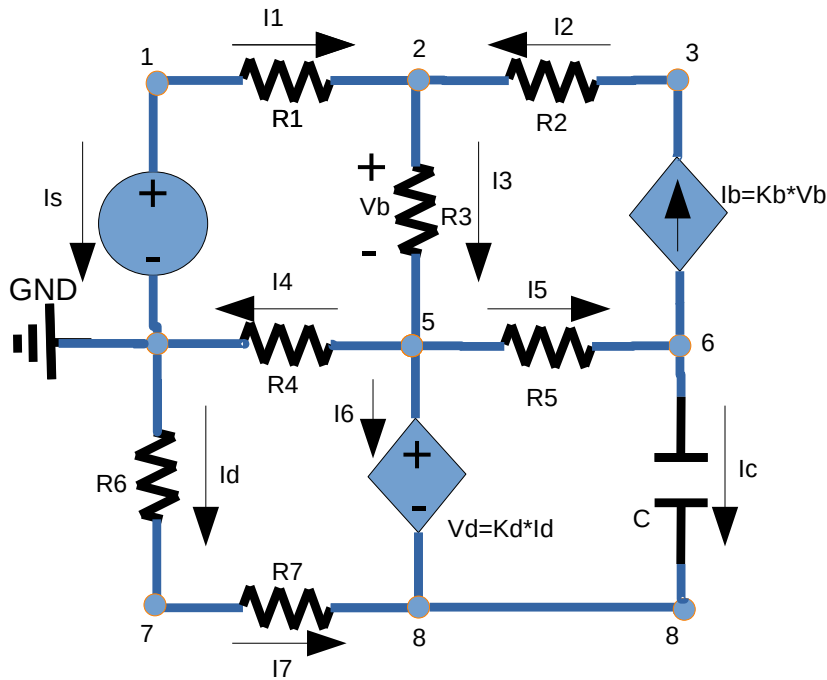


Figure 2: Circuit that was used to obtained the 2.1 equations.

The values that where computed from the system of 8 equations are represented in the next table (table 1).

Name	Value [A or V]
V1	5.0102
V2	4.7774
V3	4.2972
V5	4.8099
V6	5.5204
V7	-1.9313
V8	-2.9274
I1	0.00022595
I2	-0.00023645
I3	-0.000010502
I4	0.0011768
I5	-0.00023645
I6	-0.00095088
I7	0.00095088
Id	0.00095088
Ic	0

Table 1: Theoretical values obtained using octave to solve the equations of Node Method for the expressed conditions. *Current* is expressed in Ampere and *Tensions* are expressed in Volt.

2.2 Determination of the equivalent resistance (R_{eq}) as seen from the capacitor terminals

As suggested in the laboratory task, we made $V_s=0$ and we replaced the capacitor with a voltage source $V_x = V_6 - V_8$, where V_6 and V_8 are the voltages in nodes 6 and 8 (as obtained in 2.1). Then we ran a nodal analysis to determine the current I_x supplied by V_x . Finally we computed the equivalent resistor as $R_{eq} = V_x / I_x$, and the time constant. This procedure is necessary to determine the initial conditions, in this case they correspond to the ones of a saturated capacitor. With the computation of the current that passes through the capacitor, we can obtain the equivalent resistor, which is necessary for the calculation of the time constant, this one will allow us to deduce the natural response of this system. Using the node method one more time to analyse the circuit, we will obtain the next series of equations:

$$(V_3 - V_2) \times G_2 = (V_2 - V_1) \times G_1 + (V_2 - V_5) \times G_3 \quad (8)$$

Node 3:

$$(V_3 - V_2) \times G_2 = K_b \times (V_2 - V_5) \quad (9)$$

Node 6:

$$(V_6 - V_8) = V_x \quad (10)$$

And node 7:

$$(V_0 - V_7) \times G_6 = (V_7 - V_8) \times G_7 \quad (11)$$

The additional equations are:

$$V_1 - v_0 = V_s \quad (12)$$

$$V_5 - V_8 = -K_d \times (V_7) \times G_6 \quad (13)$$

$$(V_2 - V_5) \times G_3 + (V_7 - V_8) \times G_7 = (V_5 - V_0) \times G_4 + K_b \times (V_2 - V_5) \quad (14)$$

The main differences compared to the previous system, are the definition of a super-node that contains the nodes 5, 6 and 8, and the definition of the voltage source. We obtained the next results, from the computation of the equations above.

Name	Value [A, V, Ω or s^{-1}]
V1	0
V2	0
V3	-0
V5	0
V6	8.4479
V7	0
V8	0
I1	0
I2	-0
I3	0
I4	0
I5	-0.0028111
I6	-0
I7	0
Id	-0
Vx	8.4479
Ix	-0.0028111
Req	3005.2
Tau	0.0030845

Table 2: Theoretical values obtained using octave to solve equations of Node Method for the expressed conditions.

2.3 Computation of the natural solution $v_{6n}(t)$, in the interval $[0, 20]$ ms

After we compute the R_{eq} and the current that passes through the capacitor, we can simplify the circuit to a single V-R-C loop where a current $i(t)$ circulates. The voltage source $v_I(t)$ drives its input, and the output voltage $v_O(t)$ is taken from the capacitor terminals. Applying the Kirchhoff Voltage Law (KVL), a single equation for the single loop in the circuit can be written as

$$Ri(t) + v_O(t) = v_I(t). \quad (15)$$

Because v_O is the voltage between capacitor C's plates, it is related to the current i by

$$i(t) = C \frac{dv_O}{dt}. \quad (16)$$

Hence, Equation (??) can be rewritten as

$$RC \frac{dv_O}{dt} + v_O(t) = v_I. \quad (17)$$

Equation (17) is a linear differential equation whose solution is a superposition of a natural solution v_{On} and a forced solution v_{Of} :

$$v_O(t) = v_{On}(t) + v_{Of}(t). \quad (18)$$

As learned in the theory classes the natural solution can be represented by the next equation:

$$v_{On}(t) = Ae^{-\frac{t}{RC}}, \quad (19)$$

where A is an integration constant. As we know the initial conditions, we can obtain the constant A that is going to be equal to V_x . In this way, the natural solution is obtained.

With the results obtained in 2.2), we have determined the natural solution $v_{6n}(t)$, in the interval $[0, 20]$ ms. It was used the capacitor voltage V_x for $t < 0$ as the initial condition.

Using the next equation (knowing V_x and the greek letter tau) we can plot the result, as we can see in Figure 3

$$V_x e^{-\frac{t}{\tau}} = v_{6n}(t), \quad (20)$$

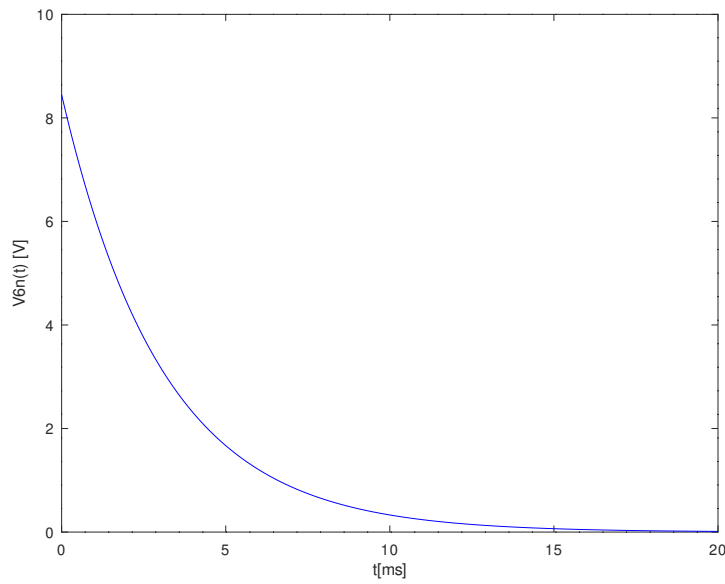


Figure 3: Natural response in v6.

2.4 Computation of the forced solution $v_{6f}(t)$, in the interval $[0, 20]$ ms

To determine the forced solution $v_{6f}(t)$ in the same interval we, as suggested, used a phasor voltage source \tilde{V}_n , replaced C with its impedance \tilde{Z}_c , and we ran the previous nodal analysis to determine the phasor voltages in all nodes.

The next table shows the obtained values.

In this way, as was expected, the only phasor that is not above the real axis, is the one that is not related to the capacitor.

To determine the expression, $v_{6f}(t)$, we had to obtain the gain and the phase delay:

$$\frac{v_6}{v_s} = |\tilde{V}_6| \quad (21)$$

$$\phi = \arg(\tilde{V}_6) \quad (22)$$

$$v_{6f}(t) = |\tilde{V}_6| * \sin(2\pi f + \phi) \quad (23)$$

Name	Value [V]
V1	1
V2	9.5353e-01 + 5.2168e-16i
V3	8.5769e-01 + 8.2277e-16i
V5	9.6002e-01 + 5.0130e-16i
V6	-0.579824 - 0.086773i
V7	-3.8548e-01 - 2.0129e-16i
V8	-5.8430e-01 - 3.0511e-16i

Table 3: Theoretical values obtained using octave to solve equations using phasors for the expressed conditions.

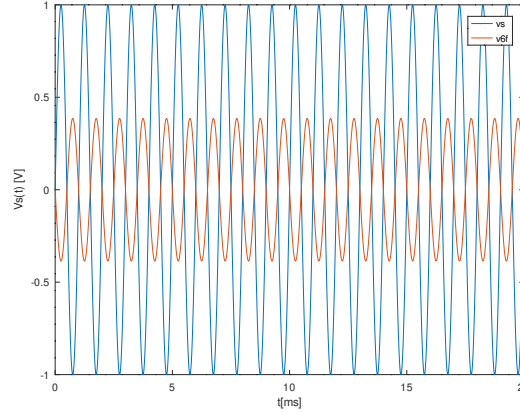


Figure 4: Final total solution $v_6(t)$. The orange function corresponds to the forced solution of $v_6(t)$ and the blue one corresponds to sinusoidal voltage source.

2.5 Computation of the final total solution $v_6(t)$

To determine the final total solution $v_6(t)$, we converted the phasors to real time functions with $f = 1KHz$, and superimposed the natural and forced solutions (as we can see in Figure 5). In this picture we plotted $v_s(t)$ and $v_6(t)$ in a time interval of $[-5,20]$ ms.

$$v_6(t) = V_x e^{-\frac{t}{\tau}} + |\tilde{V}_6| \sin(2\pi f t + \phi) \quad (24)$$

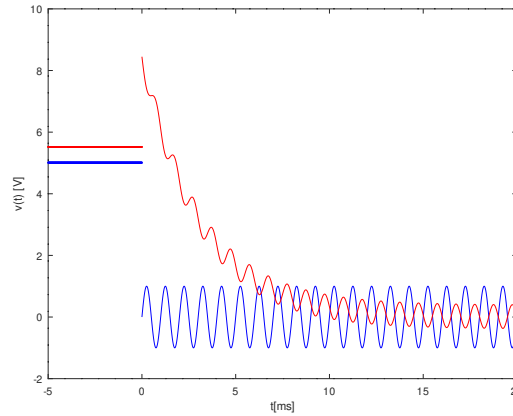


Figure 5: Final total solution $v_6(t)$. The Red function corresponds to $v_6(t)$ and the blue one to $v_s(t)$

2.6 Frequency Responses

In this part it was asked for us to determine the frequency responses $v_c(f) = v_6(f) - v_8(f)$, and $v_6(f)$ and to plot $v_s(f)$, $v_c(f)$ and $v_6(f)$ in the same figure. After we have concluded the given task, we can formulate some conclusions- The behaviour of the capacitor is due to the fact that as the frequency applied to the capacitor increases, its reactance decreases (measured in ohms). Likewise as the frequency across the capacitor decreases its reactance value increases. So, $v_c(t)$ is going to tend to zero with the increase of the frequency, because its impedance also tends to zero. That is, we have a short circuit. If the tension $v_c(t)$ starts tending to zero, this one stops of having influence in $v_6(t)$, and this last stays constant. $v_s(t)$ always have a constant value and a constant phase. The Bode's diagram of $v_c(t)$ allow us to conclude that we are in front of a low-pass filter, that is, this filter is a high frequency attenuater.

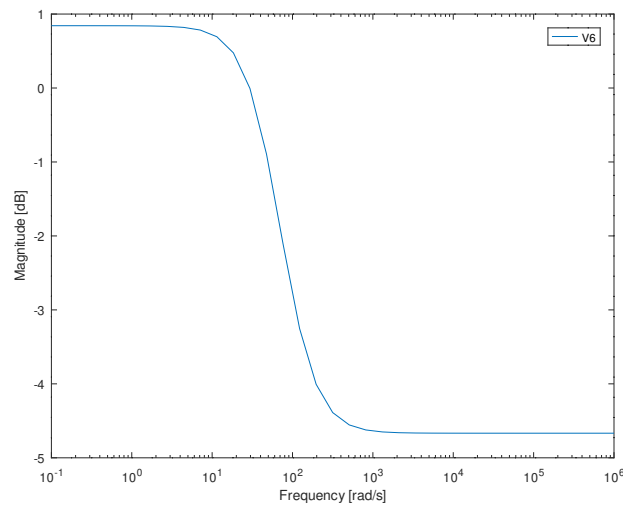


Figure 6: Bode diagram (magnitude in dB's) of $v_6(t)$

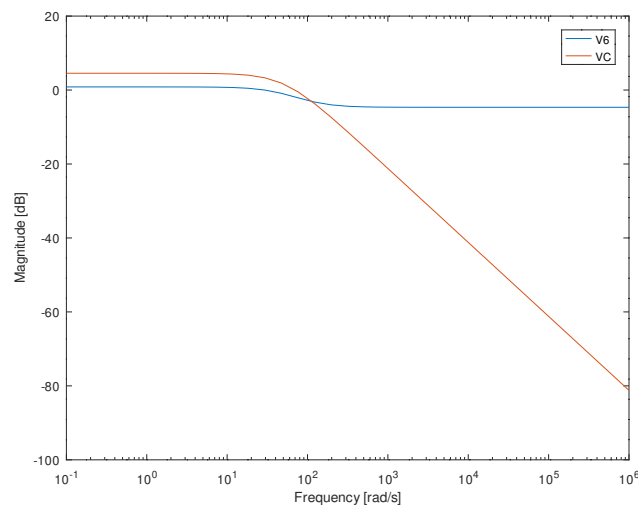


Figure 7: Bode diagram (magnitude in dB's) of $v_6(t)$ and $v_c(t)$

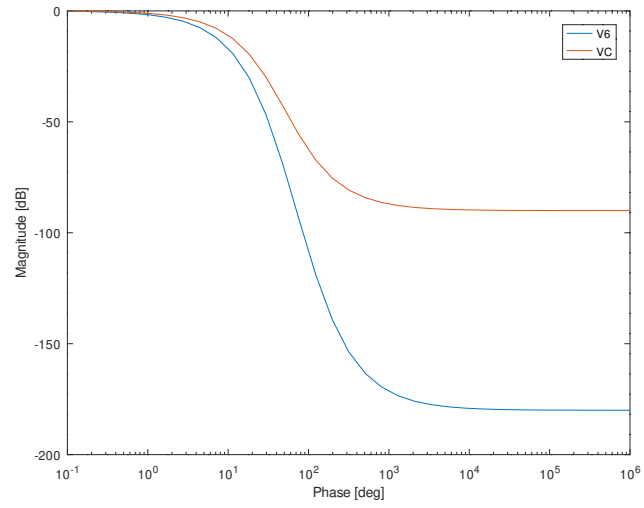


Figure 8: Bode diagram (phase in degrees) of $v_6(t)$

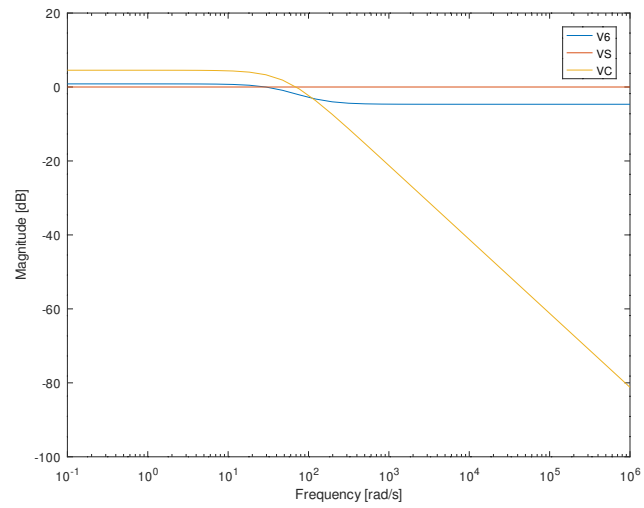


Figure 9: Bode diagram (magnitude in dB's) of $v_6(t)$, $v_c(t)$ and $v_s(t)$

3 Simulation Analysis

3.1 Operating Point Analysis for $t < 0$

Table 4 shows the simulated operating point results for the circuit under analysis. Compared to the theoretical analysis results, we can see that the values are exactly the same.

Name	Value [A or V]
@r1[i]	2.259480e-04
@r2[i]	2.364497e-04
@r3[i]	-1.05017e-05
@r4[i]	-1.17683e-03
@r5[i]	-2.36450e-04
@r6[i]	9.508803e-04
@r7[i]	9.508803e-04
n1	5.010158e+00
n2	4.777353e+00
n3	4.297180e+00
n5	4.809850e+00
n6	5.520426e+00
n7	-1.93130e+00
n8	-2.92744e+00

Table 4: Operating point. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

3.2 Operating Point Analysis for $v_s(t)=0$

Table 5 shows the simulated operating point results for the circuit, this time with the null voltage source and with the replacement of the capacitor by a voltage source $V_x = V(6) - V(8)$. This procedure is necessary to determine the initial conditions, in this case they correspond to the ones of a saturated capacitor.

Name	Value [A or V]
@r1[i]	0.000000e+00
@r2[i]	0.000000e+00
@r3[i]	0.000000e+00
@r4[i]	0.000000e+00
@r5[i]	-2.81109e-03
@r6[i]	0.000000e+00
@r7[i]	0.000000e+00
n1	0.000000e+00
n2	0.000000e+00
n3	0.000000e+00
n5	0.000000e+00
n6	8.447866e+00
n7	0.000000e+00
n8	0.000000e+00

Table 5: Operating point. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

3.3 Simulation of the natural response of the circuit

In this point we have simulated the natural response of the circuit, using the boundary conditions $V(6)$ and $V(8)$ as obtained in 3.2). Then we used Ngspice's transient analysis mode to get $v_6(t)$ in the interval $[0, 20]$ ms. Finally we have plotted the result, as you can see in Figure 10. This plot is equal to the one get in the theoretical analyses

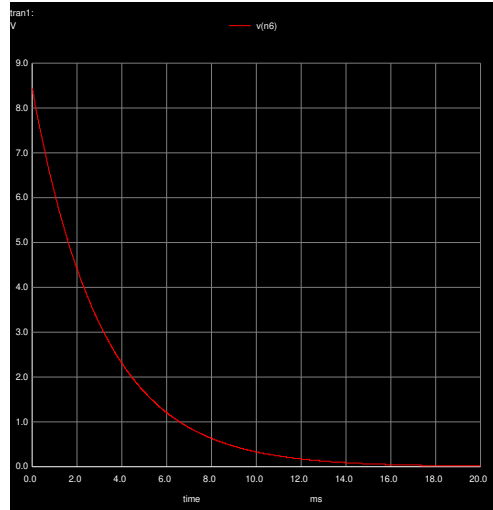


Figure 10: Transient natural response output of voltage V6

3.4 Simulation of the natural and forced response of the circuit

We simulated the natural and forced response on node 6 by repeating step 3) (3.3) with $v_s(t)$ as given in Fig. 1 and with $f=1$ kHz. Then we plotted both the stimulus and the response.

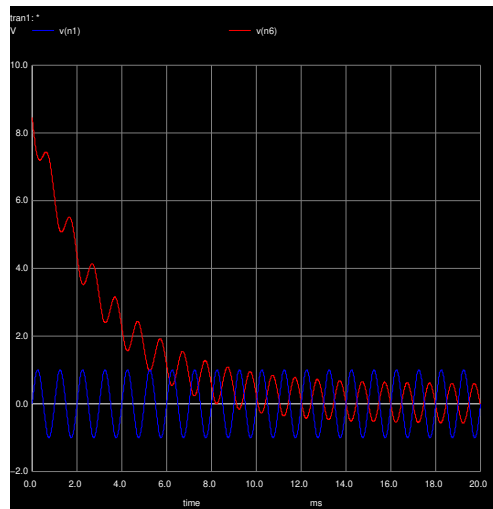


Figure 11: Transient total response output voltage V6

3.5 Simulation of the frequency response in node 6

The next point was to do the response in frequency, as it was already referred, the increase in frequency, decreases the capacitor impedance, this is, the tension will decrease. This is the reason why we observe a negative variation in terms of magnitude in the Bode's diagram, since 10Hz to 10^4 Hz. With the influence of this frequency the variation on the capacitor is so small, that is not going to interfere with v6. As Vs is a voltage source both its magnitude and phase do not change.

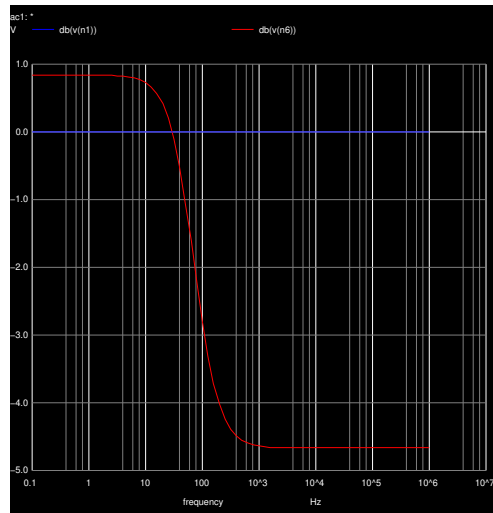


Figure 12: Frequency response (Bode Diagram: Magnitude)

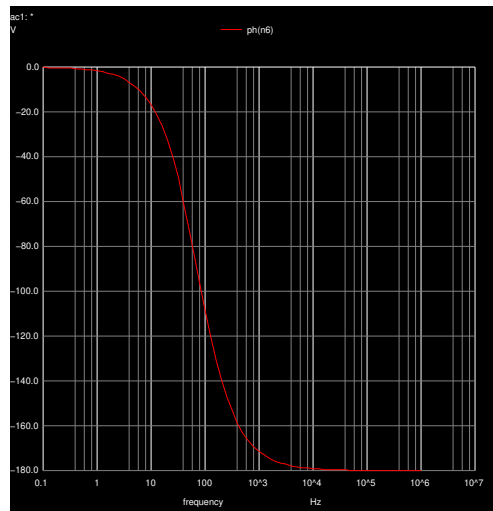


Figure 13: Frequency response (Bode Diagram: Phase)

4 Conclusion

In this laboratory assignment the objective of analysing an RC circuit has been achieved. Static, time and frequency analyses have been performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. The simulation results matched the theoretical results precisely. The reason for this perfect match is the fact that this is a straightforward circuit containing only linear components, so the theoretical and simulation models cannot differ. For more complex components, the theoretical and simulation models could differ but this is not the case in this work.