Processor-in-the Loop Test and Experimental Validations for developed Nine level PV Inverter using High Performance ARM-STM32F407

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Abstract— **In this paper a Single-Phase nine level inverter based on conventional single-phase H-bridge topology is proposed. It is dedicated to be used for ensuring the connection of single AC load to photovoltaic system. The proposed inverter system features less of switches number and a new auxiliary switches conception. Hence, it gives better voltage regulation, smooth operation and efficient yield compared to multi-level inverters. The proposed inverter topology is capable of producing nine levels of output voltage levels. This inverter is firstly simulated under MATLAB/ Simulink software, thereafter, co-simulated using the Processor-in-the-loop (PIL) technique. Secondly, the proposed inverter is designed and tested experimentally. The inverter control is implemented on the high-speed ARM-STM32F407 board. Based on the obtained results, it can be seen clearly that co-simulation results are matching experimental results, which proves the validity of the proposed multi-level inverter. This topology can be extended for more number of phases and levels.**

Keywords: Multi-level inverter, Semiconductor power devices, THD. STM32F407 Board, PIL testing.

I. INTRODUCTION

Nowadays, the rapid development of power electronics inverters have shown an important evolution, where many topologies are proposed to overcome the main existing drawbacks faced with the conventional topology of two-level inverters associated with their bulky output filters. Indeed, one of the main solution that is proposed along the last decade is the multilevel inverters, which allows producing a nearly sine waveform, associating smaller output filters, less harmonic content, less switching loss, less voltage stress, low EMI level, and less volume and weight [1-3]. Three basic topologies were proposed, the first multilevel is the neutral-point-clamped (NPC) inverter which requires special modulation techniques to control the inherent oscillations in voltages across the series connected, which become difficult at higher number of voltage levels [4]. Moreover, a significant increase in the number of clamping diodes renders this topology very complex and less efficient at higher number of voltage levels [5-7]. The second topology is the flying capacitor (FC) multilevel inverter where the voltages across the capacitors are used for generating different voltage levels [8]. Many more schemes are proposed for the balancing the capacitor voltages in the FC topology. However, as the number of levels in voltage increases, the FC circuit becomes complex, due to substantial increase in number of capacitors. The third topology is the cascaded H-bridge (CHB) multilevel converter, which employs series connection of H-bridge cells supplied from isolated DC voltage sources. The major limitation of this topology is the requirement of multiple DC voltage sources, as each H-bridge cell requires a DC source [9,10]. In addition to the aforementioned basic multilevel inverter topologies, a number of new topologies for different applications are proposed, which are all based on the hybridization of the basic topologies such as the hybrid-clamped multilevel inverter topology [11], neutral point clamped converters with coupled inductors [8]. However, many other new topologies have been proposed in the past few years [7].

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This paper describes the development of a simplified single-phase nine-level inverter based on H-bridge topology as well as a new structure of auxiliary switches as shown in Fig.1 & 2, and detailed in section II. This inverter is co-simulated using the process-in-the-loop (PIL) concept in order to check the validity of its control. This inverter with proposed topology is physically developed, where its control is implemented on the STM32F407 Board. The obtained results are very satisfactory when the system is tested experimentally.

II. Power Circuit Operation

The proposed single-phase multilevel inverter has the following merits over other existing multilevel inverter topologies.

1) It consists of single-phase conventional H-bridge inverter, bidirectional auxiliary switches (number varies depending upon level) and a capacitor voltage divider formed by capacitors.
2) Improved output waveforms.
3) Smaller filter size.
4) Lower electromagnetic interference (EMI) and total harmonic distortion (THD).
5) Reduced number of switches employed.
6) Less complexity of the circuit as the levels increase.
7) Attains minimum 40% drop in the number of main power switches required. Moreover, since the capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multilevel configurations.

The proposed single-phase simplified nine-level inverter was developed from the five-level inverter in [15]-[16]. It contains a single-phase conventional H-bridge inverter, three supplementary switches S5, S6, S7 and a capacitor voltage divider formed by four capacitors namely Cl, C2, C3 and C4, as illustrated in Fig. 2.

The supplementary switches, formed by the controlled switch S5, S6 and S7.The single-phase simplified nine-level inverter proposed power circuit with supplementary switches is shown in Fig.1.

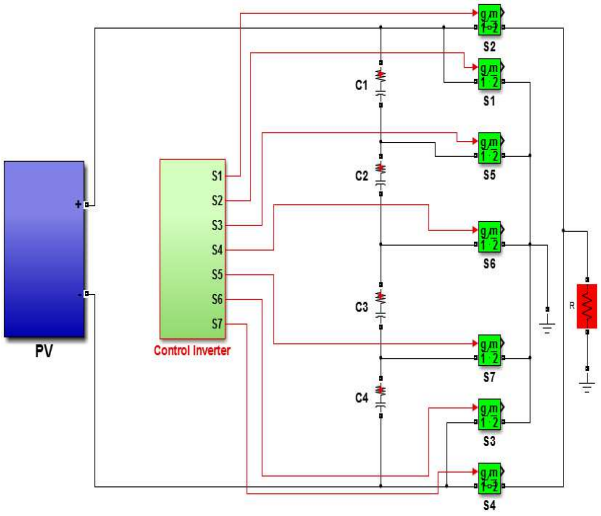


Fig.1. Simplified nine-level inverter proposed power circuit.

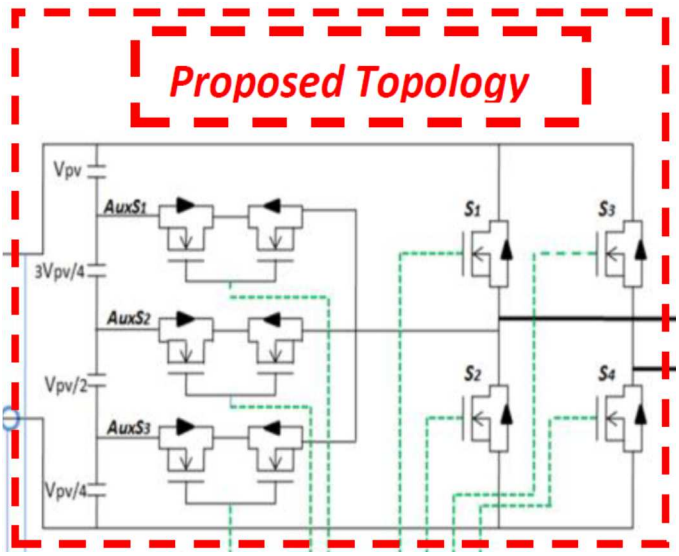


Fig. 2. Single-phase nine level proposed topology

The proposed single-phase simplified nine-level inverter is capable of producing nine different levels of output-voltage levels (Vpv, 3Vpv/4, 2Vpv/4, Vpv/4, 0, - Vpv/4, -2Vpv/4, -3Vpv/4, -Vpv) from the dc supply voltage Vpv, shown in Fig. 3.

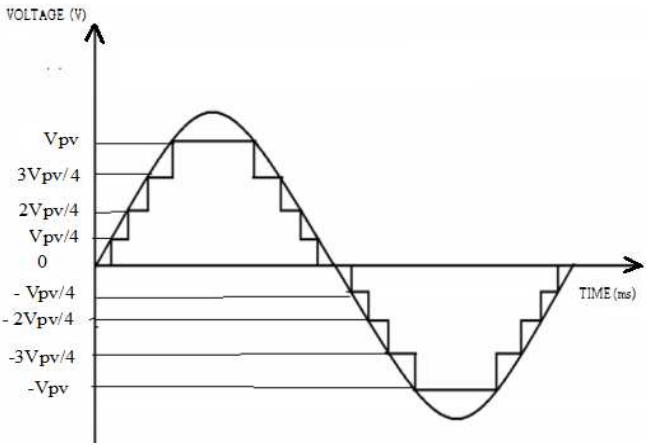


Fig. 3. Single-phase proposed output voltage waveform

The required nine levels of output voltage are generated as follows and can be easily understand by the table. I.

A. Mode Operation:1

The switch S1 is ON, connecting the load positive terminal to Vpv, and S4 is ON, connecting the load negative terminal to ground. Remaining switches S2, S3, S5, S6 and S7 OFF; the voltage across the load terminals R is Vpv.

B. Mode Operation:2

The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. Remaining switches Sl, S2, S3, S6 and S7 are OFF; the voltage across the load terminals R is 3Vpv/4.

C. *Mode Operation:3*

The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. Remaining switches Sl, S2, S3, S5 and S7 are OFF; the voltage across the load terminals R is 2Vpv/4.

D. *Mode Operation:4*

The bidirectional switch S7 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. Remaining switches Sl, S2, S3, S5 and S6 are OFF; the voltage across the load terminals R is Vpv/4.

E. *Mode Operation:5*

This mode of operation has two possible switching combinations. Either switches S3 and S4 are ON, remaining switches S1, S2, S5, S6 and S7 are OFF or Sl and S2 are ON, remaining switches S3, S4, SS, S6 and S7 are OFF. In both switching combinations terminal ab is short circuited, hence the voltage across the load terminals R is zero.

F. *Mode Operation:6*

The switch S2 is ON, connecting the load negative terminal, and bidirectional switch S5 is ON, connecting the load positive terminal to ground. Remaining switches Sl, S3, S4, S6 and S7 are OFF; the voltage across the load terminals R is -Vpv/4.

TABLE I: Switching combinations required to generate the nine-level output voltage waveform

Operation Mode	V_{Load}	S1	S2	S3	S4	AuxS1	AuxS2	AuxS3
Mode 1	Vpv	1	0	0	1	0	0	0
Mode 2	3Vpv/4	0	0	0	1	1	0	0
Mode 3	2Vpv/4	0	0	0	1	0	1	0
Mode 4	Vpv/4	0	0	0	1	0	0	1
Mode 5	0	1	0	1	0	0	0	0
	0	0	1	0	1	0	0	0
Mode 6	(-)Vpv/4	0	1	0	0	1	0	0
Mode 7	(-)2Vpv/4	0	1	0	0	0	1	0
Mode 8	(-)3Vpv/4	0	1	0	0	0	0	1
Mode 9	(-)Vpv	0	1	1	0	0	0	0

G. *Mode Operation:7*

The switch S2 is ON, connecting the load negative terminal, and bidirectional switch S6 is ON, connecting the load positive terminal to ground. Remaining switches Sl, S3, S4, S5 and S7 are OFF; the voltage across the load terminals R is -2Vpv/4.

H. *Mode Operation:8*

The switch S2 is ON, connecting the load negative terminal, and bidirectional switch S7 is ON, connecting the load positive terminal to ground. Remaining switches Sl, S3, S4, S5 and S6 are OFF; the voltage across the load terminals R is -3Vpv/4.

I. *Mode Operation:9*

The switch S2 is ON, connecting the load negative terminal to Vpv, and S3 is ON, connecting the load positive terminal to ground. Remaining switches Sl, S4, S5, S6 and S7 are OFF, the voltage across the load terminals R is -Vpv. In the nine-level inverter circuit three capacitors in the capacitive voltage divider are connected directly across the dc supply voltage Vpv and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the three capacitors is automatically restored.

III. PROCESSOR-IN THE-LOOP AND SIMULATION RESULTS

Processor-in-the-loop (PIL) is recognized as a competent simulation tactic allowing the test of control systems before applied in real system, where some of the control-loop components are implemented in real hardware device as ARM-STM32F407 board and some are simulated in Matlab. Typically, the Input/output ports and the peripherals are used as an interface between the plant simulation (Matlab) and the embedded system (STM32F407) under test, as shown in Fig. 4.

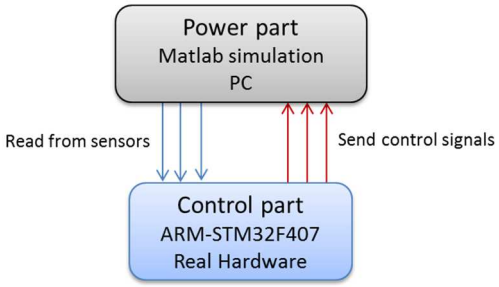
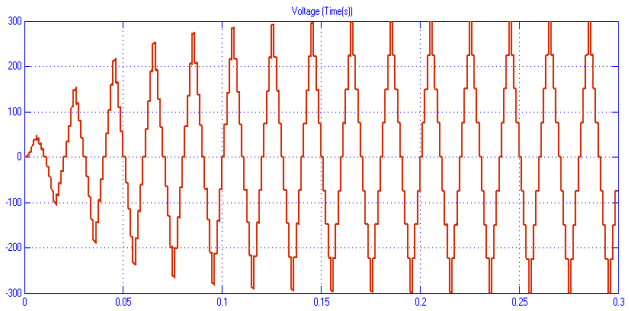
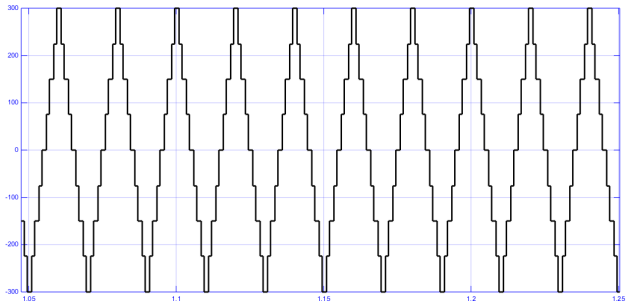


Fig. 4. The PIL Model using STM32F407 and Matlab Simulink.



(a)



(b)

Fig. 5. Output voltage waveform of the simplified nine-level inverter proposed circuit.(Vpv bus =300V)

Figure 5.a shows the simulated nine-level output voltage waveform under MATLAB/Simulink. From this waveform, the first part time (0s to 0.15s) indicates that the output voltage inverter is tracking the reference voltage. The length of this part is based on the efficiency of the Phase Locked Loop (PLL) applied with the PV system.

The second test is the Processor-in-the-loop (PIL) test. For this test, there are two main parts; the control part, where the inverter control is integrated in the embedded board, and the power part still running on MATLAB/Simulink. The output voltage results given from PIL testing shown in the Fig.5.b.

All the results are clearly visible that, the simulated and co-simulated output waveforms are very close to the ideal output defined for a proposed nine-level simplified inverter circuit. The nine-levels of voltages are:

Vpv =300V, 3Vpv/4= 225V, 2Vpv/4 = 150V, Vpv/4 =75V, OV, - Vpv/4 = -75V, -2Vpv4 = -150V, -3Vpv4 = -225V, -Vpv= -300V.

IV. EXPRIMENTAL VALIDATION

The implementation of the proposed single-phase nine-level inverter was based on semi-conductor metal–oxide–semiconductor field-effect transistor MOSFET switches (type IRF840).Four switches are used as principal ones for ensuring the function of the single bridge. Whereas, six switches are used two by two as auxiliary switches to ensure the T-type topology. On the same time, the two groups are used in series but in reverse direction with two diodes to satisfy the criteria of bidirectional controlled switches, which are reversible in current and voltage. These used switches are controlled via the special gate drives, which they are based on TLP250 to guarantee a good isolation between the control circuit and the power switches. The control of the switches and the measurements signals are ensured by using the embedded board (ARM-STM32F407), adapted to work with relatively higher sampling time. The whole setup is shown in Fig.6, whereas, the principle of operation of the setup is shown in Fig. 7. The experimental validation is carried out based on two techniques, the first one is the conventional technique based on the well-known triangular-sinusoidal PWM and the second one, is the square control technique. The harmonic content and the FFT analysis for the both techniques of the output voltage are presented in Fig. 8. The left side of this figure is corresponding to the new proposed control technique and the right one is corresponding to the conventional PWM.

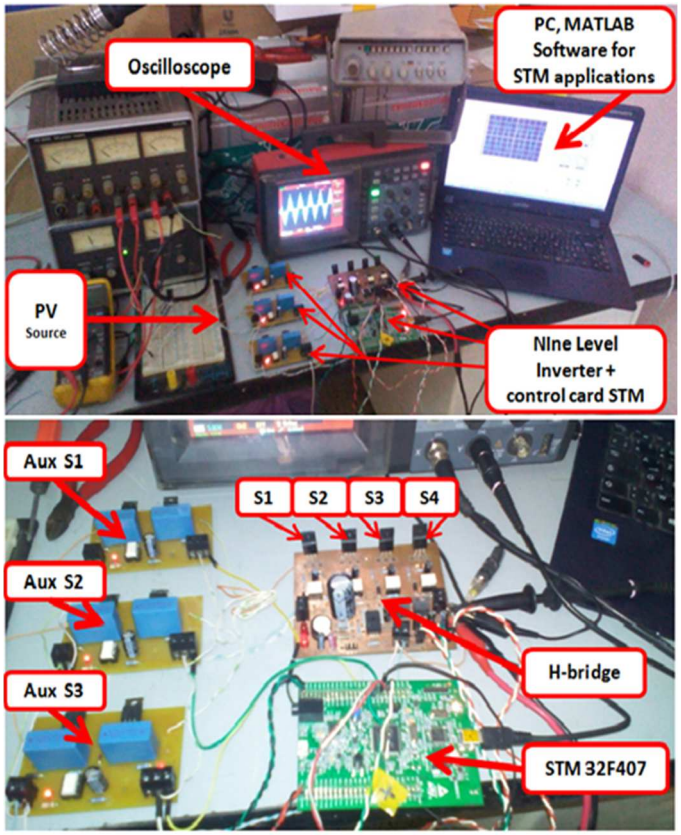


Fig 6. Block diagram of the experimental setup.

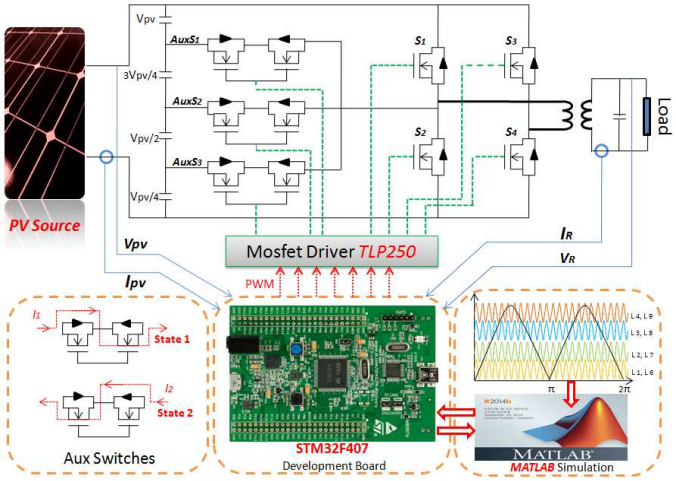


Fig 7. A laboratory experimental prototype of the nine level PV inverter.

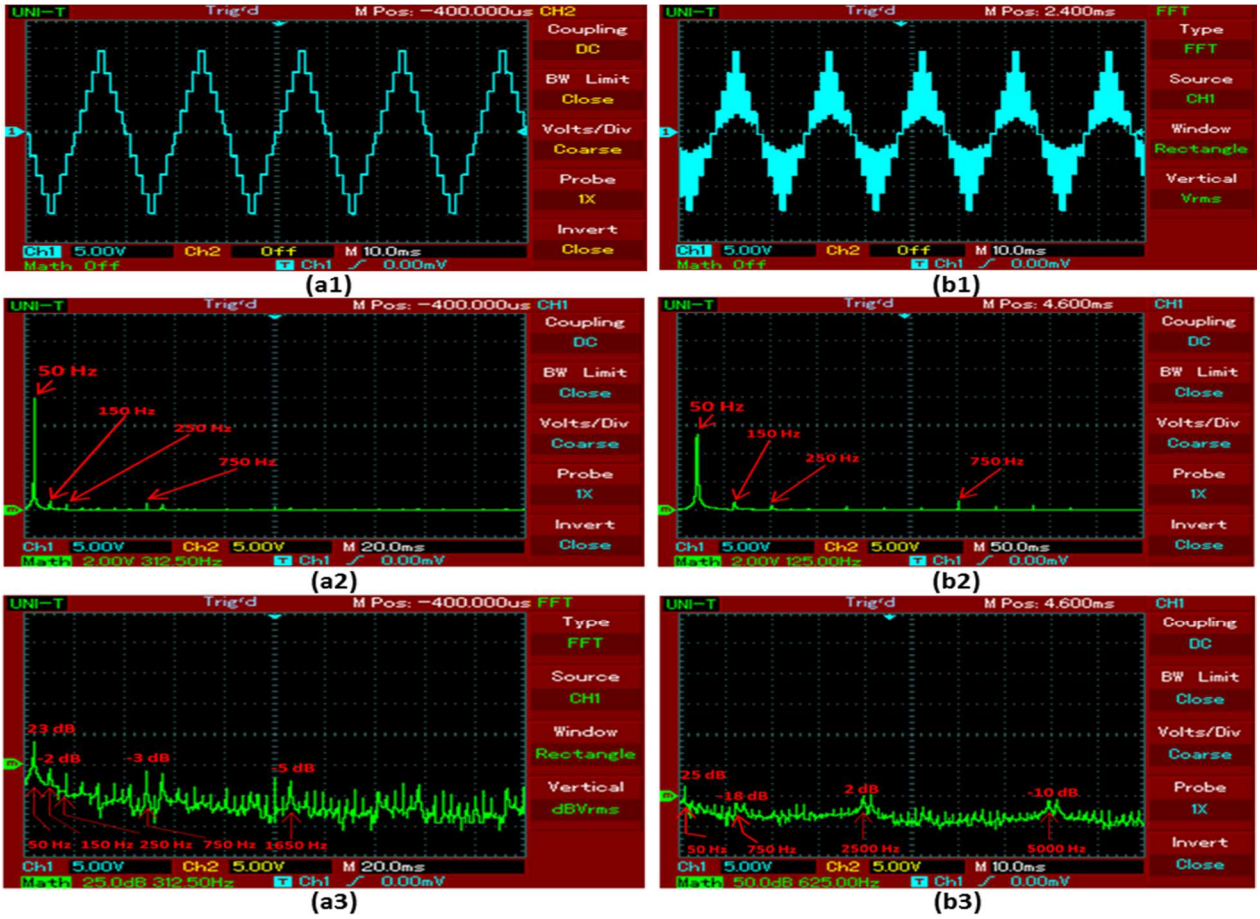


Fig 8. Proposed control: a1: Output voltage waveform, a2: the Spectral content and a2: FFT analyses using square control. PWM control: b1: Output voltage waveform, b2: the Spectral content, b3: FFT analyses using PWM control.

V. CONCLUSION

In this paper, we propose a nine-level single-phase inverter with reduced switches compared to a common multi-level inverter. The performance of the multilevel inverter with proposed topology is experimented and analyzed in detail. Furthermore, with this topology, we notice enhanced output waveforms and lower THD in the nine-level inverter compared to that of PV inverters connected to multiple levels. The designed nine-level single-phase inverter can be adapted to any number of voltage levels for many other applications.

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