PIL Test for Voltage Source Inverter control used in Off-grid PV system

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***Abstract*- This paper treats the case of the off-grid photovoltaic (PV) system, feeding a three-phase resistive load and working only during sunlight availability. In this case, backup batteries are not used. So, no charge controller is needed, neither any DC-DC power converter as long as the PV generator (PVG) delivers a voltage greater to a certain value that keeps good functionality of the inverter. Thus, this PV chain is reduced only to PV array and three-phase voltage source inverter (3-ph-VSI), followed by (delta/wye) transformer. The discrete virtual Phase Locked Loop (PLL) is used to generate a fixed frequency (50 Hz). The proposed system topology allows designing a low cost system, and providing necessary power that can meet the daytime load demand. Next, Processor in the Loop (PIL) method is performed in order to test the hardware implementation of the inverter control algorithm already simulated with MATLAB/ Simulink. This is done by creating the PIL block which will be run in the STM32F407-VG discovery board, while the plant model will be simulated in the host computer. The ST-LINK communication interface is used to connect the host computer to the embedded board.**

Keywords: PV, PLL, VSI, PIL, STM32F407 Board

I. INTRODUCTION

Photovoltaic Generators (PVGs) have undergone of intense development. They are proving to be of particular interest in the case of PV generators that are not connected to the grid, commonly known as the off-grid PV systems [1-2]. These systems are installed on their own or in combination with another dispersed electrical generator [3].

Many attempts are made to optimize such systems. Most of them deal with systems using batteries [2,4]. In this case, solar charge controller is essential. The types of charging method are mainly based on the Pulse Width Modulation (PWM) [5] or on Maximum Power Point Tracking (MPPT) [6]. Also, battery maintenance is necessary for proper functioning, safety, and the PV system lifetime, increasing consequently the costs. Further, in order to provide 3-ph voltage in such system, a basic inverter control is the most used such as, Space-Vector Modulation (SVM) or 3-ph carrier-based PWM [7-8].

In this study, we propose an off grid PV system topology without storage facilities. In this case, the inverter control is totally different of those cited before. Indeed, the inverter input is a variable DC voltage delivered directly by PVG, and depends on temperature and irradiance levels [9]. This inverter input voltage which is also the (PVG) output voltage must exceed a certain value that keeps good functionality of the inverter. While, the inverter output voltage must be regulated at desired 3-ph voltage and frequency. So, the demand of the loads side determines the suitable inverter control parameter. Thus, it is very difficult to obtain stable and precise control of the 3-ph voltage without limiting the current flowing through the inverter, and therefore limiting operating the PV array at peak efficiency. Also, the nature of the loads defines the current to be delivered by the inverter which may be linear or non-linear. It may have an unknown quantity of harmonics limiting thereby the use of the current control loop. Consequently, a voltage control loop is used instead of current control loop. Such inverter control mode is dedicated mainly to ensure a quality of the voltage waveform (low THD).

The inverter 3-ph output voltage is amplified by (delta-wye) 3-ph transformer (110V/380V) to desired AC Voltage (380V) required by the loads. The discrete virtual 3-ph PLL [9] is used to generate fixed frequency (50 Hz) needed by the loads to work properly.

This proposed off grid PV system can be useful for small scale [4] such as water pumping [10-12]. It can be exploited only during daytime, mainly in rural areas where there is no grid connection.

Once the inverter control algorithm is validated using Matlab/Simulink (controller and plant are executed in the same software environment), the PIL simulation test will be performed in order to test the hardware implementation of this control algorithm [13].

To achieve PIL simulation test, many methods can be found in the literature [13-15]. Among these methods, is by configuring a Simulink model to run PIL block simulations on the STM32F407-VG discovery board. The code is generated from the inverter controller model for the chosen embedded board in order to create the PIL block. This is done by using the target's compiler and embedded coder tool.

The created PIL block which is run in the STM32F407-VG discovery board is connected to the PV plant model

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so as to acquire measured instantaneous 3-ph Voltages of the Y-connected load (V_{abc}) and the desired voltage reference (V_{ref}). While, the plant model still running on the host computer. After that, the PIL block computes the 3-ph modulating signal (U^*_{abc}) needed for the 3-ph VSI control, and send it to the plant as shown in Figure.1.

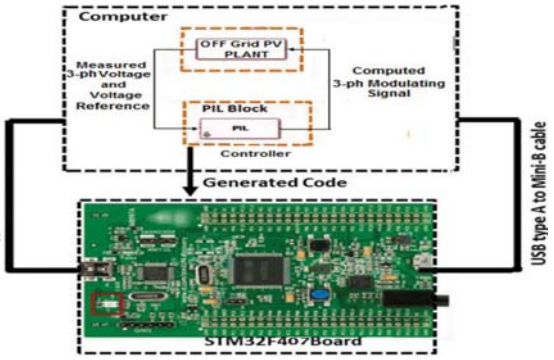


Fig.1. General Scheme of the PV system using PIL block

In order to configure a Simulink model to run PIL block simulation, additional steps must be done:

- ✓ The PIL verification must be enabled.
- ✓ The STM32F4 Discovery is selected as target hardware.
- ✓ Baremetal as operating system (OS) is also selected.
- ✓ The ST-LINK is used as communication interface between the board (target) and computer (host).The USB type A to Mini-B cable to connect them.

Finally, the Simulation results show the validity of the model under variable irradiance and temperature to provide necessary power that can meet the daytime load demand. They also demonstrate the efficiency of the proposed algorithm using PIL technical without using any costly additional devices.

II. STUDY SYSTEM PRESENTATION

The Study system contains, Figure.2:

- ❖ PVG 4000Wc (KC200GT modules),
- ❖ 3-ph VSI,
- ❖ 3-ph VSI controller block,
- ❖ Inductive filter (L=2.49 mH),
- ❖ 3-ph transformer (delta 110 / wye 380 Volts),
- ❖ Circuit-breaker (activated after 0.5 s) to connect two 3-ph resistive loads (Load1: 1500W and Load2: 500W)

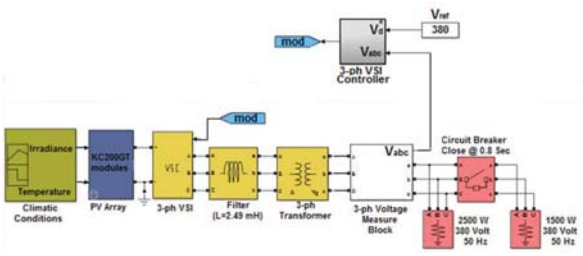


Fig.2.Off-grid PV system diagram under Simulink

II.1. Single-Diode PV Cell Modeling

The photovoltaic cell is modeled by a simple one diode model. Equivalent circuit of the PV cell model is represented in Figure.3, [16-17].

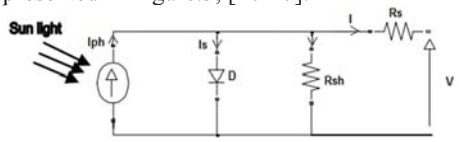


Fig.3. One diode model of PV cell.

The developed current by PV cell is given by (1), Figure.3, [17]:

$$I = Iph - Is\left(e^{\frac{q(V+Rs*I)}{nKT}} - 1\right) - \frac{(V+Rs*I)}{Rsh} \quad (1)$$

Iph: Current (A) generated by the incident light,
K : Boltzmann constant = 1.381 10^{-23} J/k,
q : Electron charge=1.602 $^{-19}$ C,
n : Diode ideality constant,
Is : Leakage current of the diode (A),
Rs : Series resistance (Ω),
Rsh : Shunt resistance (Ω).

PV cell model single diode can be represented in similink by Figure.4.

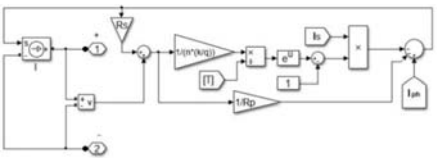


Fig.4. PV cell model in Simulink (single diode)

II.2. Transformer (delta/wye) characteristics

The use of the transformer depends on the DC voltage and therefore on the 3-ph VSI output voltage. Its use is nevertheless useful for galvanic insulation.

[V1 Ph-Ph (Vrms), V2 Ph-Ph (Vrms)] = [110 380]

III. 3-PH VSI CONTROL

In our designed topology, the 3-ph VSI converts the variable DC voltage delivered by the PV array to a fixed 3-ph AC voltage (380 V) with desired frequency (50Hz), using a specific control as described in Figure.5.

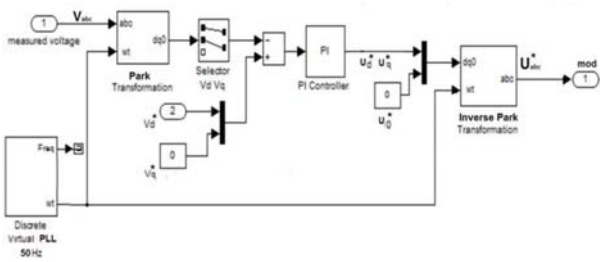


Fig.5. 3-ph VSI Controller block under Simulink

Active and reactive powers of the 3-ph VSI are controlled independently. The voltage reference (Vref) is used to set the desired output voltage magnitude (380V). It also represents direct component reference (v^*_d) and in the meantime the active power reference. Whereas, the quadratic component (v^*_q) represents the reactive power reference and set to 0.

The PI controller outputs(u^*_d , u^*_q) described in (2), are nothing but the d-q components of the 3-ph modulating signal (u^*_{abc}), used to control the 3-ph VSI. Figure.5

$$\begin{cases} u^*_d = PI(v^*_d - v_d) \\ u^*_q = PI(v^*_q - v_q) \end{cases} \quad (2)$$

PI refers to proportional–integral controller

$$\text{With, } \begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_{abc/dq} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3)$$

Where , $T_{abc/dq}$ is the park transformation [18-19].

v_{abc} are the instantaneous 3-ph Voltages measured across the Y-connected load.

Discrete Virtual PLL [20] to set the desired frequency at 50 Hz. The Phase angle is thereafter deduced and used in park transformation.

$$\text{Finally , } u^*_{abc} = \begin{bmatrix} u^*_a \\ u^*_b \\ u^*_c \end{bmatrix} = T_{dq/abc} \begin{bmatrix} u^*_d \\ u^*_q \end{bmatrix} \quad (4)$$

Where, $T_{dq/abc}$ is the inverse park transformation [19].

III.1. DC Bus Voltage calculation

The 3ph-VSI requires a DC voltage input equal at least to a voltage value represented by (5) : [21]

$$Vdc = \frac{2.\sqrt{2}.VLL}{\sqrt{3}.\ m} \quad (5)$$

VLL represents the Line to line RMS Voltage. m is the modulation index, (generally taken between 0.85 and 0.9).

In our case, the 3ph-VSI output Voltage VLL is the voltage of the transformer primary winding (110 V). So, Vdc must be greater to 200 Volts according to (5).

IV. SIMULATION RESULTS AND DISCUSSION

In this simulation, we consider the 4 kW PV array uses KC200GT modules. The array consists of 2 strings of 10 modules connected in series (10*2*200 = 4 kW).

Table.1 [22]: KC200GT electrical datasheet at STC

Parameters	Index	Values
Maximal Power	Pmax	200 W
Open Circuit Voltage	Voc	32.9 V
Short Circuit Current	Isc	8.214 A
Temperature coefficient for Voc	Tc_Isc	- 0.1230 V/K
Temperature coefficient for Isc	Tc_Voc	0.0032 A/K
Series Resistance	Rs	0.221 Ω
Parallel Resistance	Rp	415.405 Ω
Diode quality factor	a	1.3
Number of Cells in Series	ns	54

IV.1. Simulation results

The Irradiance and the temperature profiles are defined by a Signal Builder block which is connected to the PV array inputs. Figure.6.

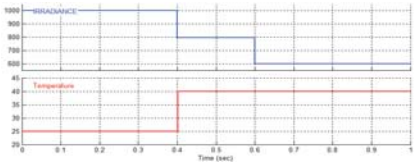
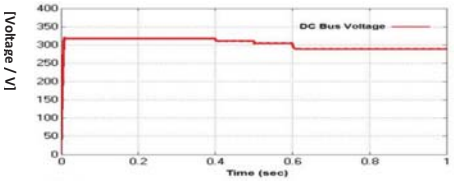
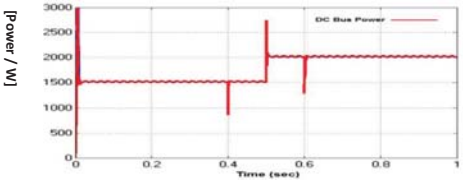


Fig.6. Scenarios of irradiance and temperature.

When we run simulation for 1s; we obtain the following results:



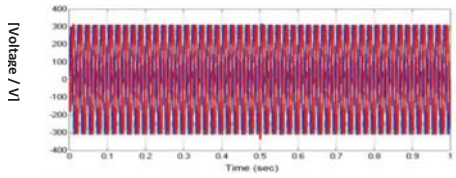
(a)



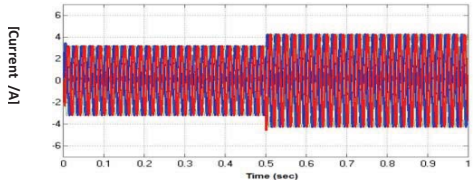
(b)

(a) DC Voltages ; (b) DC Powers.

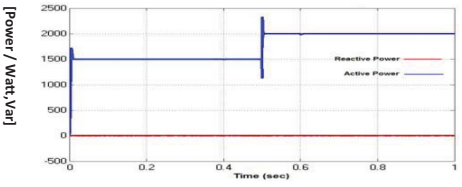
Fig.7. DC bus voltage and power results



(a)



(b)



(c)

(a) Inverter line-to-ground Voltage .Vabc_inv;
(b) Inverter Current Iabc_inv;
(c) Active & Reactive Power PQ_inverter

Fig.8. AC bus of voltage, current and power results

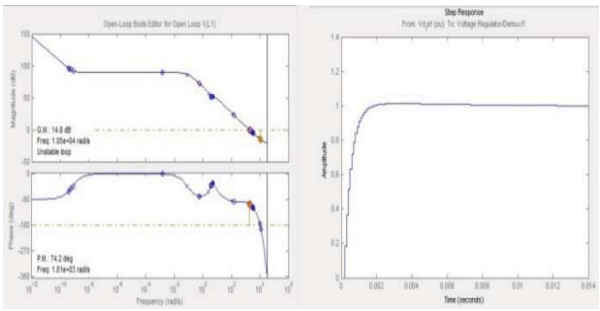
IV.2. Results discussion

From t = 0 to t = 0.5s, the PVG feeds the load of 1500 Watts. The breaker is thereafter activated at 0.5 s to connect the second load of 500 Watts.

The simulation results presented in Figure.9 and Figure.10, show that the control of the 3-ph VSI to a desired set point voltage for a variable load, will limit the current flowing through the 3-ph VSI. Thus, the PV array not necessarily operates at peak efficiency.

In the other hand, Figure.(8.a) shows the voltage control loop regulates well the 3-ph output voltage of the 3-ph VSI at desired reference value (380V) as expected . This later remains constant even for load variations or different climatic condition.

However, the transients of power on the DC side and active power on the AC side present a large overshoots, as shown in Figure.(7.b) and Figure.(8.c). This occurs exactly when the two loads are connected at 0.5 s. To improve their signals quality and reduce their overshoots, Simulink control design is used in order to adjust PI controllers. This later is based on Ziegler-Nichols tuning method [23]. Moreover, it allows linearizing the model by Bode and Step response diagrams [24] , where, controllers can be interactively designed against requirements in the time and frequency domain as shown in Figure.(9).

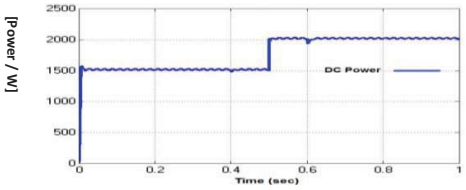


(a) (b)

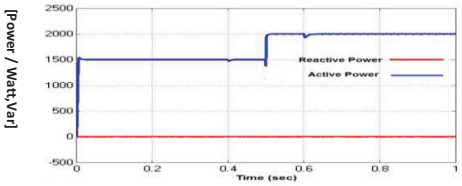
(a) Bode diagram ; (b) Step response

Fig.9. Bode and step response diagrams

The PI controller is adjusted using bode diagram presented in Figure.(9.a) until obtaining good response step as shown in Figure.(9.b). This improves the powers signal quality with less overshoot as shown in Figure.(10). The corresponding PI controller values in this case are stored (P= 0.189; I= 62.939).



(a)



(b)

DC Power ; (b) Active & Reactive Power PQ_inverter

Fig.10. DC & AC Active Powers after tuning PI controller

V. CODE VERIFICATION AND VALIDATION WITH PIL TEST

This section shows how to use Simulink Support Package for STM32F Hardware for code verification and validation using PIL.

V.1. Different steps to configure the Model for Supported STM32F Hardware.

The objective here is to create a PIL block [7] out of the Controller subsystem that will run on the STM32F hardware. Next, the code is generated and implemented in the S-function block provided by Simulink. This PIL block is connected to the plant model (PVG, 3-ph VSI, and Transformer).

Here are, the brief steps to follow in order to reach this purpose. Figure.11, Figure.12, Figure.13 and Figure.14.

1. In the Simulink model, click Simulation > Model Configuration Parameters to open Parameters dialog.
2. Select the Hardware Implementation panel and select STM32F Discovery hardware from Hardware board drop Menu .Do not change any other settings.
3. Choose PIL as Target hardware Resources drop menu.
4. Choose ST-Link as PIL communication interface.

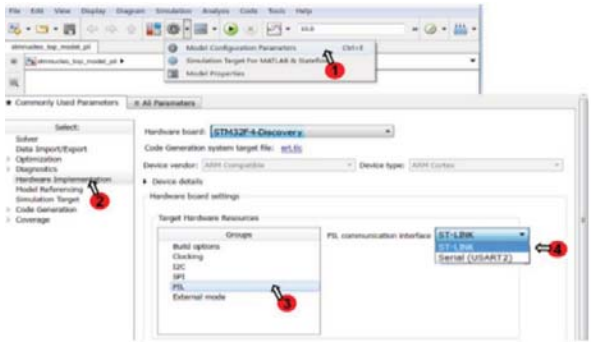


Fig.11. Selection of STM32F407 discovery board.

5. Click on all Parameters

6. Click on Code Generation and in Advanced parameters to create a PIL block.

Fig.12. PIL block creation

7- Click on Code Target.

8- Choose Baremetal as an operating system (OS), for its efficiency and full visibility of the scheduler code.

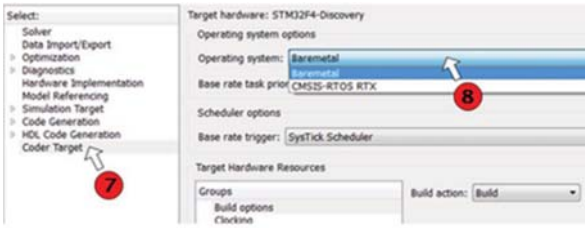


Fig.13. Selection. of Operating System (OS)

9. Run PIL simulation .Figure.14.

The STM32F407 board which contains the controller model is connected to the computer which contains the plant model.

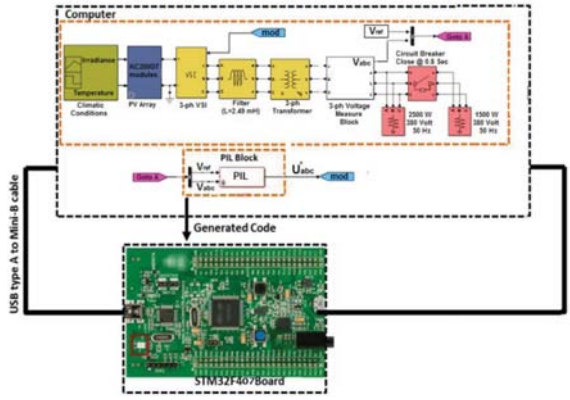
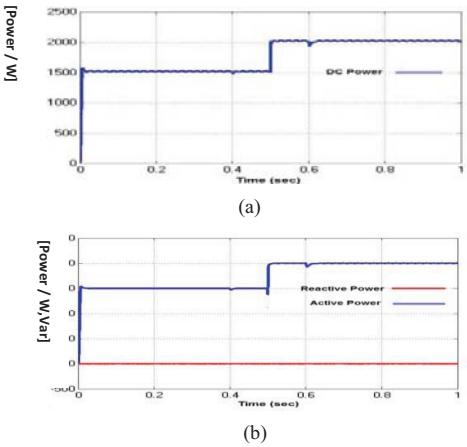


Fig.14. PIL test simulation using STM407 Board

PIL block which is connected to the plant model computes the 3-ph modulating signal (U^*_{abc}) needed for 3-ph VSI control. This later is fed back into the Simulation to drive the virtual environment as shown in Figure.14.

V.2. PIL simulations Results



a) DC Power ; (b) Active & Reactive Power PQ_inverter

Fig.15. DC & AC Active Powers using PIL test

V.3. Results discussion

The result obtained using PIL test is presented in Figure.15 and compared with the normal simulation mode presented in Figure.10. It shows very clearly that the both results are similar.

VI. CONCLUSION

This paper presents a simple off grid PV system topology with its control strategy. Simulation results show the performance of the chosen control law for the 3-ph VSI, and system capability to provide necessary power that can meet daytime load demand. They also demonstrate its ability to regulate well the 3-ph output voltage at desired level, regardless of the climatic conditions or the load variation.

Further, among different topologies employed, the configuration proposed simplifies the final system design with less cost and less installation complexity. Indeed, the PV chain devices are reduced to PVG and 3-ph VSI followed by Delta-Wye transformer, without any DC-DC power electronic converter neither batteries bank.

Next, by using PIL test, the hardware implementation of the proposed control algorithm for the 3-ph VSI is validated. The generated code which is implemented by the PIL block is run in the STM32F407-VG discovery board, while, the plant model is simulated in the host computer. Both are run at the same time and exchange data based on this control algorithm. The obtained simulation results for the PIL test are in total accordance with results of the first normal simulation.

The PIL verification process described in this paper is very easy to use and set up. It provides an excellent tool with low-cost solution to validate control algorithm without physical presence of the power stage. It can be very useful for performing various tests that would be difficult to do on the real hardware.

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