Experiment No. 5:-

Design and implementation of 4 bit parallel binary adder

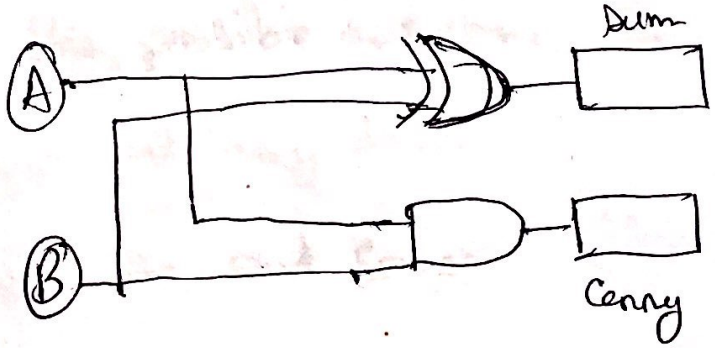
Objectives:

- Binary addition with half adder and full adder
- 4bit parallel order addition and substraction

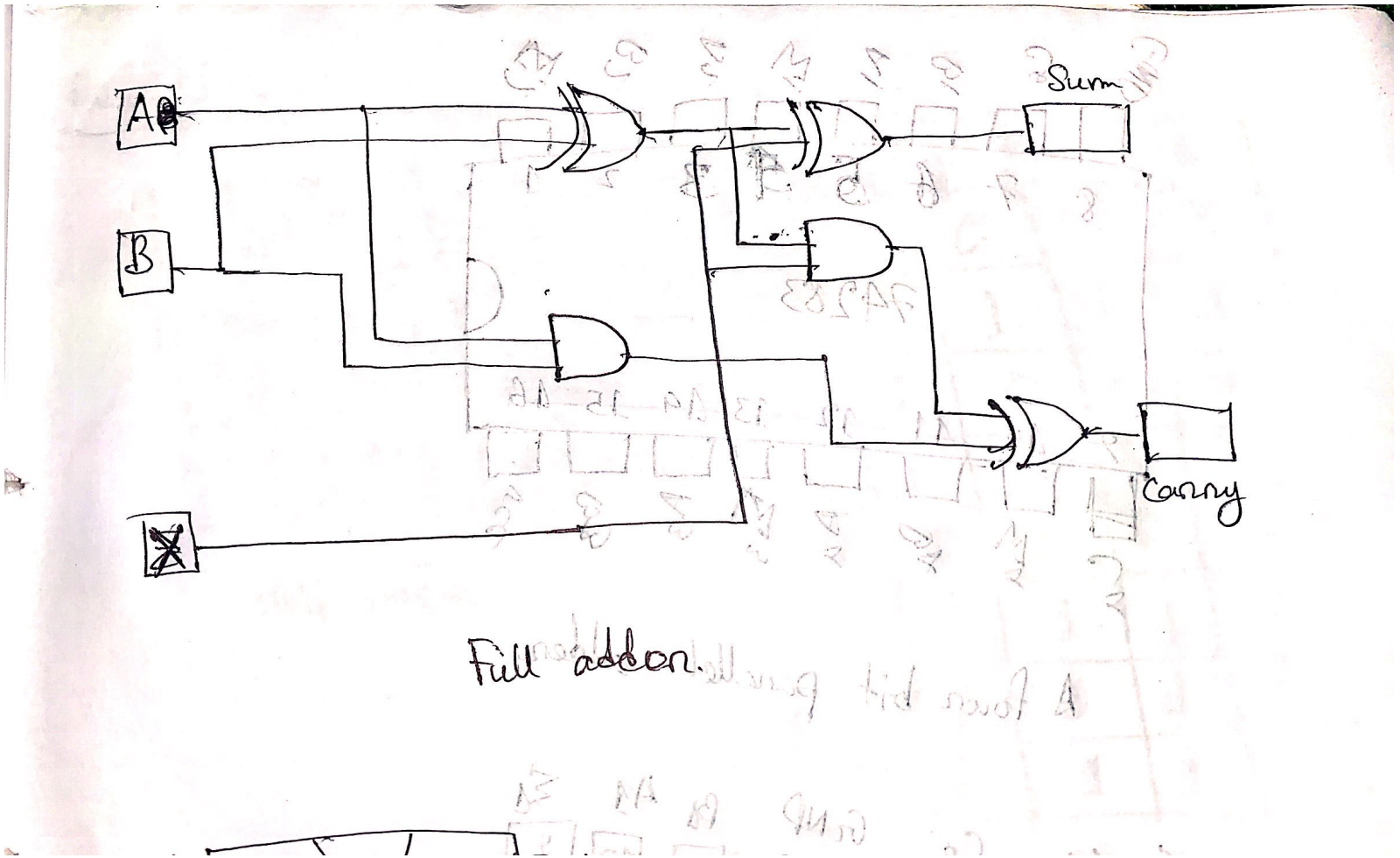
Required components:

1) AND gate
2) OR gate
3) XOR gate
4) LOGICSTATE
5) LOGICPROBE.
6) 74283 4 parallel checker bit

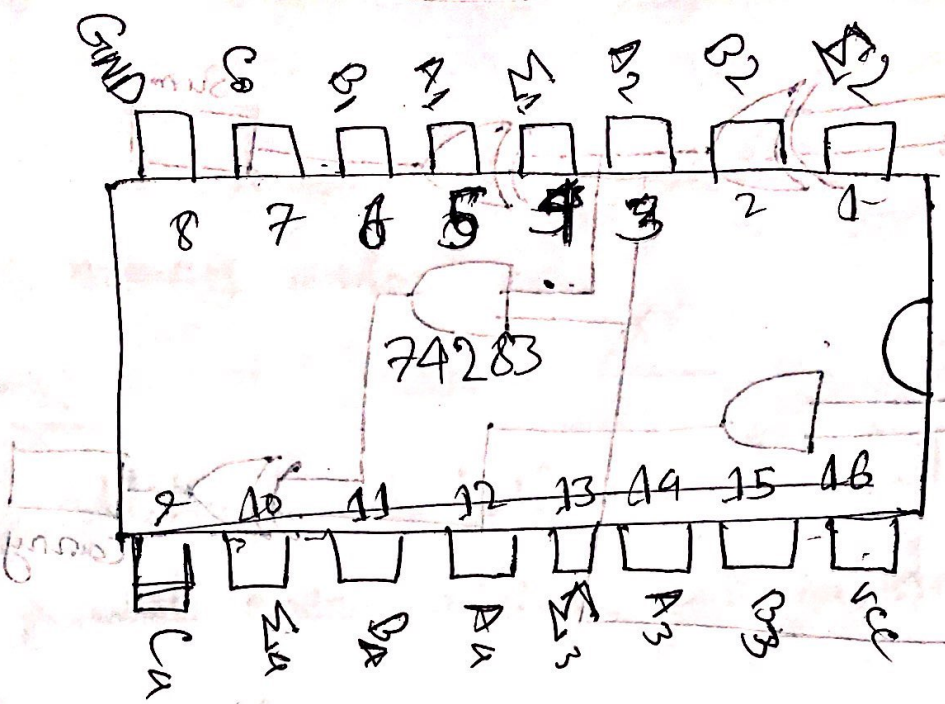
Experimental Setup:



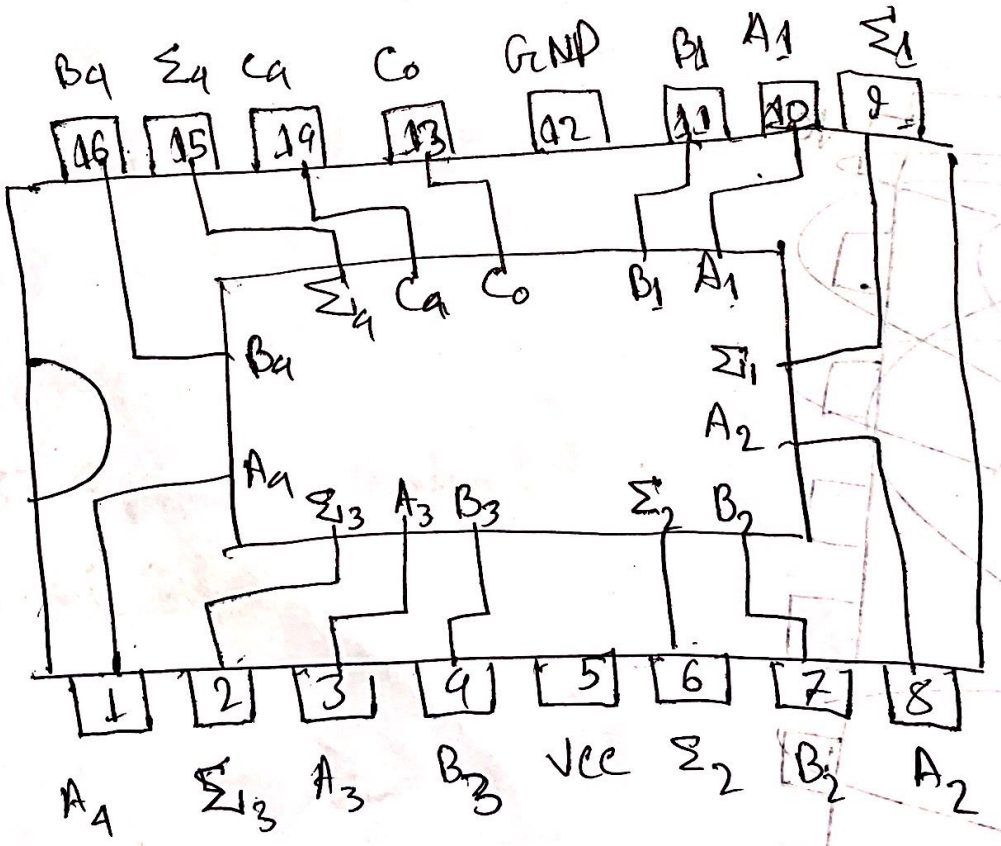
:- Half adder



Full adder.



A four bit parallel adder



A four bit full adder cum substractor

Result:

x	y	c	S
0	0	0	0
0	1	0	1
1	0	0	1
0	1	1	0

Half adder

x	y	X	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full adder

Discussion:

Half adder add two 1 bits and we get a sum and a carry out. In Full adder there is a carry in & and a ~~carry~~ carry out and we get the sum of three ~~bits~~ numbers.