Experiment-3

Parity Generator and Checker

Objective:

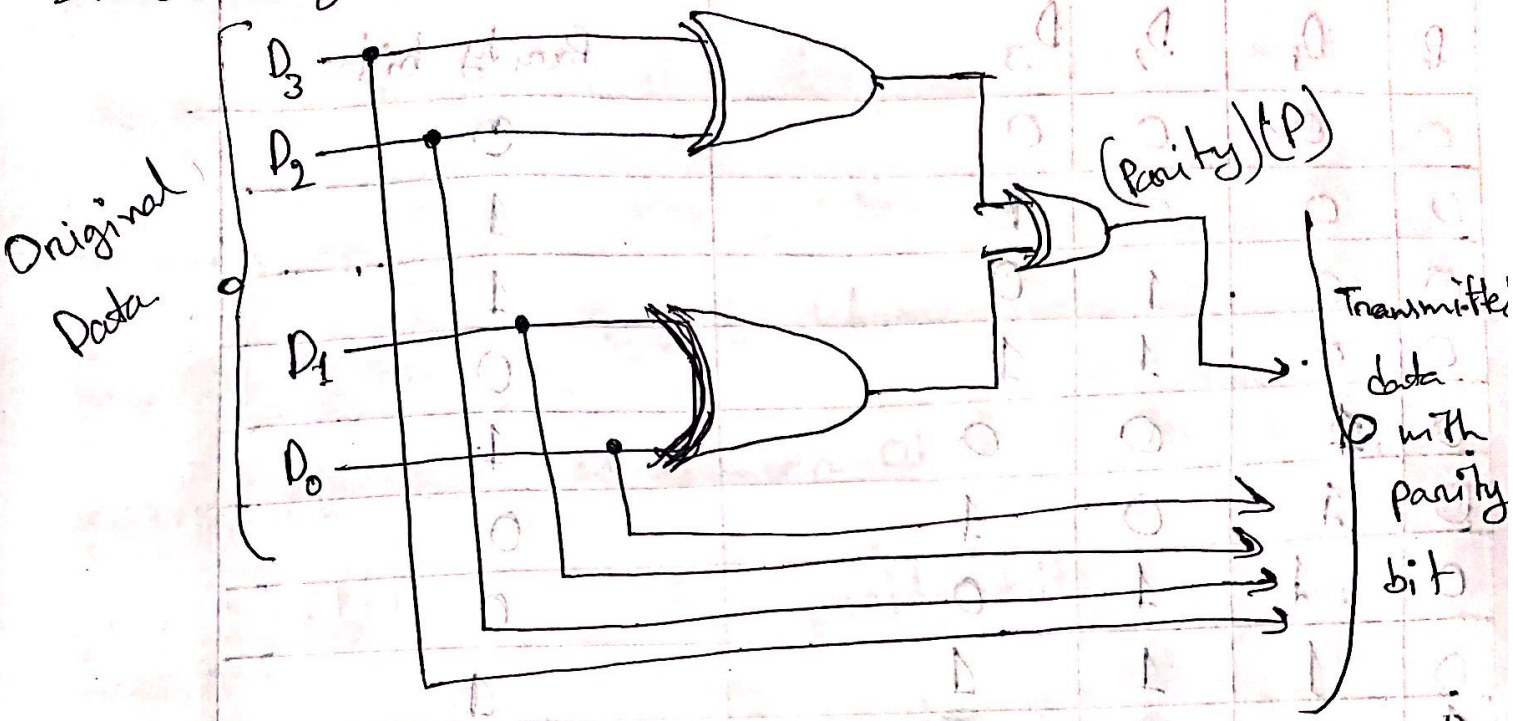
- To design and implement an even parity Generator and Even parity checker using XOR gates) (IC-7486)

Required Components and Equipments:

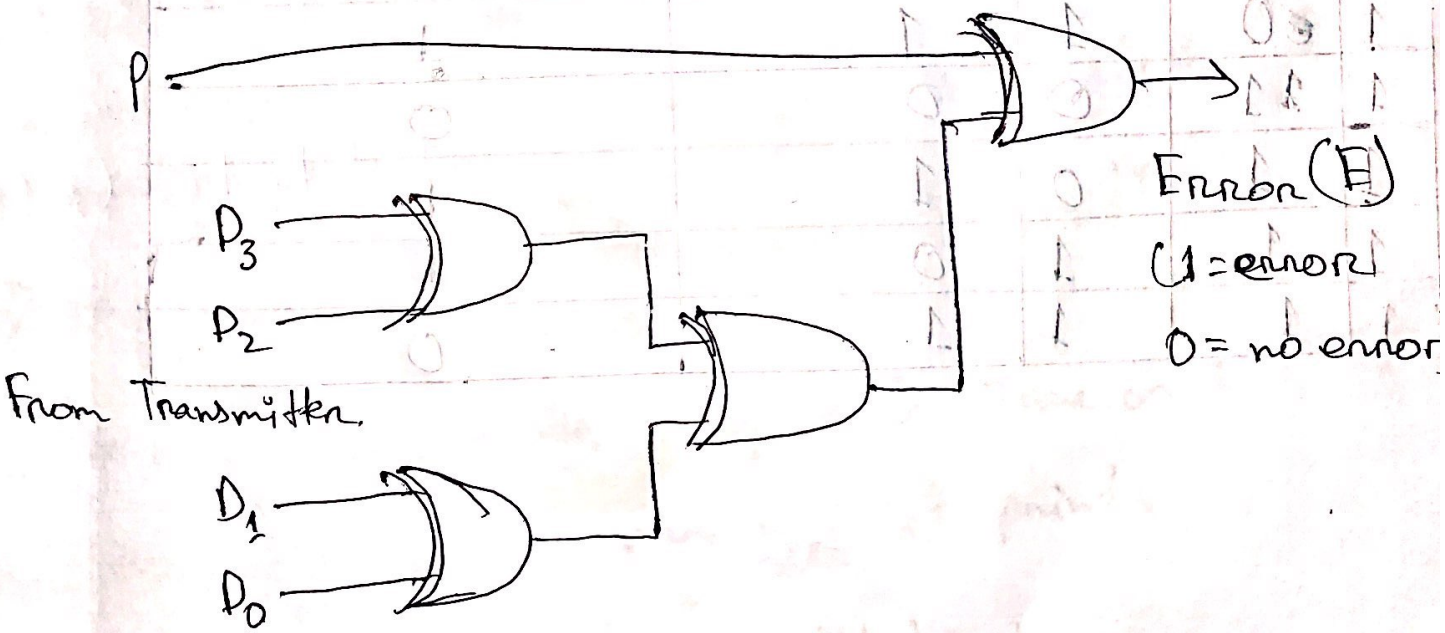
- XOR gate
- LOGIC STATE
- LOGIC PROBE

Diagram of Circuit:

Even Parity generator.



Even Parity Checker.



Results in Tabulated form:

D_0	D_1	D_2	D_3	Parity bit
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

~~Description~~

Discussion:

The parity rule is that the even parity ~~rule~~ is when we have even number of 1 in our function then we have to determine 0 as a parity bit. But odd number of 1 in ~~the~~ a function the 1 is the parity bit.

a) 0111; here, there are ~~even~~ odd number of '1' so parity bit is '1'

b) 1001; here, there are even number of '1' so parity bit is '0'

c) 0000; ~~there~~ this is even so parity bit is '0'

d) 0100; odd number of '1' so parity bit is '1'.

In the checker is the output is True or '1' then there will be no error; if it prints False or '0' there there will be no error.