Basic Opearation: The input bits of the DAC are enabled (made equal to a 1) one at a time, starting with the most significant bit (MSB). As each bit is enabled, the comparator produces an output that indicates whether the input signal voltage is greater or less than the output of the DAC. If the DAC output is greater than the input signal, the comparator's output is LOW, causing the bit in the register to reset. If the output is less than the input signal, the 1 bit is retained in the register. The system does this with the MSB first, then the next most significant bit. Then the next, and so on. After all the bits of the DAC have been tried, the conversion cycle is complete.

Figure 1 illustrates the step-by-step conversion of a constant input voltage (***5.1V in this case***). Let's assume that the DAC has the following output characteristic: V_{out} , = 8 V for the 2^3 bit (MSB), V_{out} = 4 V for the 2^2 bit, V_{out} = 2 V for the 2^1 bit. and V_{out} = 1V for the 2^0 bit (LSB).

First step: Figure 1(a) shows the conversion cycle with the MSB = 1. The output of the DAC is 8 V. Since this is greater than the input of 5.1 V, the output of the comparator is LOW, causing the MSB in the SAR to be reset to a O in next step.

Second step: Figure 1(b) shows the conversion cycle with the 2^2 bit equal to a 1. The output of the DAC is 4 V. Since this is less than the input of 5.1 V, the output of the comparator switches to a HIGH, causing this bit to be retained/kept in the SAR.

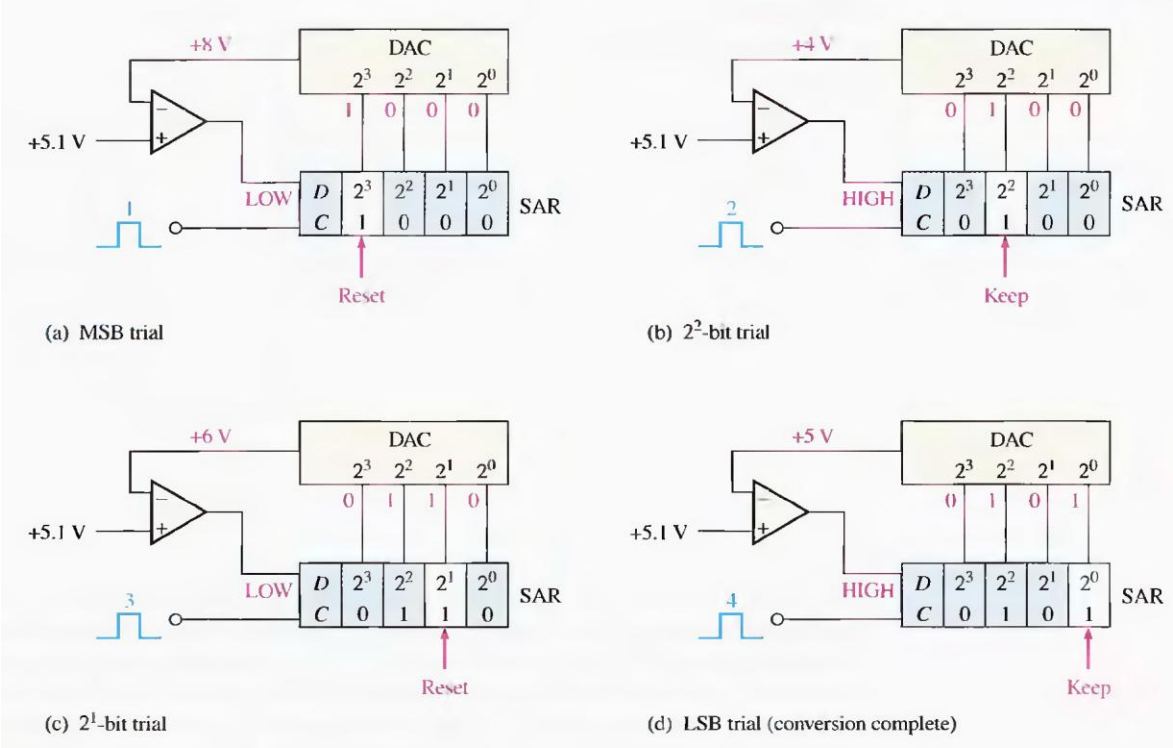

Figure 1. Successive approximation conversion process.

Third step: Figure 1(c) shows the in the conversion cycle with the 2^1 bit equal to a 1. The output of the DAC is 6 V because there is a 1 on the 2^1 bit input and on the 2^1 bit input (4 V + 2 V = 6 V). Since this is greater than the input of 5.1 V, the output of the comparator switches to a LOW, causing this bit to be reset to a 0.

Fourth step: Figure 1(d) shows the conversion cycle with the 2^0 bit equal to a 1. The output of the DAC is 5 V because there is a 1 on the 2^2 bit input and on the 2^0 bit input (4 V + 1 V = 5 V).

The four bits have all been tried, thus completing the conversion cycle. At this point the binary code in the register is 0101, which is approximately the binary value of the input of 5.1 V.