MODULE – 1

FETs & OP-AMPs

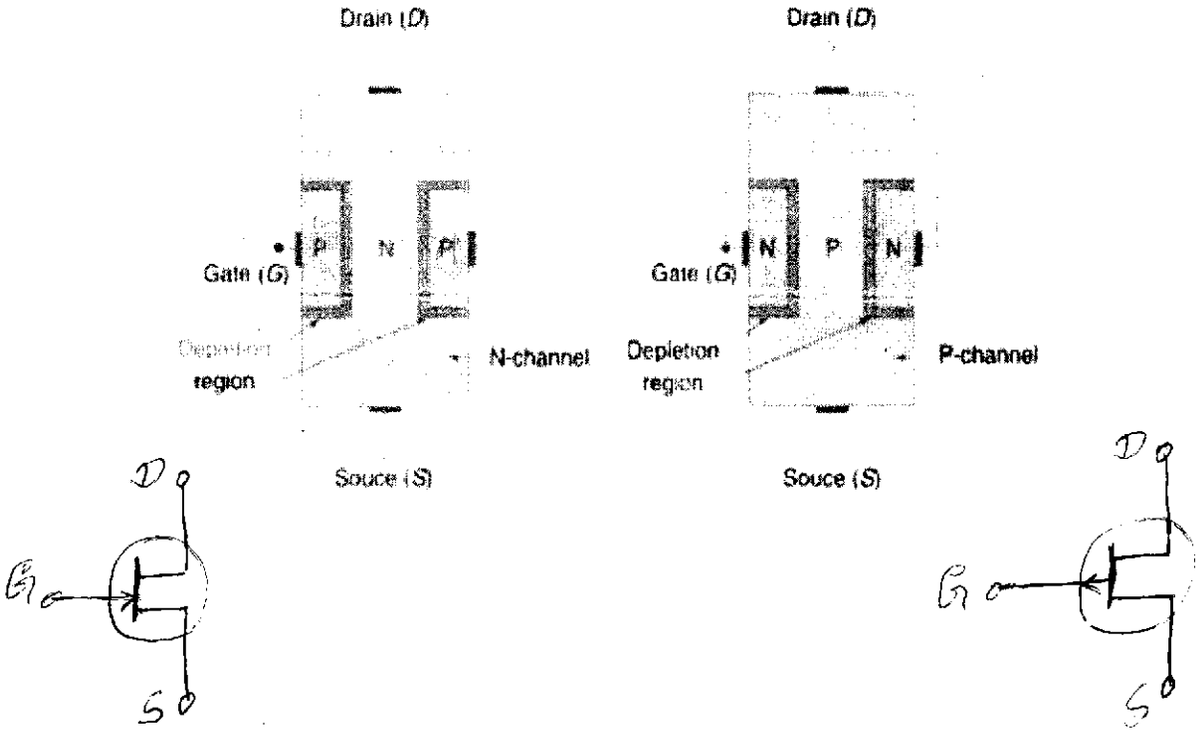
FIELD EFFECT TRANSISTORS

JUNCTION FIELD EFFECT TRANSISTORS (JFETs):

JFET is the simplest of the FETs. ***JFET*** *is a three-terminal device where the voltage applied at one terminal controls the current through the other two terminals.*

JFETs comprise a semiconductor channel embedded into semiconductor layers of opposite polarity. Depending upon the semiconductor channel, JFETs are classified as N-channel or P-channel JFETs.

Construction & Principle of Operation:



The Cross-sectional View of N-channel & P-channel JFETs

In N-channel JFET, an N-type semiconductor material forms a channel between embedded layers of P-type material. In P-channel JFET, a P-type semiconductor forms a channel between the embedded layers of N-type material.

Hence, two PN junctions are formed between the semiconductor channel and the embedded semiconductor layers.

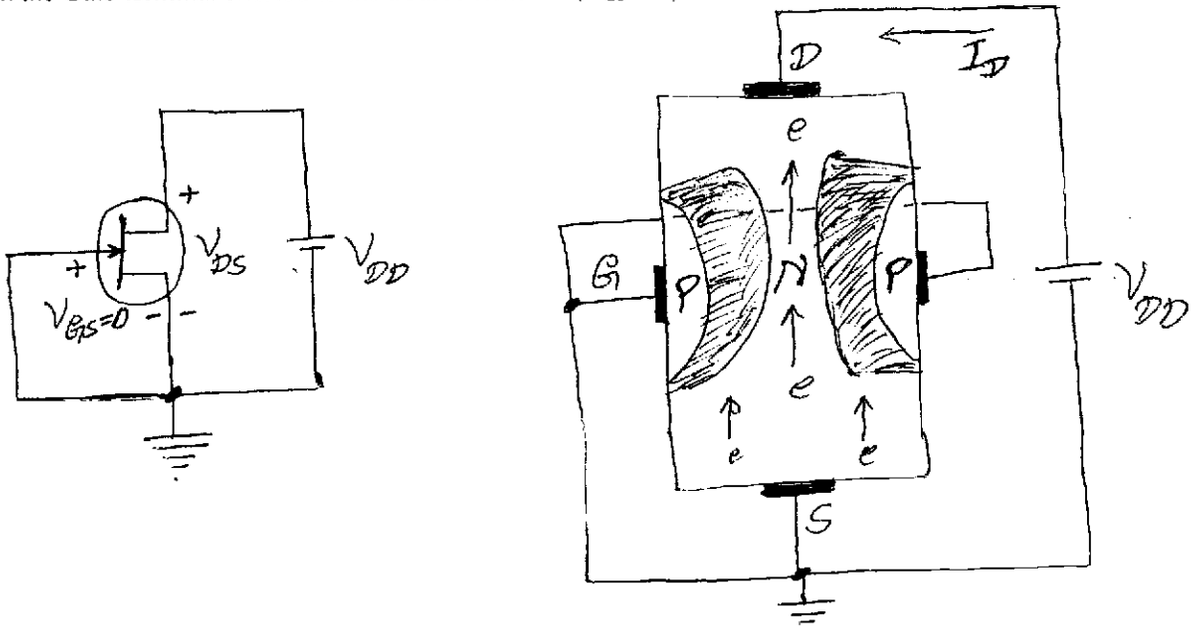
Contacts are made at the top and bottom of the channel and are referred to as the Drain (D) and the Source (S). The channel behaves as a resistive element between its drain and source terminals.

In an N-channel JFET, both the embedded P-type layers are connected together and form the Gate (G) terminal. Similarly, in a P-channel JFET, Gate (G) terminal if formed by connecting the two N-type embedded layers.

In the absence of any externally applied potential, both the PN junctions are open circuit and a small depletion region is formed at each of the junction (as shown in above Fig). The externally applied potential between the Gate and the Source terminals controls the flow of Drain current for a given potential between the Drain and the Source terminals.

Characteristic Curves:

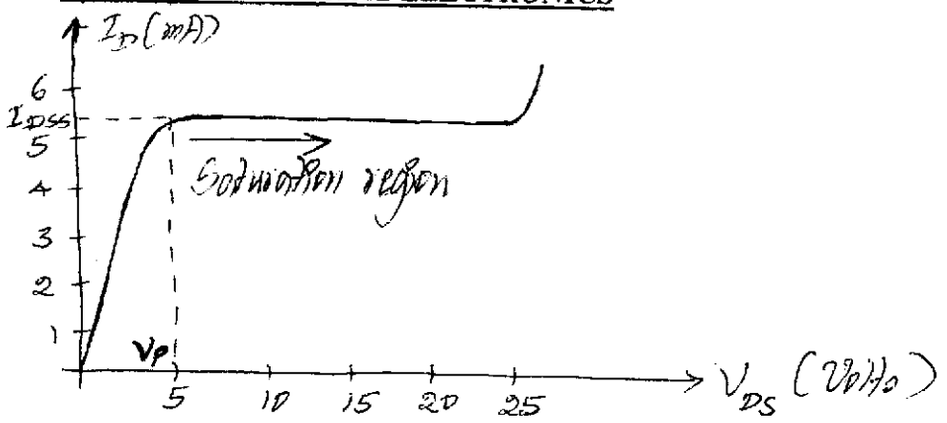
Consider an N-channel JFET with a situation when a positive Drain-Source voltage (V_{DS}) is applied to the JFET with the Gate terminal shorted to the Source terminal ($V_{GS} = 0$).



N-channel JFET with V_{GS} = 0 and Positive Value of V_{DS}

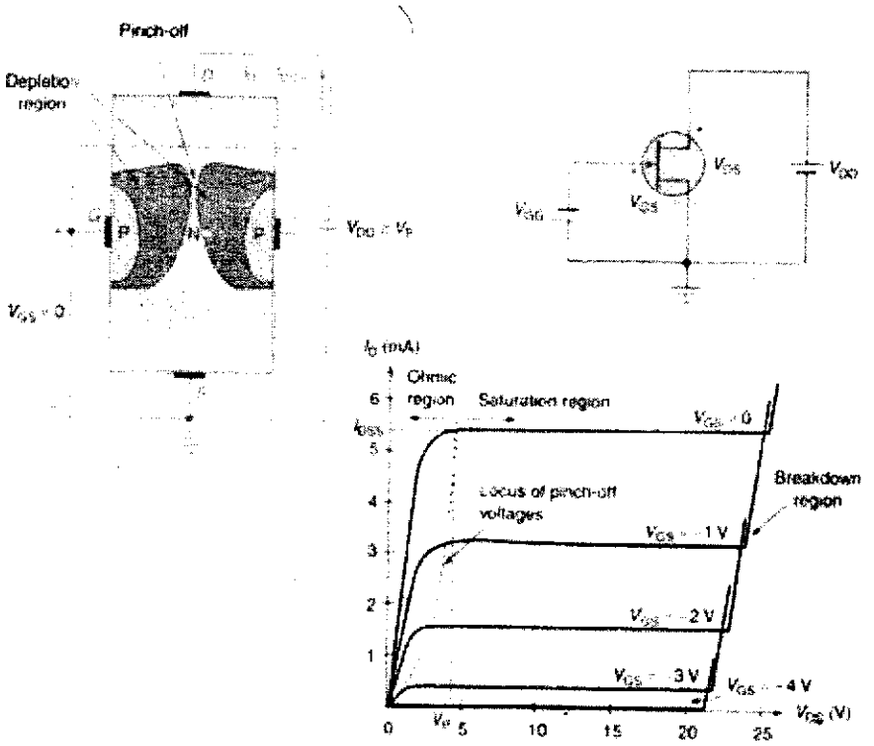
When the Drain-Source voltage is applied, the electrons in the N-channel are attracted to the Drain terminal, establishing the flow of Drain current (I_D) as shown in the above Fig. The value of I_D is determined by the value of applied V_{DS} and the resistance of the N-channel between the Drain and the Source terminals.

Due to the flow of I_D, there is a uniform voltage drop across the channel resistance, which reverse biases the two PN junctions. This results in increase in the width of the depletion region. The depletion region is wider near the Drain-region than the Source-region. This is because I_D and the channel resistance establish more reverse-bias voltage at the PN junction near the Drain-region than the Source-region.



The Relationship between I_D and V_{DS} for V_{GS} = 0

I_D increases linearly with increase in V_{DS}, till the V_{DS} reach a value where the saturation effect sets in. *The value of V_{DS} where saturation effect sets in is referred to as* ***pinch-off voltage (V_P)***. When V_{DS} reaches V_P, the value I_D does not change with further increase in V_{DS}. This condition is referred to as *pinch-off condition*. This happens because the width of the depletion regions of the PN junctions has increased significantly near the drain region, resulting in reduction of channel width. Hence, I_D remain constant for $V_{DS} > V_P$.



N-channel JFET Biasing Circuit & Output Characteristic Curves

The Gate-Source voltage (V_{GS}) is the control voltage for JFETs. When a negative bias is applied to the Gate terminal, there is an increase in width of the depletion region. Hence, pinch-off phenomenon occurs at lower values of V_{DS}. Also, the value of Saturation Drain current decreases. As the value of V_{GS}

becomes more negative the value of saturation current decreases further. The Drain current becomes zero for $V_{GS} = -V_P$. This voltage is referred to as *Gate-Source cut-off voltage* or the *Gate-Source pinch-off voltage* ($V_{GS(off)}$).

In the output characteristic curve (Fig shown above), the region to the left of the locus of pinch-off voltages is the *Ohmic region* or the *Voltage-Controlled Resistance region*. The region to the right of the locus of pinch-off voltages is the *Saturation region* or the *Constant Current region*. In Ohmic region, JFET acts as a variable resistor whose resistance is controlled by the applied Gate-Source voltage.

The Drain resistance in the saturation region is given by;

$$r_d = \frac{r_0}{(1 - V_{GS}/V_P)^2}$$

where, r_0 – is the resistance at $V_{GS} = 0$

r_d – is the resistance at a particular value of V_{GS}.

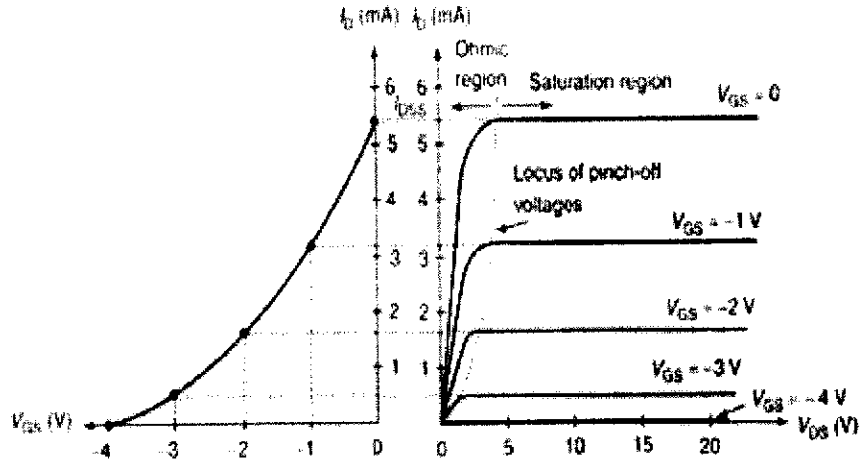
The relationship between the output current I_D in the saturation region for the given value of input V_{GS} is given by (*Shockley's equation*);

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where, I_{DSS} – is the Drain current for short circuit connection between Gate and the Source.

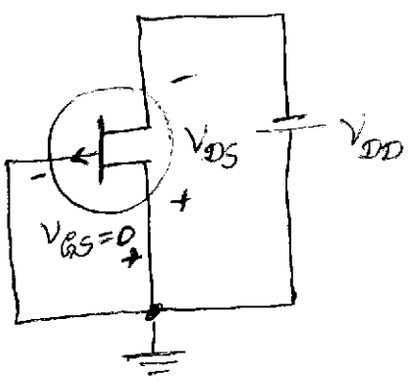
From this Shockley's equation, it is clear that, there is a non-linear square law relationship between the output Drain current (I_D) and the input Gate-Source voltage (V_{GS}). Because of this square law characteristic, JFETs are very useful devices in radio tuners and TV receivers.

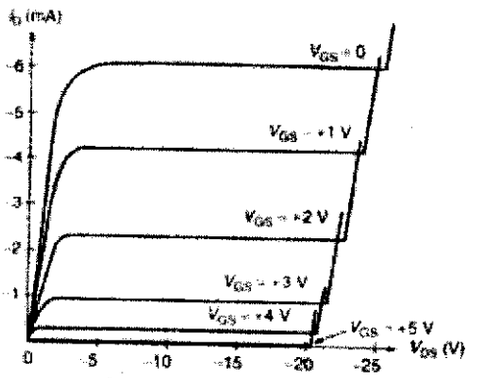
The transfer characteristic of a JFET device is a plot between I_D and V_{GS}. This can be plotted using Shockley's equation or using the output characteristics curves. The following Fig shows how to obtain the transfer characteristics curves using the output characteristic curves.



Transfer Characteristic Curves of N-channel JFET

The P-channel JFETs behave in the same manner as the N-channel JFETs with the direction of currents and polarities of voltages reversed.





P-channel JFET Biasing Circuit & Output Characteristic Curves

Effect of Temperature on JFET Parameters:

JFETs offer better thermal stability as compared to BJTs. Increase in JFET temperature results in *decrease in the depletion region width* and the *decrease in the carrier mobility.*

- *Decrease in the width of depletion region* results in increase in channel width; which in turn increases in I_D. This results in positive temperature coefficient for I_D. Increase in I_D with temperature results in increase in $V_{GS(OFF)}$. $V_{GS(OFF)}$ has a positive temperature coefficient of the order of 2.2 mV/^{0}C.
- *Decrease in carrier mobility* gives ⊠ a negative temperature coefficient.

Since both mechanisms occur simultaneously, the effect of one mechanism compensates for the other. Hence, JFETs offer better temperature stability.

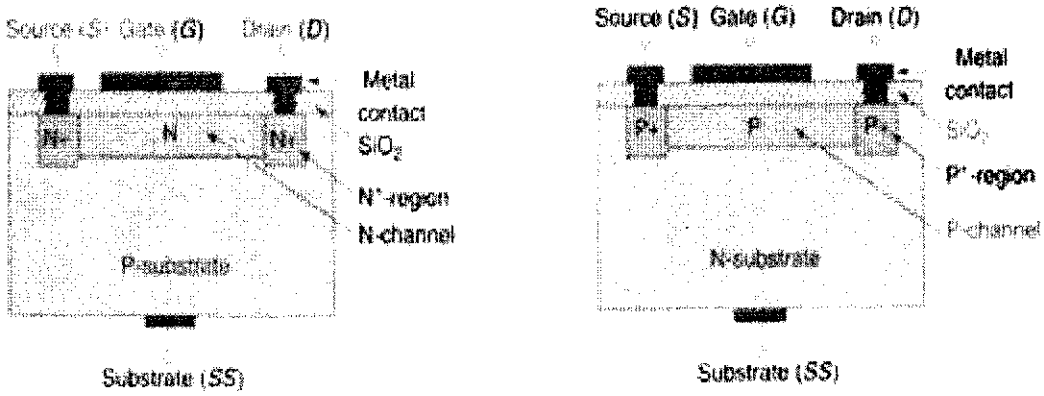
METALOXIDE FIELD EFFECT TRANSISTORS (MOSFETs):

A MOSFET is also a three-terminal device where the Drain current is controlled by the applied Gate voltage (like a JFET). MOSFETs are also referred to as Insulated Gate FETs (IGFETs). MOSFET is insulated from the semiconductor channel by a very thin oxide layer.

MOSFETs are classified into two types depending upon their construction and mode of operation – the *depletion MOSFET (DE-MOSFET)* the *enhancement MOSFET (E-MOSFET).*

Depletion MOSFETs:

In a DE-MOSFET, a channel is physically constructed between the Drain and the Source terminals. Depending on the channel material, DE-MOSFETs are classified as *N-Channel DE-MOSFETs* and *P-channel DE-MOSFETs.*

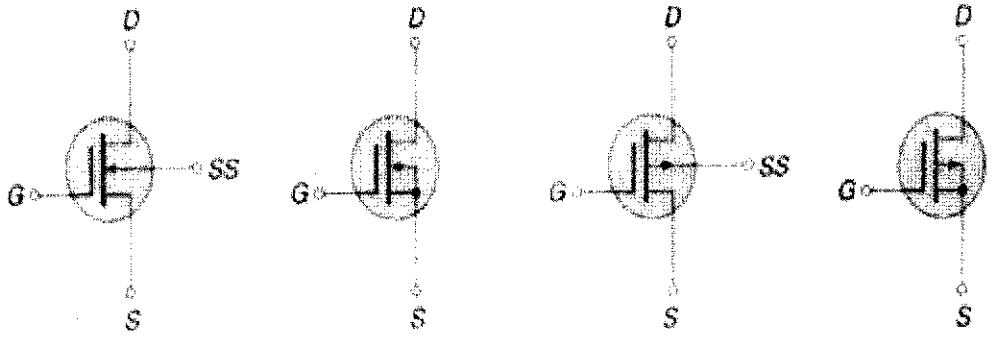


Cross-section of an N-channel & P-channel DE-MOSFET

The cross-sectional view of an N-channel DE-MOSFET comprises a substrate made of a P-type semiconductor material. Two N+ type regions linked by an N-channel are formed on the substrate. The Source and the Drain terminals are formed by connecting metal contacts to the two N+ regions (as shown in the above Fig). The Gate terminal is connected to the insulating silicon dioxide (SiO_2) layer on the top of the N-channel. Hence, there is no direct electrical connection between the Gate terminal and the channel of DE-MOSFET.

There is a capacitance that exists between the Gate terminal and the channel as the metal Gate contact and the channel act as walls of a parallel plate capacitor and the SiO_2 layer form the dielectric. Hence, the input impedance of a DE-MOSFET is very high (in the order of $10^{10} - 10^{15}\ \Omega$).

The construction of P-channel DE-MOSFET is similar to that of an N-channel DE-MOSFET, with the difference being that the substrate is an N-type semiconductor and the channel is P-type material.



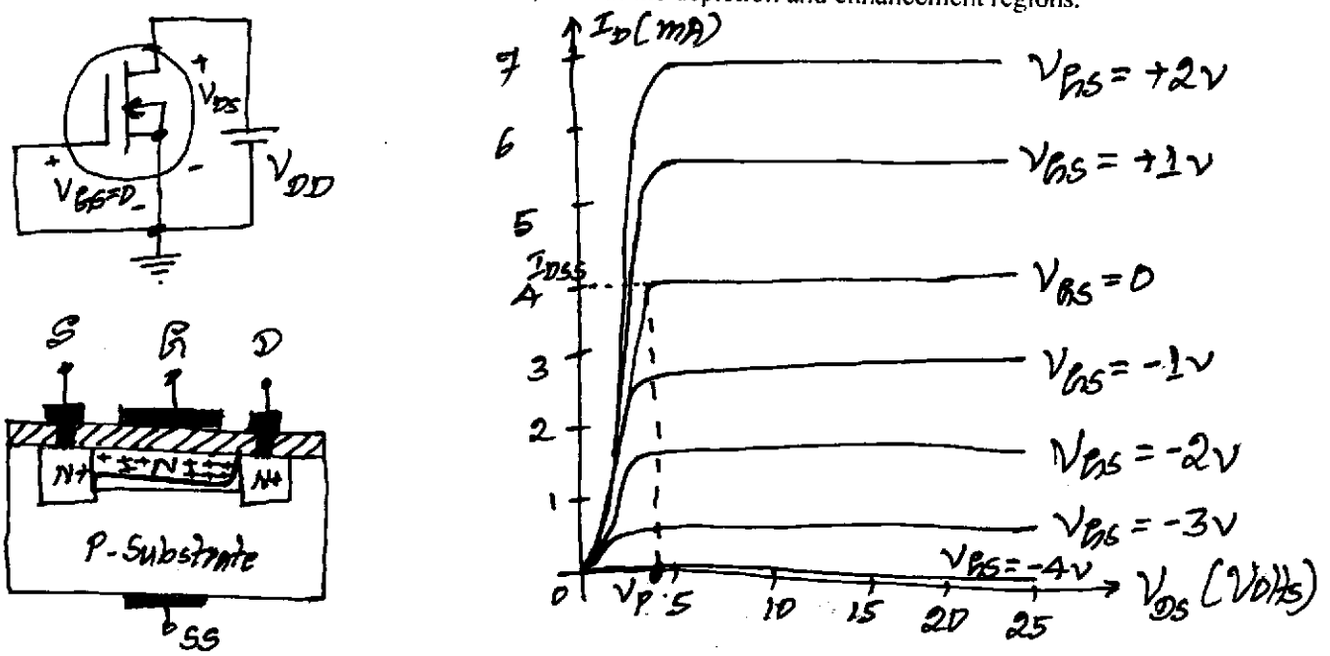
Circuit Symbol of an N-channel DE-MOSFET & P-channel DE-MOSFET

Operation of N-channel DE-MOSFET: When the Gate and the Source terminals are shorted, ($V_{GS} = 0$) and a positive voltage is applied between the Drain the Source terminals; there is a flow of current in the N-channel, as the electrons are attracted by positive potential at the Drain terminal. The current increases with increase in V_{DS}; and after certain value of V_{DS}, it becomes constant.

When the Gate terminal is at a negative potential as compared to the Source terminal, electrons in the N-channel are repelled by this negative potential towards the P-type substrate. Also, holes in the P-type substrate are attracted towards the Gate. This results in recombination of holes and electronics and there will be reduction of number of free electrons in the N-channel. Higher the negative potential more is the rate of recombination and less the number of free electrons in the N-channel. Hence, the drain current decreases with increase in the value of the negative Gate-Source potential.

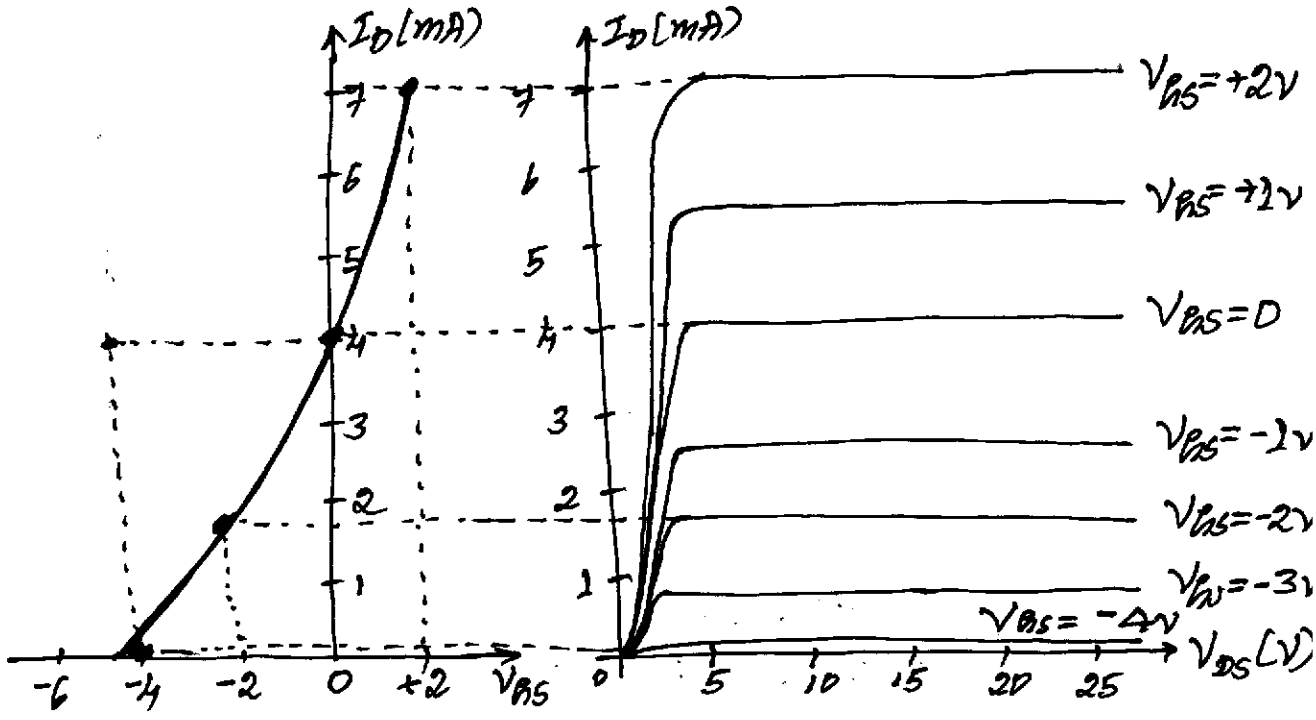
For positive values of Gate-Source voltage, electrons in the P-type substrate are attracted into the channel and establish new carriers through the collisions between accelerating particles. Thus the Drain current increases rapidly with increase in the positive value of Gate-Source voltage.

As the application of positive Gate-Source voltage increases the value of Drain current, the region of positive Gate-Source voltage is referred to as the *enhancement region*. The region for zero and negative values of Gate-Source voltage is referred to as *depletion region*. The Shockley's equation defined for JFETs is applicable for DE-MOSFETs, in both the depletion and enhancement regions.



Output Characteristic Curves of N-channel DE-MOSFET

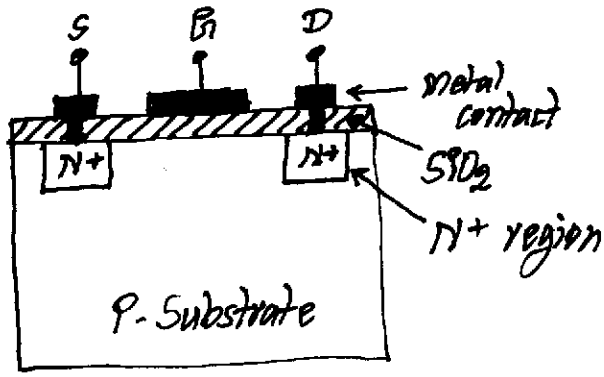
The transfer characteristics for DE-MOSFET can be plotted in a similar fashion for that of a JFET (see the following Fig).

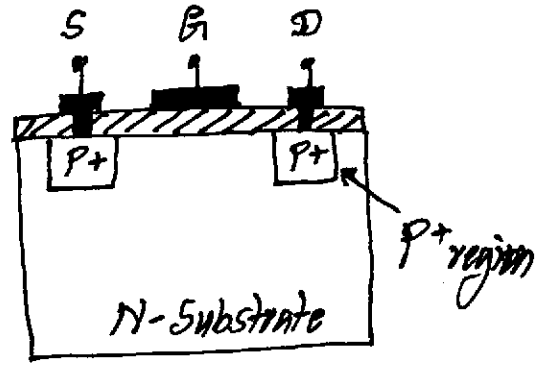


Transfer Characteristic Curves of N-channel DE-MOSFET

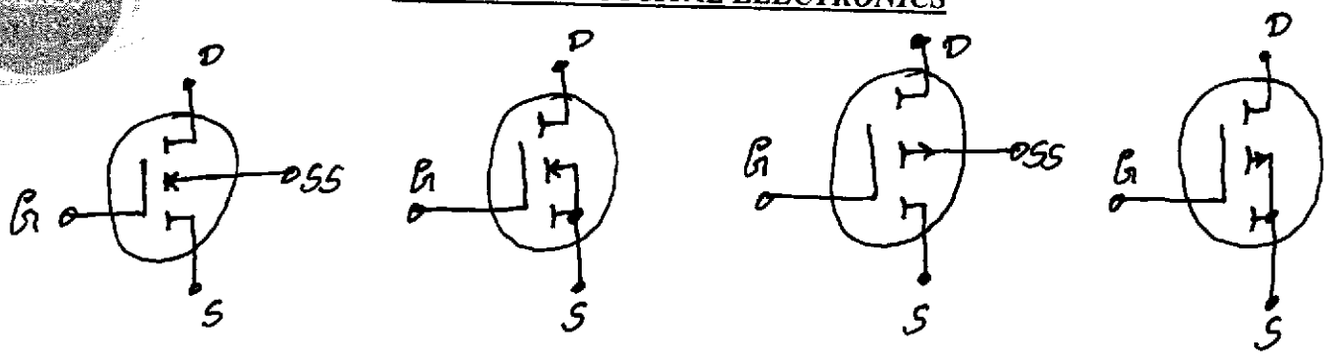
Enhancement MOSFETs:

The construction of an E-MOSFET is similar to that of a DE-MOSFET with the difference that there is no physical channel between the Source and Drain terminals in the E-MOSFET.





Cross-section of an N-channel & P-channel E-MOSFET

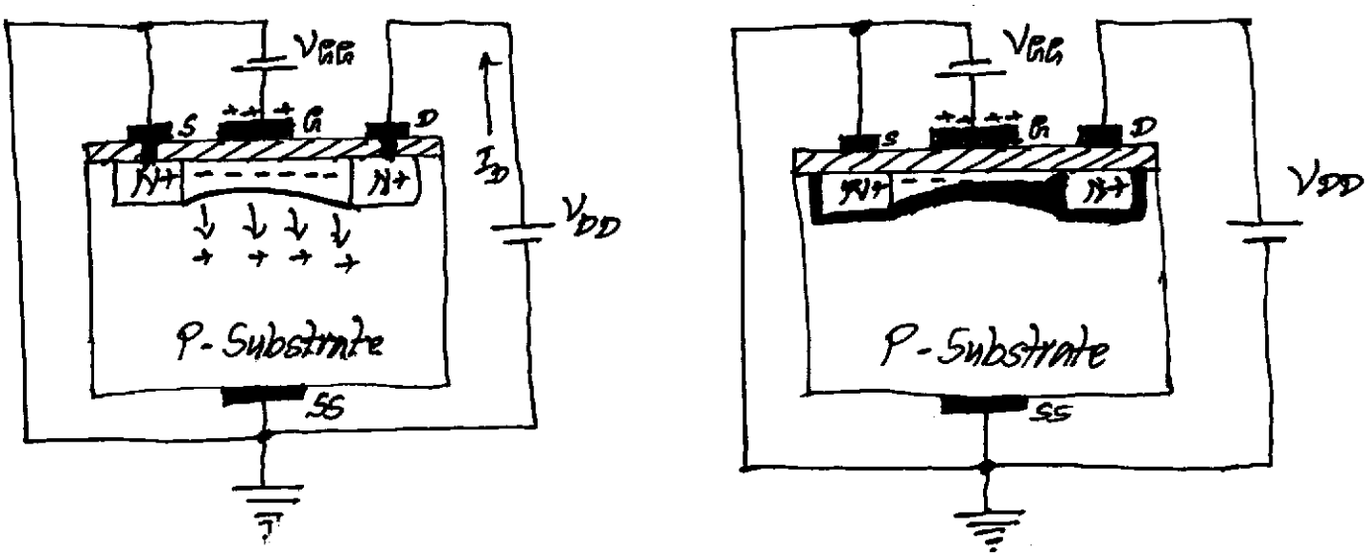


Circuit Symbol of an N-channel DE-MOSFET & P-channel DE-MOSFET

Operation of N-channel DE-MOSFET: When the Gate-Source voltage is zero (V_{GS} = 0) and some positive Drain-Source voltage (V_{DS}) is applied, there is no Drain current; as there is no channel available for flow of Drain current. Hence, E-MOSFETs are also referred to as OFF-MOSFETs, as they do not conduct when V_{GS} = 0.

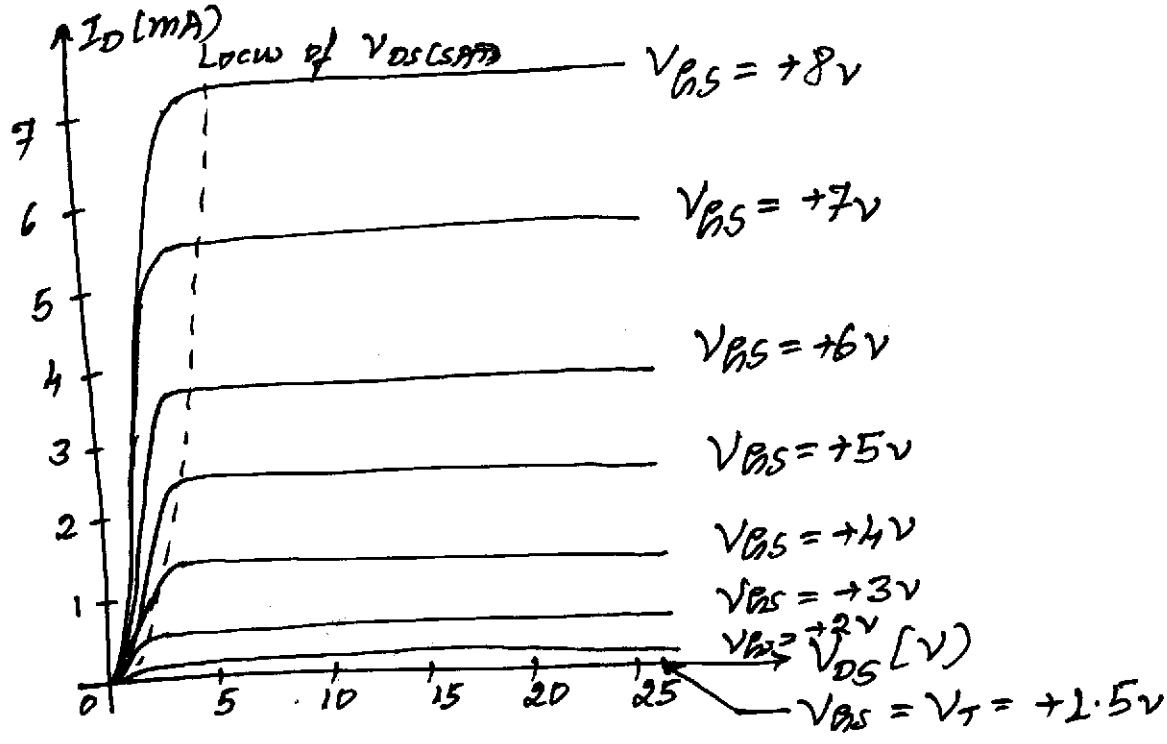
When a positive Gate-Source voltage (V_{GS}) is applied, electrons (minority carriers) in the P-type substrate will accumulate near the surface of the SiO_2 layer. Also, holes in the P-substrate are forced to move away from the edge of SiO_2 layer. This forms a channel (as shown in following Fig). As SiO_2 layer is insulating, it prevents the electrons from being absorbed at the Gate terminal. Hence, the Drain current flows.

As the value of Gate-Source voltage is increased, more and more electrons accumulate leading to an enhanced flow of Drain current. The level of Gate-Source voltage that leads to significant flow of Drain current is referred to as *threshold voltage (V_T)*.



Working of N-channel E-MOSFET & Pinching Phenomenon in E-MOSFET

For a fixed Gate-Source voltage and increasing the level of Drain-Source voltage (V_{DS}), leads to an initial increase in the Drain current, which eventually saturates due to the reduction of Gate-Drain voltage (V_{GD}). Reduction in the Gate-Drain voltage reduces the attractive forces for the free carrier in the induced channel near the Drain region. This results in the reduction of effective channel width near the Drain region. This effect is referred to as *pinching effect*. Pinching effect refers to the reduction in the width of the induced channel near the Drain region with increase in the Drain-Source voltage (as shown in the above Fig). The value of Drain-Source voltage at which the Drain current saturates is given by $V_{DS(SAT)}$.



Output Characteristic Curves for an N-channel E-MOSFET

The relationship between $V_{DS(SAT)}$ and V_{GS} is given by; $V_{DS(SAT)} = V_{GS} - V_T$

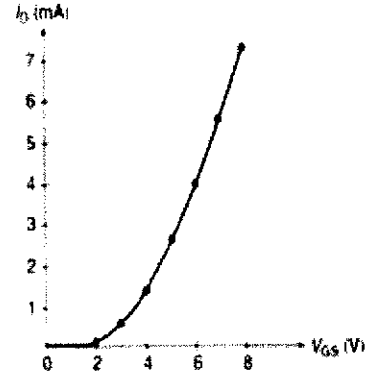
where, V_T is the threshold Gate-Source voltage.

Also, the Drain current is zero for Gate-Source voltage less than the threshold voltage V_T.

For voltages greater than the threshold voltage, the Drain current is given by; $I_D = K (V_{GS} - V_T)^2$

where, K is a constant.

The relationship between the Drain current and the Gate-Source voltage is non-linear and the current is proportional to the square of the voltage (shown in the Fig).



Transfer Characteristics of an N-channel E-MOSFET

ANALOG AND DIGITAL ELECTRONICS

Problem: *Draw the output characteristics of an N-channel E-MOSFET, when the Gate-Source voltage (V_{GS}) is twice the threshold voltage (V_T). An external supply V_{GG} is applied between the Gate and the Drain terminals. Draw the curve between the Drain current and voltage V_D for $V_{GG} = V_T/2$.*

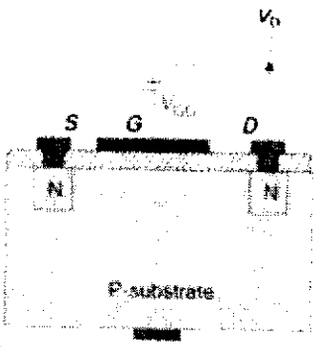
Solution:

- E-MOSFETs conducts for $V_{GS} > V_T$.

  We have; $I_D = K(V_{GS} - V_T)^2$

  Let I_{DS} is the current for $V_{GS} = 2V_T$.

  $\Rightarrow I_{DS} = K(2V_T - V_T)^2 \Rightarrow K = I_{DS}/V_T^2$.



- The output characteristics can be plotted by using the equations;

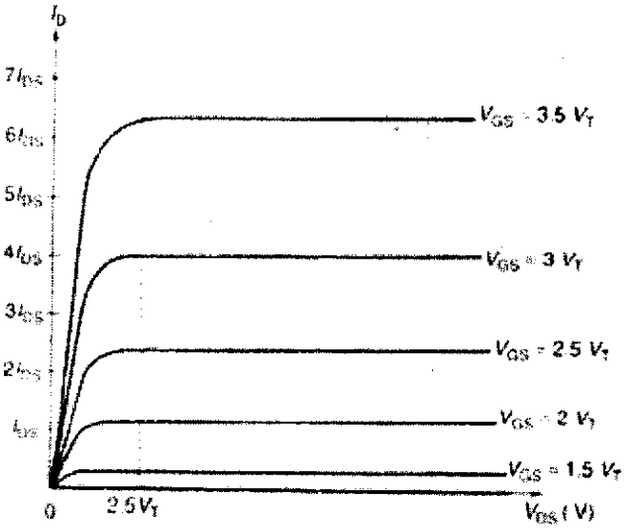
  $$I_D = \frac{I_{DS}}{V_T^2}(V_{GS} - V_T)^2 \qquad V_{DS(sat)} = V_{GS} - V_T.$$

- Since voltage V_{GG} is applied betn G & D-terminals;

  $$V_{GS} = V_{GG} + V_{DS} = V_{GG} + V_D \quad [\because V_D = V_{DS}]$$

- Given, $V_{GG} = V_T/2 \Rightarrow V_D/V_{DS} = V_{GS} - V_T/2$

V_{GS}	I_D	V_{DS}/V_D
$0.5V_T$	0	0
V_T	0	$0.5V_T$
$1.5V_T$	$0.25I_{DS}$	V_T
$2V_T$	I_{DS}	$1.5V_T$
$2.5V_T$	$2.25I_{DS}$	$2V_T$
$3V_T$	$4I_{DS}$	$2.5V_T$
$3.5V_T$	$6.25I_{DS}$	$3V_T$



DIFFRENCES BETWEEN JFETs AND MOSFETs:

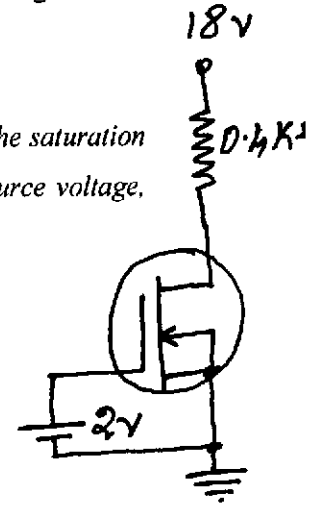
JFETs	MOSFETs
1. JFETs are operated in depletion mode only.	1. DE-MOSFETs can be operated in both depletion and enhancement modes and E-MOSFETs are operated in enhancement mode only.
2. Input resistance for JFETs is greater than 10^9 Ω.	2. Input resistance for MOSFETs is much higher than JFETS (around 10^{13} Ω).
3. JFETs have higher Drain resistance (in the range of 100 KΩ to 1 MΩ) than MOSFETs; and hence their characteristic curve is more flat than that of MOSFETs	3. The Drain resistance of MOSFETs is in the range of 1 to 50 KΩ.
4. The Gate current for JFETs is in the range of 100μA to 10 nA.	4. The leakage current in MOSFET is much smaller than that in JFETs. The Gate current for MOSFETs is in the range of 100 nA to 10 pA.
5. MOSFETs are easier to construct and are used more widely than JFETs.	

BIASING MOSFETs:

Biasing is done to produce the required Gate-to-Source voltage (V_{GS}) to get the desired value of Drain current (I_D). The biasing circuits should maintain the Drain current and Drain-Source voltage within reasonable limits.

Depletion MOSFETS:

Problem: The following Fig shows a biasing configuration using DE-MOSFET. Given that the saturation Drain current is 8 mA and the pinch-off voltage is – 2 V; determine the value of Gate-Source voltage, Drain current and the Drain-Source voltage.



Solution:

- In a DE-MOSFET, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$

$\Rightarrow I_D = 8\times10^{-3}\left[1 - \frac{2}{(-2)}\right]^2 = 32\times10^{-3} = 32\text{ mA}$.

- Applying Kirchhoff's voltage law to the output section, we get; $-V_{DD} + 0.4\times10^3 \times I_D + V_{DS} = 0$

or $-18 + 0.4\times10^3 \times 32\times10^{-3} + V_{DS} = 0$

$\Rightarrow V_{DS} = 18 - 12.8 = 5.2\text{ V}$.

- $V_{GS} = 2\text{ V}$
- MOSFET operating in enhancement region.
- $I_{DSS} = 8\text{ mA}$
- $V_p = -2\text{ V}$
- $V_{DD} = 18\text{ V}$

Hence; Gate-Source voltage, $V_{GS} = 2V$

Drain current, $I_D = 32mA$

Drain-Source voltage, $V_{DS} = 5.2V$.

Problem: *Design a voltage-divider-bias network using DE-MOSFET with the supply voltage V_{DD} = 16 V, I_{DSS} = 10 mA and V_P = – 5 V to have a quiescent Drain current of 5 mA and Gate voltage of 4 V (Assume the Drain resistor R_D to be four times the source resistor R_S).*

Solution: Given; $V_{DD} = 16V$, $I_{DSS} = 10mA$, $V_P = -5V$, $I_D = 5mA$, & $V_G = 4V$.

- Since, $I_D < I_{DSS}$; the MOSFET is operated in depletion mode
- We have; $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

i.e., $5\times10^{-3} = 10\times10^{-3}\left[1 - \frac{V_{GS}}{(-5)}\right]^2$ or $0.5 = \left(1 + \frac{V_{GS}}{5}\right)^2$

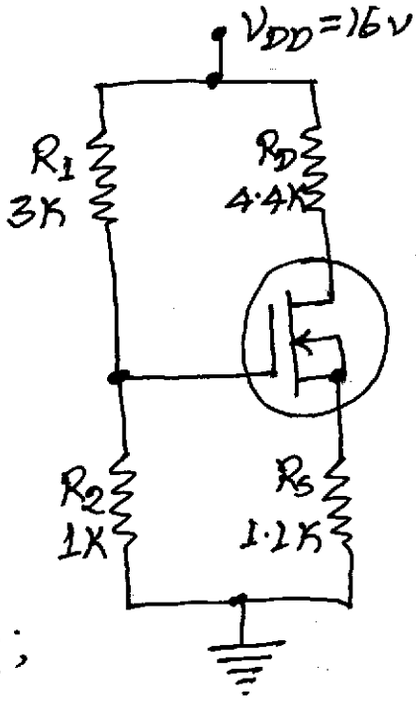
$\Rightarrow V_{GS}/5 = 0.7 - 1 = -1.5V$

- Also; $V_{GS} = V_G - V_S = V_G - I_D R_S$

i.e., $-1.5 = 4 - V_S$

or $V_S = I_D R_S = 4 + 1.5 = 5.5V$

$\therefore R_S = \frac{5.5}{5\times10^{-3}} = 1.1K\Omega$.

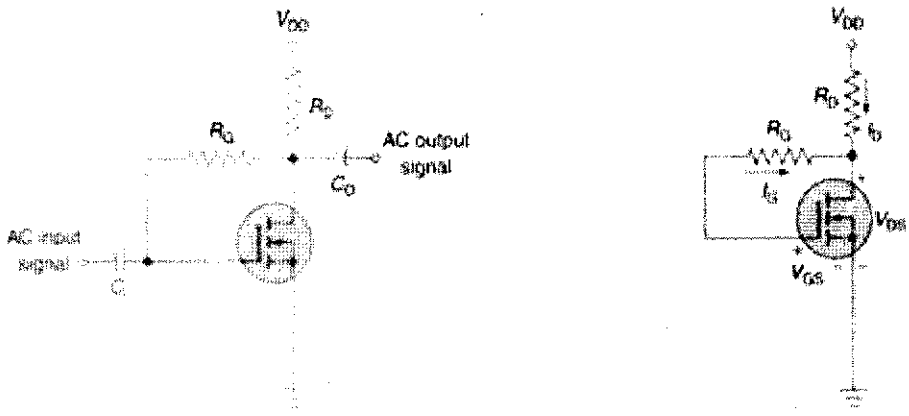


- We have; $R_D = 4R_S \Rightarrow R_D = 4.4K\Omega$.
- $V_G = \left[\frac{R_2}{R_1 + R_2}\right] V_{DD}$ Assume, $R_2 = 1K\Omega$;

$\Rightarrow 4 = \left[\frac{1\times10^3}{R_1 + 1\times10^3}\right] 16$ or $R_1 = 3K\Omega$.

Enhancement MOSFETs: Two most popular biasing configurations for E-MOSFETs are the feedback biasing configuration and the voltage-divider configuration.

Feedback Biasing Configuration:



Feedback Biasing Configuration for N-channel E-MOSFET & DC Equivalent Circuit

The feedback connection to the Gate terminal is taken from the Drain terminal through resistor R_G. The resistor R_G brings bias voltage to the Gate terminal to turn the MOSFET on.

Applying Kirchhoff's voltage law to the input section, we get; $V_{DD} - I_D R_D + I_G R_G - V_{GS} = 0$

But, Gate current is approximately equal to zero; and hence voltage drop across R_G will be approximately equal to zero; i.e., $I_G R_G = 0$ Hence, we get; $V_{DD} - I_D R_D - V_{GS} = 0$

Or; $V_{GS} = V_{DD} - I_D R_D$ ---------(1)

Applying Kirchhoff's voltage law to the output section, we get; $V_{DD} - I_D R_D - V_{DS} = 0$

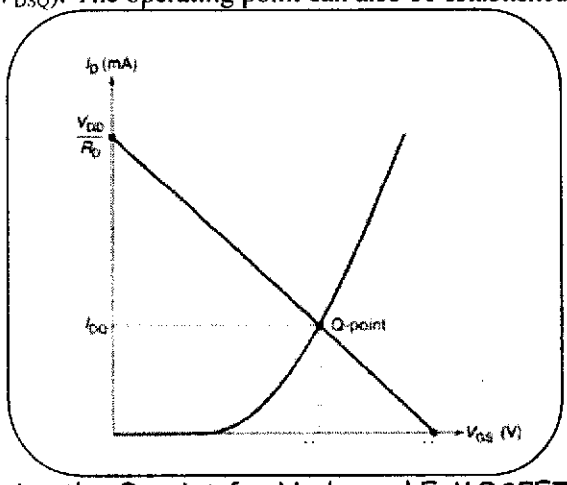
Or; $V_{DS} = V_{DD} - I_D R_D$ ---------(2)

It is clear from equations (1) and (2) that, the Gate-Source voltage (V_{GS}) and the Drain-Source voltage (V_{DS}) are equal; i.e., $V_{GS} = V_{DS}$

The operating point (Q-point) is given by (I_{DQ}, V_{DSQ}). The operating point can also be established by using graph method (shown in following Fig).

The operating point can be obtained by –

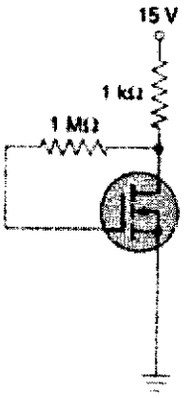
- ✓ Superimposing the equation (1) on the transfer characteristics of the MOSFET, or
- ✓ Superimposing the DC load line defined by equation (2) on the output characteristic curves of the MOSFET.



Graphical Method for Determining the Q-point for N-channel E-MOSFET

Problem: *The following Fig shows a circuit using E-MOSFET. Given that, the threshold voltage for the MOSFET is 2 V and $I_{D(on)}$ = 6 mA for $V_{GS(on)}$ = 5 V; determine the value of the operating point.*

Solution:



$R_D = 1K\Omega$
$R_F = 1M\Omega$
$V_{GS} = 5V$
$V_T = 2V$
$I_D = 6mA$.

- We have; $I_D = K(V_{GS} - V_T)^2$

  $\therefore K = 6\times10^{-3}/(5-2)^2 = \underline{0.67\ mA/V^2}$.

- The gate-source voltage in the feedback configuration is;

  $V_{GS} = V_{DD} - I_D R_D$

  $= 15 - I_D * 1\times10^3$

  $= 15 - 1000 I_D$.

- Substituting the value of I_D in the expression; $I_D = K(V_{GS} - V_T)^2$, we get;

  $I_D = 0.67\times10^{-3}(15-1000I_D - 2)^2$

  $= 0.67\times10^{-3}(13 - 1000I_D)^2$

  or $3000 I_D = 2(169 - 26000 I_D + 10^6 I_D^2)$

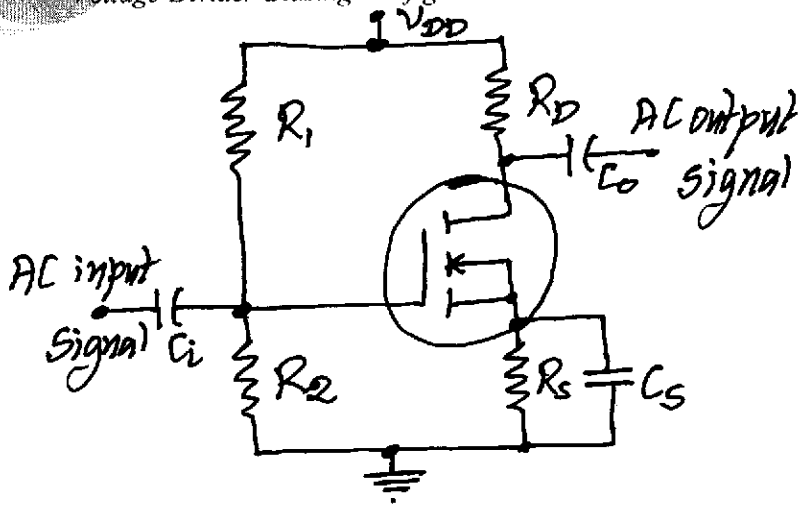
  or $2\times10^6 I_D^2 - 55000 I_D + 338 = 0 \Rightarrow I_D = \underline{9.3mA}$.

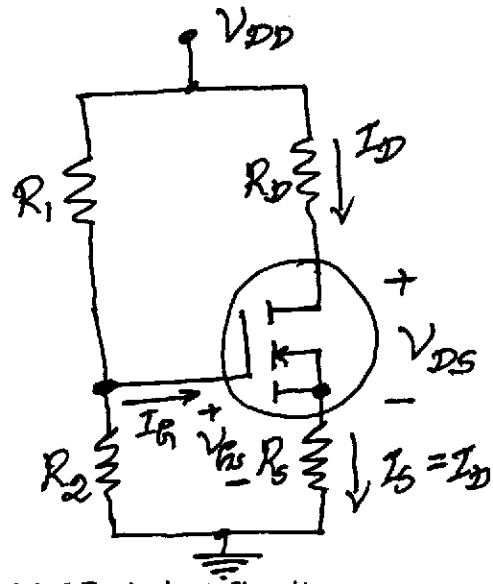
- The drain-source voltage is given by; $V_{DS} = V_{DD} - I_D R_D$

  or $V_{DS} = 15 - 9.3\times10^{-3}\times1\times10^3 = 15 - 9.3 = \underline{5.7V}$.

- Hence, the operating point is $\underline{(9.3mA, 5.7V)}$.

Voltage-Divider-Biasing Configuration:

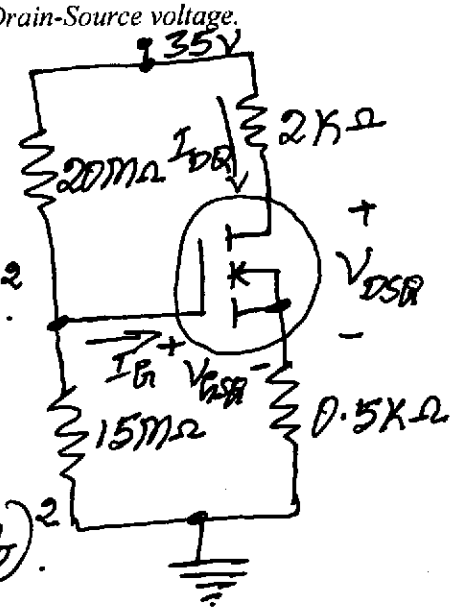




Voltage-Divider-Biasing Configuration for N-channel E-MOSFET & DC Equivalent Circuit

Problem: *The following Fig shows a voltage-divider configuration for the E-MOSFET. Given that the threshold voltage for the MOSFET is 4 V and value of $I_{D(on)}$ = 6 mA for $V_{GS(on)}$ = 8 V; use graphical method to determine the value of the Drain current, Gate-Source voltage and Drain-Source voltage.*

Solution:



- We have; $I_{D(on)} = K(V_{GS(on)} - V_T)^2$

$$\Rightarrow K = \frac{6\times10^{-3}}{(8-4)^2} = 0.375\ mA/V^2$$

- Therefore, the value of the drain current is given by; $I_D = K(V_{GS} - V_T)^2$.

or $I_D = 0.375\times10^{-3}(V_{GS} - V_T)^2$

$R_1 = 20M\Omega$ $R_2 = 15M\Omega$

$R_D = 2K\Omega$ $R_S = 0.5K\Omega$

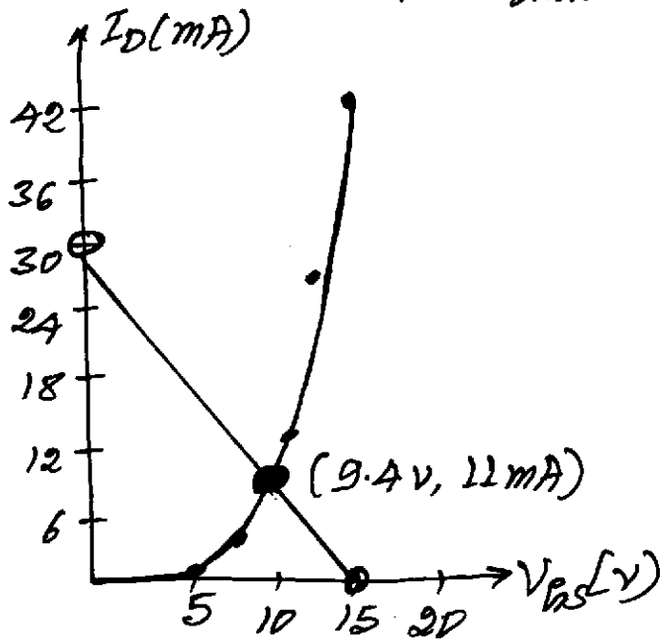
$V_T = 4V$

$I_{D(on)} = 6\ mA$

$V_{GS(on)} = 8V$

V_{GS}	I_D
5V	0.375 mA
7.5V	4.59 mA
10V	13.5 mA
12.5V	27.09 mA
15V	45.375 mA

- Using the values of V_{GS} & I_D, the transfer characteristics of the MOSFET can be drawn.



- The gate-voltage is;

$$V_G = V_{DD}\frac{R_2}{R_1+R_2}$$

$$= 35 \times \frac{15\times10^6}{(20+15)\times10^6}$$

$$= 15\text{ V}.$$

- The gate-source voltage is;

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

- For $I_D = 0$; $V_{GS} = \underline{15\text{ V}}$.
- For $V_{GS} = 0$; $I_D = 15/500 = \underline{30\text{ mA}}$.

- Hence, the load-line coordinates are $(0, 15\text{V})$ & $(30\text{mA}, 0)$.

From the above fig.; the quiescent values of gate-source voltage and the drain current are 9.4V & 11mA respectively.

- The drain-source voltage is given by;

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

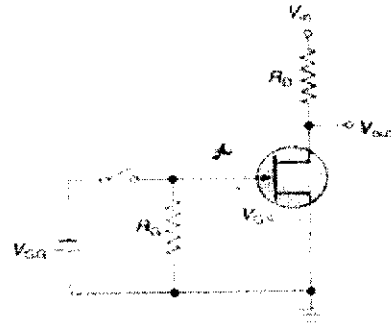
$$= 35 - 11\times10^{-3}(2\times10^3 + 0.5\times10^3)$$

$$= \underline{7.5\text{ V}}.$$

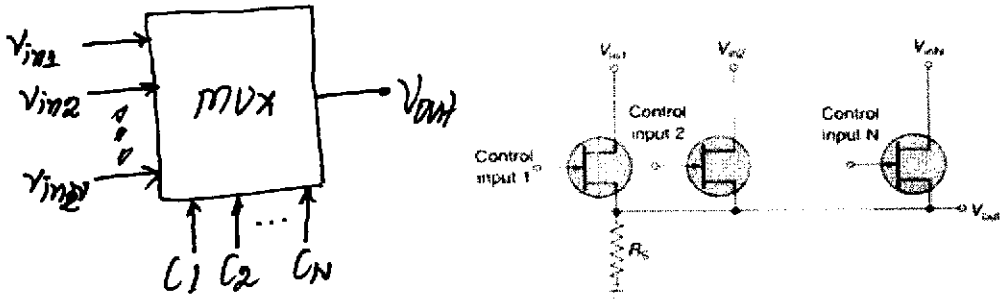
FET APPLICATIONS:

FETs offer very high value of input impedance as compared to BJTs. Some of the common applications of FETs are discussed below:

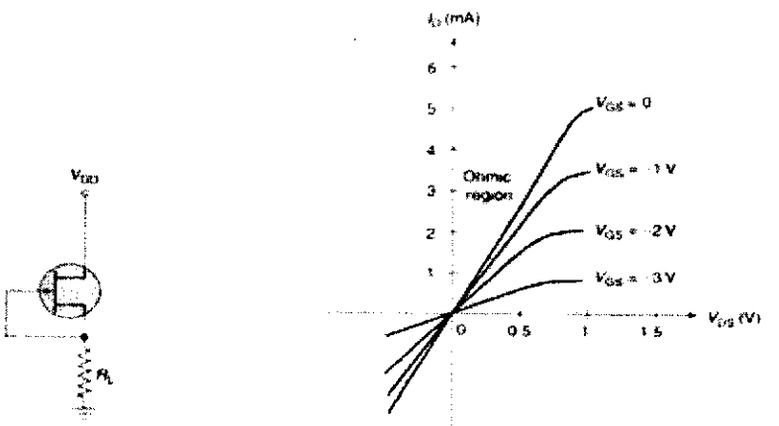
1. **Amplifiers:** FET devices are commonly used as low-noise amplifiers and buffer amplifiers. FETs are low-noise devices and hence they are used in the front-end of receivers and other electronic systems. JFETs in common-drain configuration offer high input impedance and low output impedance; and hence, they are used as buffer amplifiers to isolate the preceding stage from the following stage.
2. **Analog Switch:** FETs are used as analog switches (as shown in the following Fig). When no Gate voltage (V_{GG}) is applied, the FET operates in the saturation region and acts as a closed switch. When a negative Gate voltage is applied, the FET operates in cut-off region (offers very high resistance and acts as open switch).



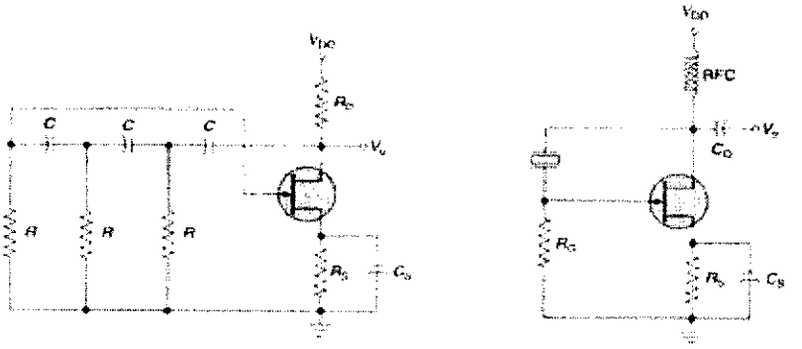
3. **Multiplexers:** FETs are used in multiplexer circuits where each FET device acts as single-pole single-through switch (as shown in the following Fig). The input signals are applied to the Drain terminals of the JFETs, while the corresponding control inputs are applied to the Gate terminals. When a control input is zero, the input is transferred to the output. All other control inputs will be made more negative than the $V_{GS(off)}$ voltage; hence, all the other input signals are blocked.



4. **Current Limiters:** FETs can also be used in current limiting applications (as shown in the following Fig). During the normal operation of the circuit, the JFET acts in the Ohmic region. When the load current increases (due to short-circuit or other reasons), the JFET operates in the saturation region. Hence, it acts as a constant current source and prevents excessive current through the load.



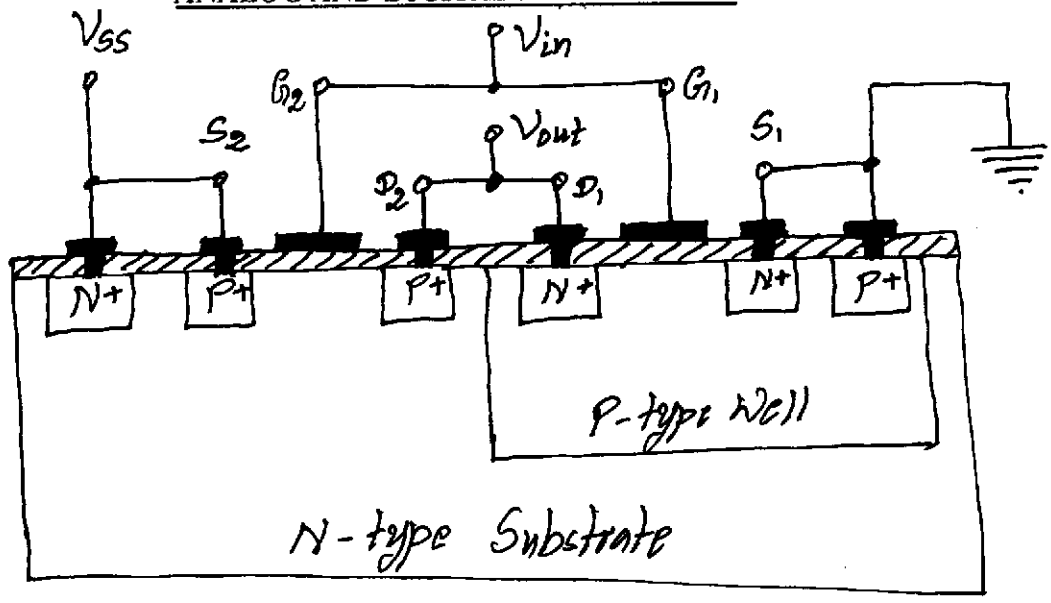
5. **Voltage-Variable Resistors (VVRs):** FETs when operated in the Ohmic region (for small positive values of V_{DS}), acts as voltage-variable resistors. In this region the Drain resistance can be controlled by the V_{GS}. For an N-channel FET, the value of R_D increases with increase in the negative value of V_{GS} (as shown in the above Fig). If an AC voltage (small peak-to-peak) is applied between the Drain the Source terminals, then FET acts as a linear resistor, for a given Gate-Source voltage. FET based VVRs are used in automatic gain control circuits.
6. **Oscillators:** FETs are also used in phase-shift oscillators & crystal controlled oscillators (as shown in the following Fig).



CMOS DEVICES:

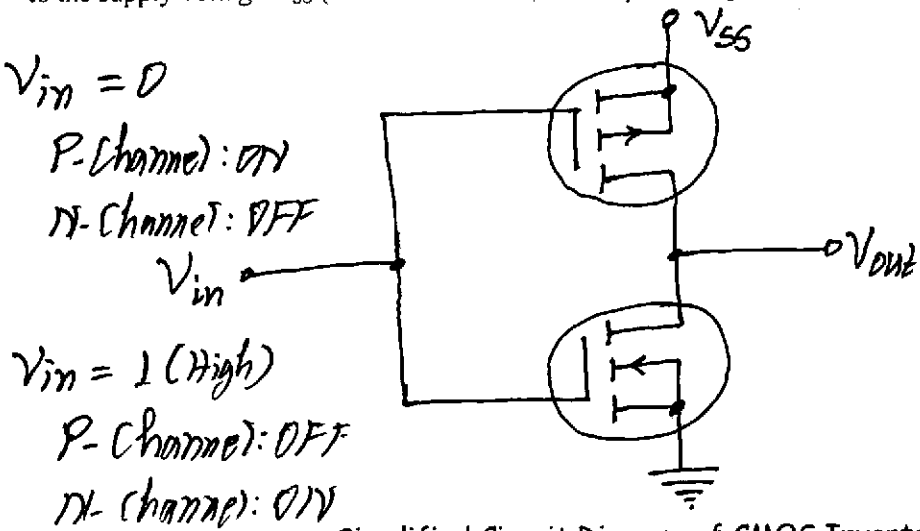
Complementary Metal Oxide Semiconductor (CMOS) are those semiconductor devices, in which both P-type and N-type E-MOSFETs are diffused onto the same chip. CMOS devices offer high input impedance, low power consumption, and require far less space, as compared to BJT-based circuits. Hence, CMOS devices are extensively used in computer logic design.

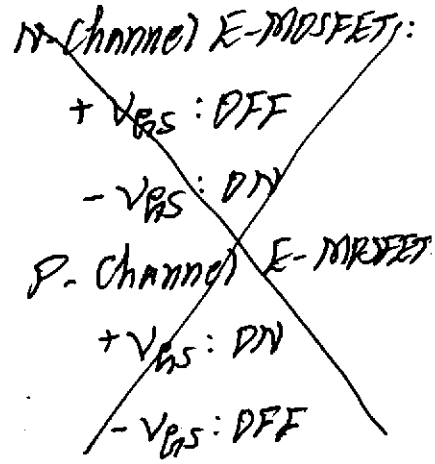
The following Fig shows the basic Inverter circuit using CMOS configuration. Inverter is a logic circuit that inverts the applied input signal (logic LOW to logic HIGH and/or vice-versa). The complementary N-type and P-type E-MOSFETs are connected in series, with their Gate terminals tied together to form the input terminal. Also the Drain terminals are connected together to form the output terminal. Source terminal of P-channel MOSFET is connected to voltage V_{SS} and the Source terminal of N-channel MOSFET is connected to the ground (as shown in the following Fig).



CMOS Inverter

The simplified circuit diagram of CMOS inverter is shown in the following Fig. When the input voltage V_{in} is logic LOW, the Gate-Source voltage (V_{G2S2}) of the P-channel E-MOSFET is equal to $-V_{SS}$ and the MOSFET is in the ON-state. This provides a low resistance path between the V_{SS} and the output terminal. The Gate-Source voltage (V_{G1S1}) of N-channel E-MOSFET is 0 V. Hence, it is OFF, resulting in very high impedance between the output terminals and the ground. Therefore, the output voltage V_{out} is equal to the supply voltage V_{SS} (or on other words, the output voltage is HIGH).





Simplified Circuit Diagram of CMOS Inverter

When the input voltage V_{in} is at logic HIGH, the Gate-Source voltage (V_{G2S2}) of the P-channel E-MOSFET is 0 V. Hence, this MOSFET is in the OFF-state. The Gate-Source voltage (V_{G1S1}) of N-channel E-MOSFET is equal to the supply voltage (V_{SS}). Hence, it is switched ON, and offers a low resistance path. Therefore, the output voltage (V_{out}) is approximately 0 V; a logic LOW.

ANALOG AND DIGITAL ELECTRONICS

WAVE-SHAPING CIRCUITS

INTEGRATED CIRCUIT (IC) MULTIVIBRATORS:

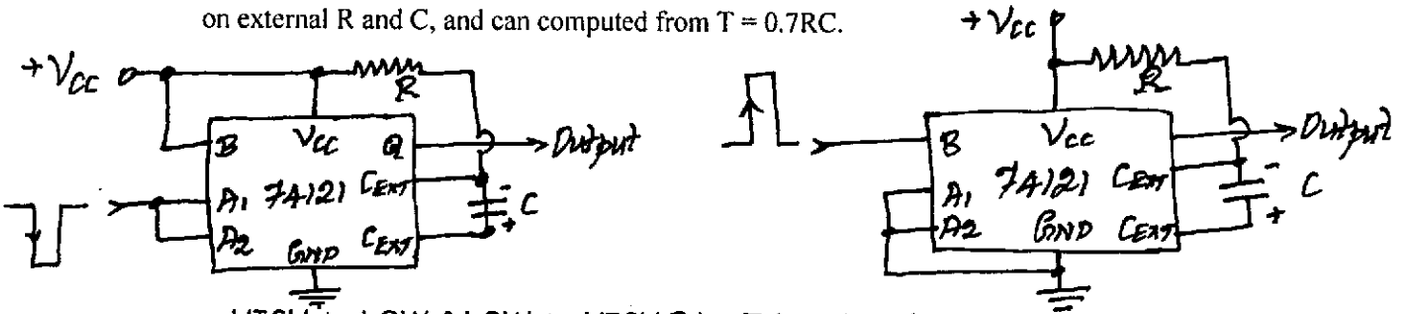
A multivibrator (like an oscillator) is a circuit with regenerative feedback, which produces a pulsed output. There are three basic types of multivibrator circuits:

- Astable – has no stable states, but switches continuously between two states. This action produces a train of square wave pulses at a fixed frequency.
- Monostable – one of the states is stable, but the other state is unstable (transient).
- Bistable – the circuit is stable in either state.

Digital IC-Based Monostable Multivibrators:

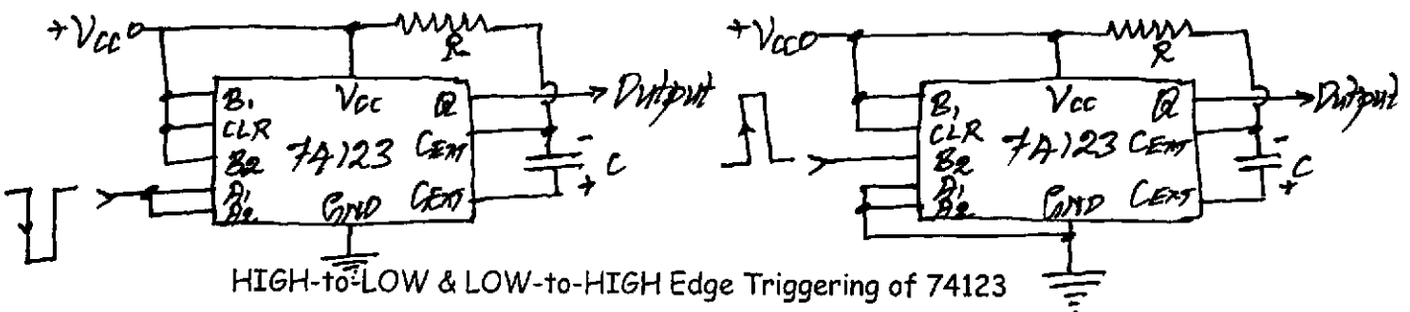
The ICs that can be used as monostable multivibrators include –

- TTL Family
  - 74121 – single monostable multivibrator: The IC provides features for triggering on either LOW-to-HIGH or HIGH-to-LOW edge trigger pulses. Output pulse width depends on external R and C, and can computed from T = 0.7RC.



HIGH-to-LOW & LOW-to-HIGH Edge Triggering of 74121

  - 74122 – single retriggerable monostable multivibrator
  - 74123 – dual retriggerable monostable multivibrator: The IC provides features for triggering on either LOW-to-HIGH or HIGH-to-LOW edge trigger pulses. Output pulse width depends on external R and C, and can computed from T = 0.28RC * [1+(0.7/RC)], where R and C are, respectively in kilo-ohms and pico-farads; and T is in nano-seconds.

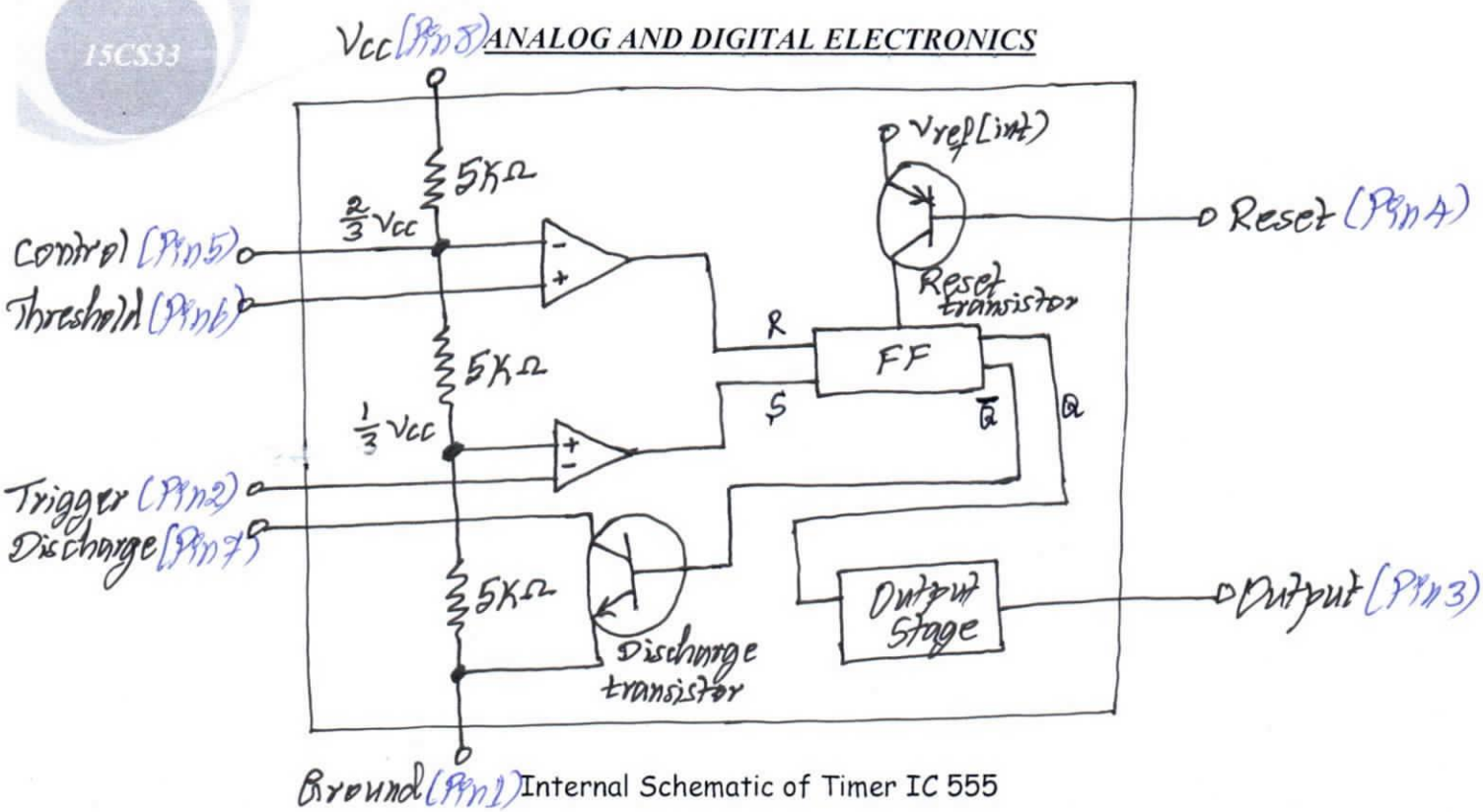


HIGH-to-LOW & LOW-to-HIGH Edge Triggering of 74123

- CMOS Family
  - 4098B – dual retriggerable monostable multivibrator

Timer IC-Based Multivibrators:

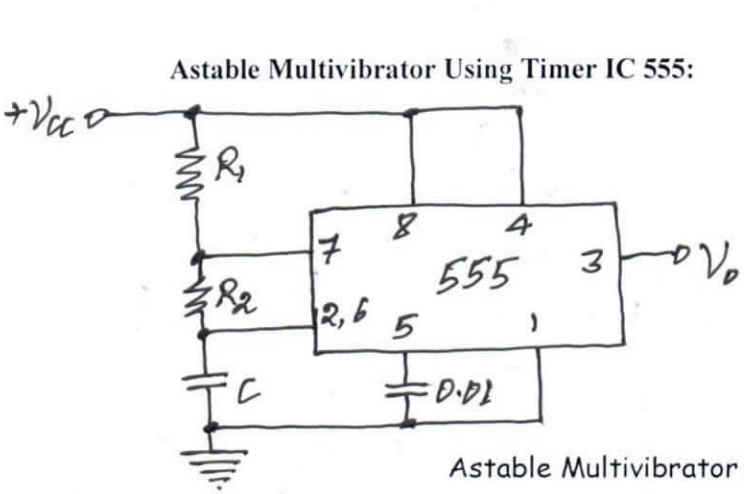
Timer IC is the one of the most commonly used general-purpose linear integrated circuits.

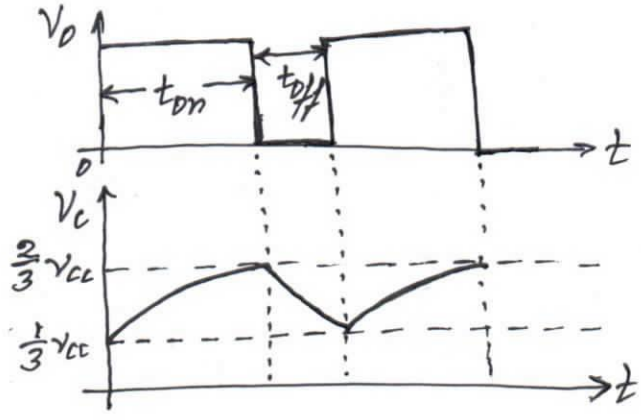


Internal Schematic of Timer IC 555

The Timer IC 555 comprises two Op-Amp comparators, a flip-flop, a discharge transistor, a reset transistor, three identical resistors and an output stage. The resistors set the reference voltage levels at the non-inverting input of the lower comparator and inverting input of the upper comparator at $+V_{CC}/3$ and $2V_{CC}/3$, respectively. The output of two comparator feed SET and RESET inputs of the Flip-Flop. This decided the logic state of its output and subsequently the final output. The Flip-Flops complementary outputs feed the output stage and the base of the discharge transistor. Hence, when the output is HIGH, the discharge transistor is OFF and when the output is LOW, the discharge transistor is ON.

Astable Multivibrator Using Timer IC 555:





Astable Multivibrator & Its Relevant Waveforms

The working is as follows:

- Initially, capacitor C is fully discharged, which forces output to go to HIGH-state.
- Now, the discharge transistor allows the capacitor C to charge from $+V_{CC}$ through R_1 and R_2.

- When the voltage across C exceeds $+2V_{CC}/3$, the output goes to LOW-state; and the discharge transistor is switched ON.
- Hence, the capacitor C begins to discharge through R_2 and the discharge transistor.
- When the voltage across C falls below $+V_{CC}/3$, the output goes back to the HIGH-state.
- The charge and the discharge cycles repeat and the circuit behave like a multivibrator.

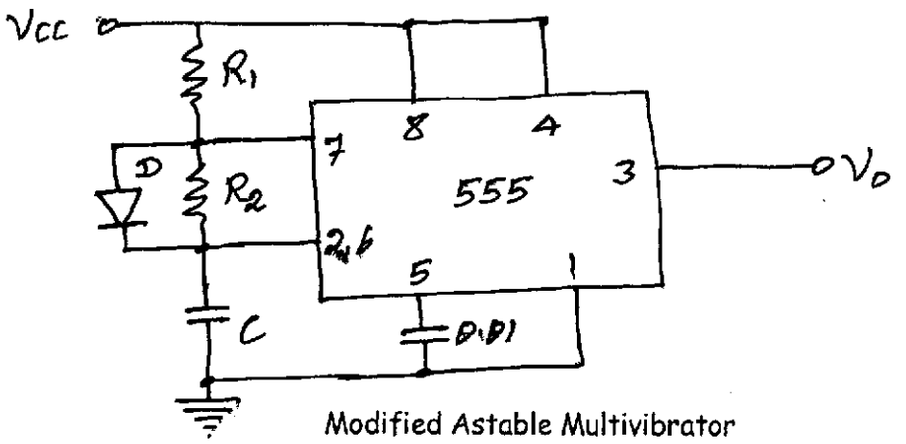
HIGH-state time period, $T_{HIGH} = 0.69 * (R_1 + R_2) * C$

LOW-state time period $T_{LOW} = 0.69 * R_2 * C$

Time period $T = 0.69 * (R_1 + 2R_2) * C$

Frequency $F = \frac{1}{0.69*(R_1+2R_2)*C}$

In the above Fig, the HIGH-state time period is always greater than the LOW-state time period. The following Fig shows a modified circuit where HIGH-state and LOW-state time periods can be choosen independently.



Modified Astable Multivibrator

HIGH-state time period, $T_{HIGH} = 0.69 * R_1 * C$

LOW-state time period $T_{LOW} = 0.69 * R_2 * C$

For $R_1 = R_2 = R$;

Time period $T = 1.38 * R * C$

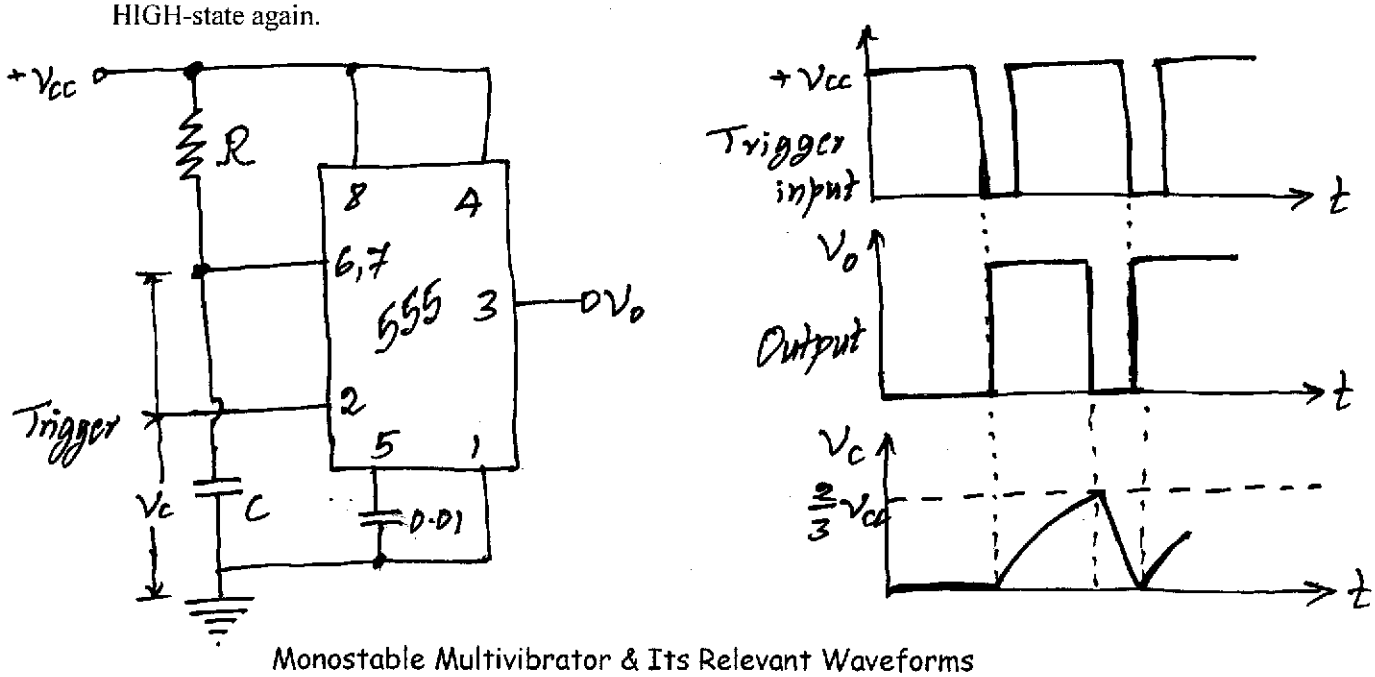
Frequency $F = \frac{1}{1.38*R*C}$

Monostable Multivibrator Using Timer IC 555:

The monostable multivibrators are also referred to as monoshots. The working of the following monoshot shown in the Fig is as follows:

- Trigger pulse is applied to Terminal-2 of the IC, which should initially be kept at $+V_{CC}$.
- A HIGH at terminal-2 forces the output to LOW-state.
- A HIGH-to-LOW trigger pulse at terminal-2 holds the output in the HIGH-state and simultaneously allows the capacitor to charge from $+V_{CC}$ through R.

- When the capacitor voltage exceeds $+2V_{CC}/3$, the output goes back to the LOW-state.
- Once again, another trigger pulse will have to be applied to terminal-2 to make the output to go to HIGH-state again.



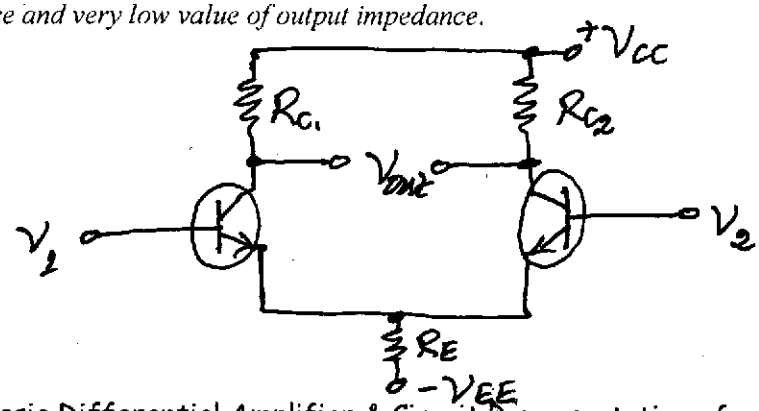
Monostable Multivibrator & Its Relevant Waveforms

Every time the timer is appropriately triggered, the output goes to HIGH-state, and stays there for a time period taken by capacitor to charge from 0 to $+2V_{CC}/3$. This time period, which equal the monoshot output pulse width, is given by; $T = 1.1 * R * C$

INTRODUCTION TO OPERATIONAL AMPLIFIERS

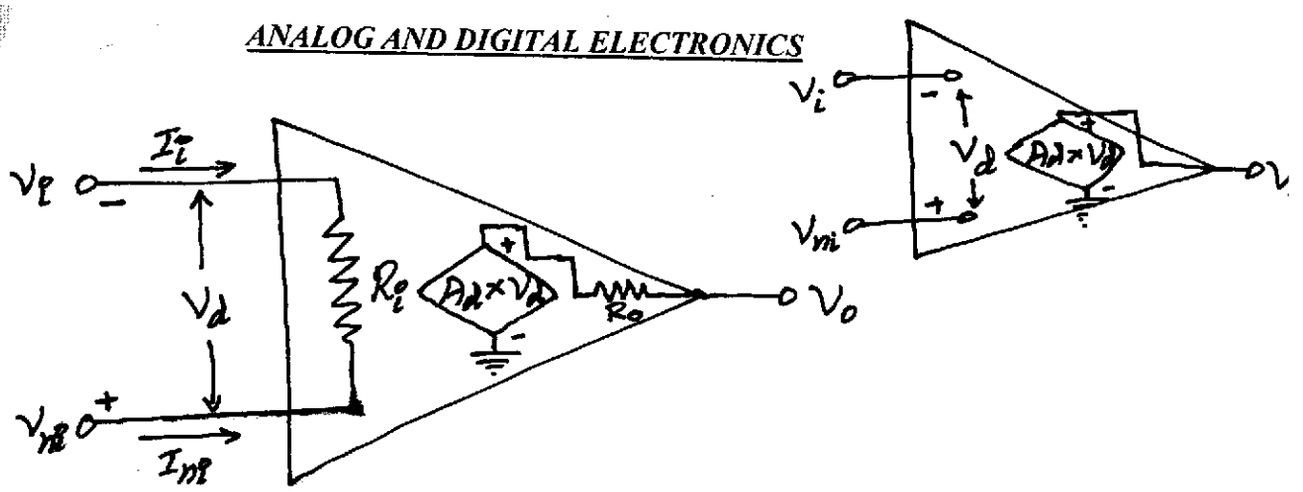
IDEAL OP-AMP versus PRACTICAL OP-AMP:

*An **Op-Amp** is a direct-coupled high gain, high bandwidth differential amplifier with very high value of input impedance and very low value of output impedance.*



Basic Differential Amplifier & Circuit Representation of an OP-Amp

The following Fig shows the Thevenin's Equivalent Model of an Ideal Op-Amp and a Practical Op-Amp.



Thevenin's Equivalent Model of an Ideal Op-Amp and a Practical Op-Amp

V_i and V_{ni} are, respectively, inverting and non-inverting inputs; and A_d is the open loop differential voltage gain. In a practical Op-Amp, there are loading effects at the input and output ports, due to finite values of input and output resistances.

The ideal Op-Amp model was derived to simplify circuit calculations. The ideal Op-Amp model makes three assumptions:

1. Input resistance (impedance), $R_i = \infty$
2. Output resistance (impedance), $R_o = 0$
3. Open-loop (differential voltage) gain, $A_d = \infty$

Based on these three assumptions, other assumptions can be derived:

1. Since $R_i = \infty$, $I_i = I_{ni} = 0$
2. Since $R_o = 0$, $V_o = A_d * V_d$
3. Zero DC input and output offset voltages
4. Bandwidth and slew rate are also infinite, as no frequency dependencies are assumed.
5. Drift is also zero, as there is no changes in performance over time, temperature, power supply variations, and so on
6. Since output voltage depends only on differential input voltage, it rejects any voltage common to both inputs. Hence, common mode gain = 0

Open-loop gain is the differential voltage gain in the absence of any positive or negative feedback. Practical Op-Amps have –

1. Input impedance can vary from hundred of kilo-ohms (for some low-grade Op-Amps) to tera-ohms (for high grade Op-Amps).
2. Output impedance may be in the range of 10 to 100 Ω
3. Open-loop gain in the range of 10,000 to 1, 00,000
4. Bandwidth is limited and is specified by gain-bandwidth product

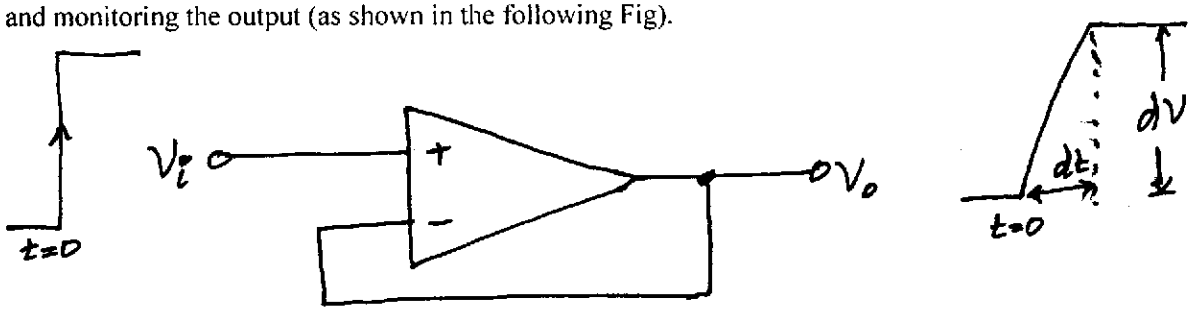
5. There may be some finite DC output (referred to as output offset voltage), even when both the inputs are grounded.

PERFORMANCE PARAMETERS:

The key parameters of an Op-Amp decide its suitability for a particular application: Key parameters of Op-Amp include the following:

Bandwidth: *of an Op-Amp is the range of frequencies that it can amplify for a given amplifier gain.* The bandwidth is usually expressed in terms of the unity gain crossover frequency (also called gain-bandwidth product). It is 1 MHz in the case of Op-Amp 741. It could be as high as 1500 MHz in the case of high bandwidth Op-Amps.

Slew Rate: *is the rate of change of output voltage with time.* It gives us an idea how well the Op-Amp output voltage follows a rapidly changing waveform at the input. It is determined by applying a step input and monitoring the output (as shown in the following Fig).

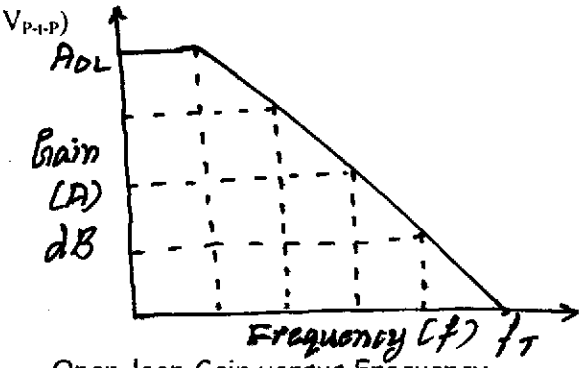


Response of Op-Amp to Step Input

The step input simulates the large signal conditions. The incapability of the Op-Amp to follow rapidly rising and falling input is due to the minimum charge and discharge times required by an internally connected capacitor across the output; i.e., slew rate limits the large signal bandwidth. Hence, the rate of change of output should be less than the slew rate of the Op-Amp. Peak-to-peak output voltage swing for a sinusoidal signal ($V_{P\text{-}t\text{-}P}$), slew rate and bandwidth are interrelated by the following equation:

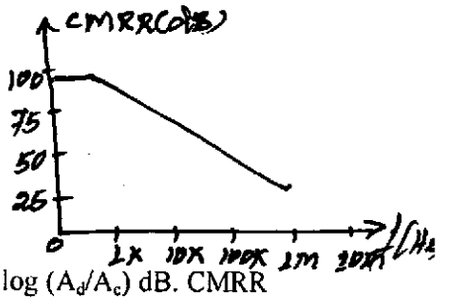
Bandwidth (highest frequency, f_{MAX}) = Slew rate / (π * $V_{P\text{-}t\text{-}P}$)

Open-Loop Gain: *is the ratio of single-ended output to the differential input.* The *(closed) loop gain* depends upon the (application) circuit. The following Fig shows the open-loop gain versus frequency curve of an Op-Amp. The gain error at any given frequency is given by the ratio of the closed-loop gain to the open-loop gain.



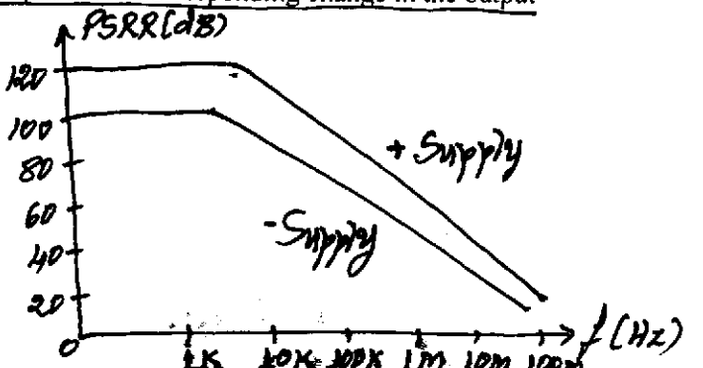
Open-loop Gain versus Frequency

Common Mode Rejection Ratio (CMRR): *the ratio of the desired differential gain (A_d) to the undesired common mode gain (A_c).* It is a measure of the ability of the Op-Amp to suppress common mode signals.



The ratio of CMRR (a DC parameter) is usually expressed as CMR, given by 20 log (A_d/A_c) dB. CMRR is also defined as the ratio of change in the common mode input to the corresponding change in the output offset voltage.

Power Supply Rejection Ratio (PSRR): *is defined as the ratio of change in the power supply voltage to the corresponding change in the output voltage.* PSRR (a DC parameter) value falls with increase in frequency. The following Fig shows PSRR versus frequency graph of AD829 Op-Amp.



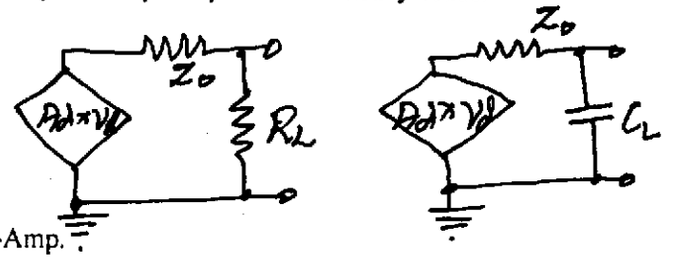
PSRR versus frequency graph of AD829 Op-Amp

Input Impedance: *is the impedance looking into the input terminals of the Op-Amp and is expressed in terms of resistance.* The effective input impedance will be different from that is specified in the data sheets, when the Op-Amp is used in the closed-loop mode. In an inverting amplifier, the effective input impedance equals the input resistance connected externally from the source of input signal to the inverting input terminal of the Op-Amp. In the non-inverting amplifier, it equals the product of the loop gain and the specified Op-Amp input impedance.

Output Impedance: *is defined as the impedance between the output terminal of the Op-Amp and ground.* Output impedance becomes a critical parameter, when using output of Op-Amps to drive heavy loads. The expression for the output in the case of –

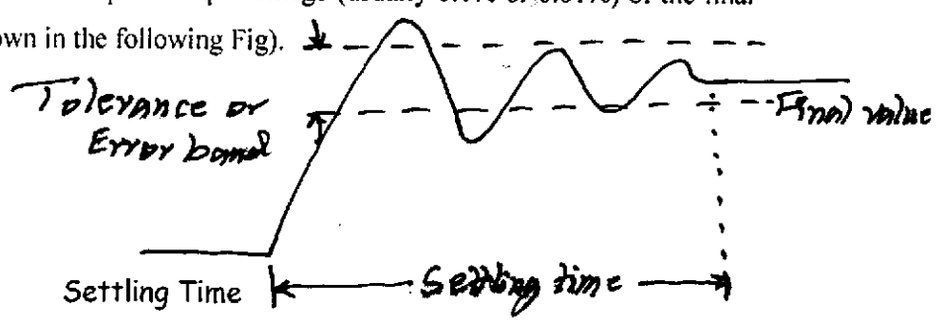
Resistive load; $Vo = A_d * V_d \left[\frac{R_L}{R_L + Z_o}\right]$

Capacitive load; $Vo = A_d * V_d \left[\frac{1}{j\left(f/f_o\right)+1}\right]$



where, $f_o = 1/2\pi Z_o C_L$ and Z_o is the output impedance of the Op-Amp.

Settling Time: *gives the response of the Op-Amp to large step signals.* It is parameter specified in the case of high-speed Op-Amps or Op-Amps with a high value of gain-bandwidth product. It is expressed as time taken by the Op-Amp output to settle within a specified percentage (usually 0.1% or 0.01%) of the final value in response to a step input (as shown in the following Fig).



Offsets and Offset Drifts: An ideal Op-Amp should produce a zero output for a zero differential input. But, it is not so in the case of real Op-Amps. It is observed that, we need to apply DC differential voltage externally to get a zero output. This externally applied input is referred to as *input offset voltage. Output*

offset voltage is the voltage at the output with both the input terminals grounded. The difference between the two bias currents flowing towards the inputs of the Op-Amp is referred to as *input offset current.*

Problem: *Op-Amp LM 741 is specified to have slew rate of 0.5 V/μs. If the Op-Amp were used as amplifier and the expected peak output voltage were 10V, determine the highest sinusoidal frequency that would get satisfactorily amplified.*

Solution: Given, Slew rate = 0.5 V/μs & $V_p = 10V$.

The highest sinusoidal freq., f_{MAX} = Slew rate / $(\pi * V_p)$

$= (0.5 \times 10^{-6}) / [\pi * 2 * 10)$

$= 7.96$ KHz.

Problem: *The differential voltage gain and CMRR of an Op-Amp when expressed in decibels are 110 dB and 100 dB, respectively. Determine the common mode gain expressed as a ratio.*

Solution: $CMRR = 20 \log (A_d/A_{cm}) = 20 \log A_d - 20 \log A_{cm}$

i.e., $20 \log A_{cm} = 20 \log A_d - CMRR = 110 - 100 = 10$ dB.

$\therefore \log A_{cm} = 10/20 = 0.5$

$\Rightarrow A_{cm} = \text{Antilog } 0.5 = 3.16$

Problem: *In the case of certain Op-Amp, 0.5 V change in the common mode input causes a DC output offset change of 5 μV. Determine CMRR in dB.*

Solution:

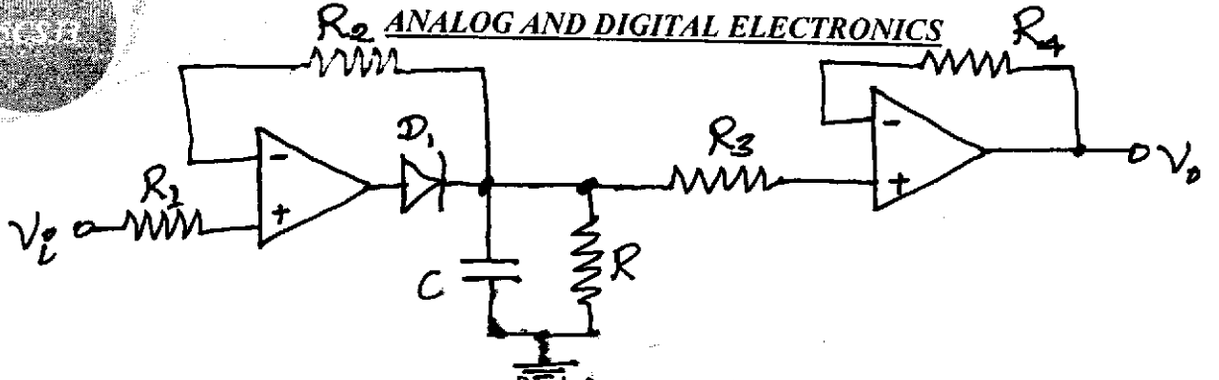
$CMRR = \Delta V_{cm} / \Delta V_{os} = 0.5 / [5 \times 10^{-6}) = 10^5$.

CMRR in dB = $20 \log 10^5 = 100$ dB.

OPERATIONAL AMPLIFIER APPLICATION CIRCUITS

PEAK DETECTOR CIRCUIT:

Peak detector circuit produces a voltage at the output equal to the peak amplitude (positive or negative) of the input signal.



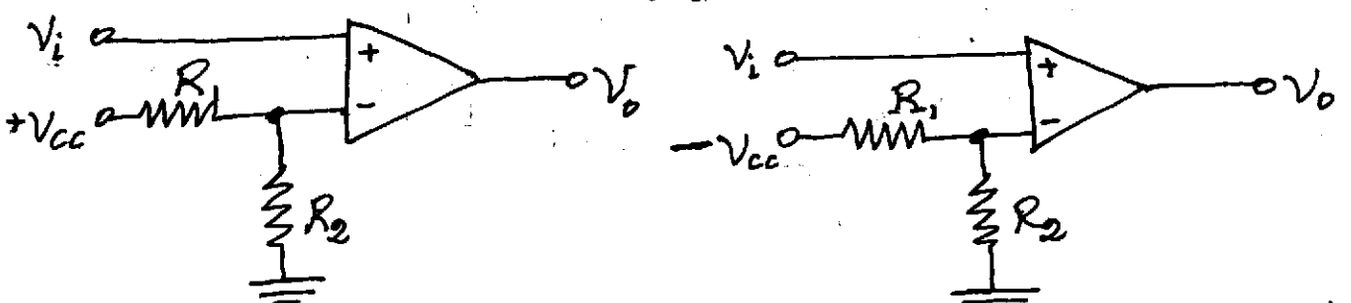
Peak Detector Circuit

During the positive half cycles of input, the diode D_1 will be forward biased. The capacitor C rapidly charges to the peak, from the output of the Op-Amp. As the input starts decreasing beyond the peak, the diode gets reverse-biased; and hence, capacitor will be isolated from the output of the Op-Amp. Now, the capacitor starts to discharge through resistance R connected across it. The value of this resistor will be much larger to allow a discharge path. The buffer circuit connected ahead of the capacitor prevents any discharge of the capacitor due to loading effects. This circuit can be made to respond to the negative peaks by reversing the polarity of the diode.

COMPARATOR:

A comparator circuit is a two-input, one-output building block that produces a high or low output depending upon the relative magnitudes of the two inputs. An Op-Amp produces (without feedback) either positively saturated or negatively saturated output voltage depending upon whether the amplitude of the voltage applied at the non-inverting input terminal is more or less positive than the voltage applied at the inverting input terminal.

One of the inputs of the comparator is applied with a reference voltage and the other input is fed with the input voltage that needs to be compared with the reference voltage. The reference voltage may be a positive or negative voltage (as shown in the following Fig).



Non-inverting Comparator with Positive Reference & Negative Reference

V_{REF} for non-inverting comparator with positive reference is given by $+V_{CC} * [R_2/(R_1+R_2)]$.

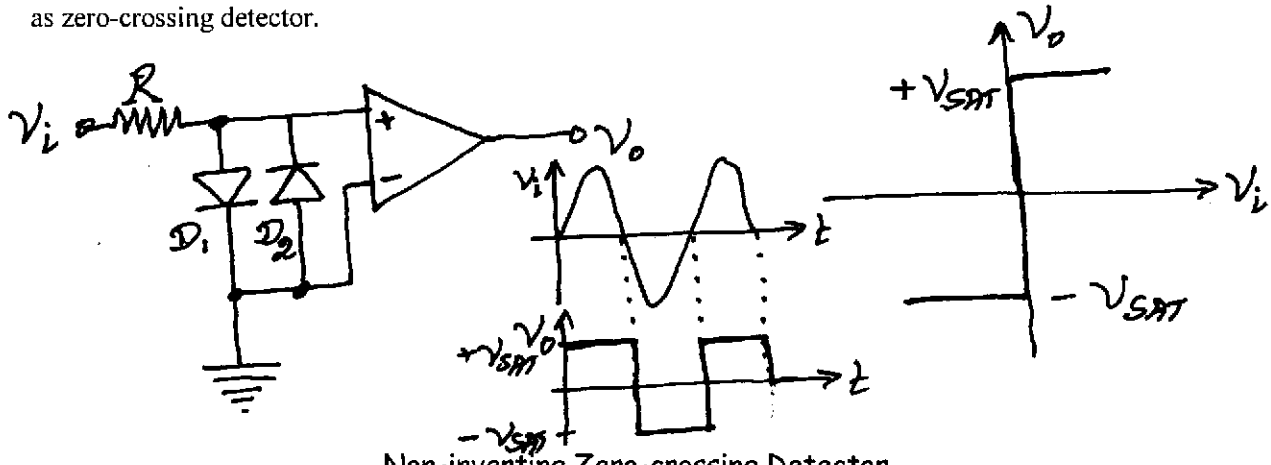
V_{REF} for non-inverting comparator with negative reference is given by $-V_{CC} * [R_2/(R_1+R_2)]$.

Inverting-type voltage comparators can similarly be built for positive and negative reference voltages.

Summary: In comparator –

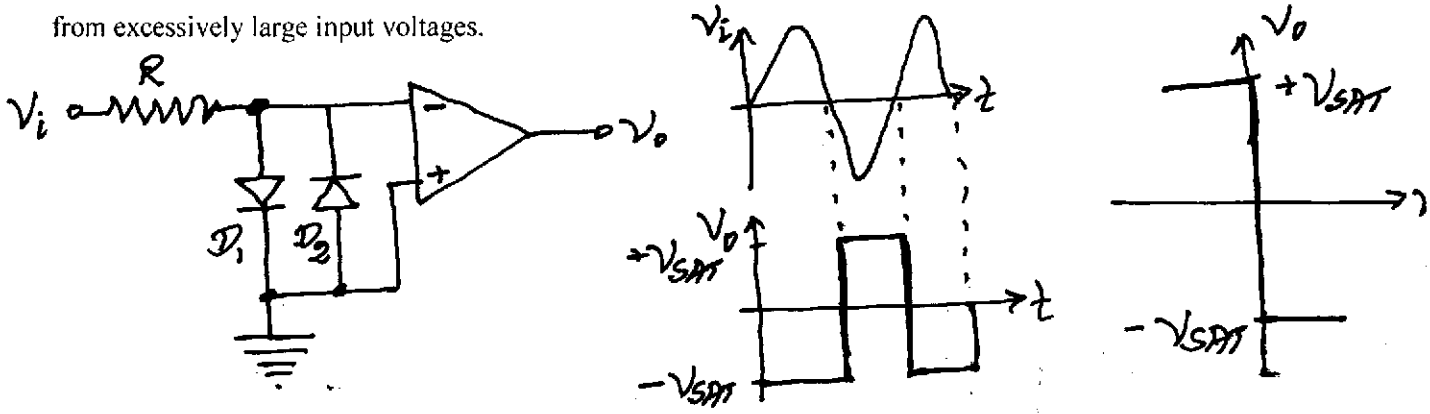
- ✓ If the input voltage is less than the reference voltage, then the output voltage will be negatively saturated.
- ✓ If the input voltage is equal to the reference voltage, then the output voltage will be zero.
- ✓ If the input voltage is greater than the reference voltage, then the output voltage will be positively ~~negatively~~ saturated.

Zero-Crossing Detector: A special case of comparator, where the reference voltage is zero, is referred to as zero-crossing detector.



Non-inverting Zero-crossing Detector

Here, an input more positive than zero leads to a positively saturated output (as shown in the waveform above). The diodes connected at the input are to protect the sensitive input circuits inside the Op-Amp from excessively large input voltages.

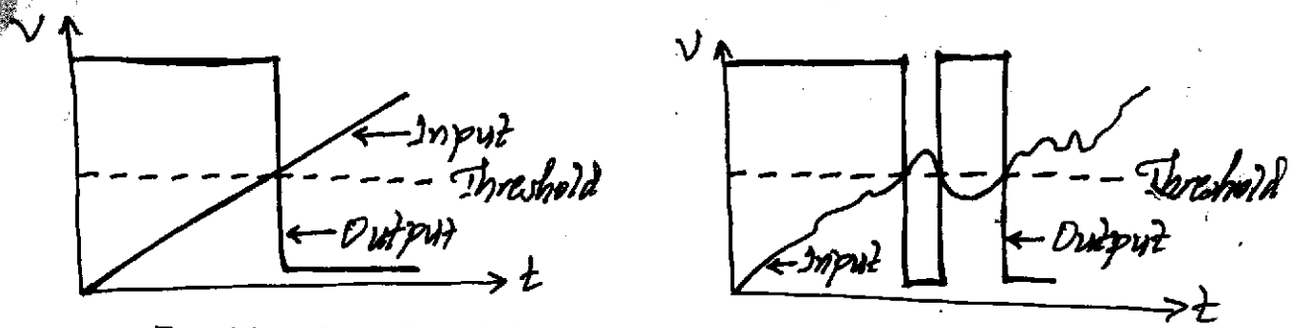


~~Non~~-Inverting Zero-crossing Detector

Here, an input more positive than zero leads to a negatively saturated output (as shown in the waveform above).

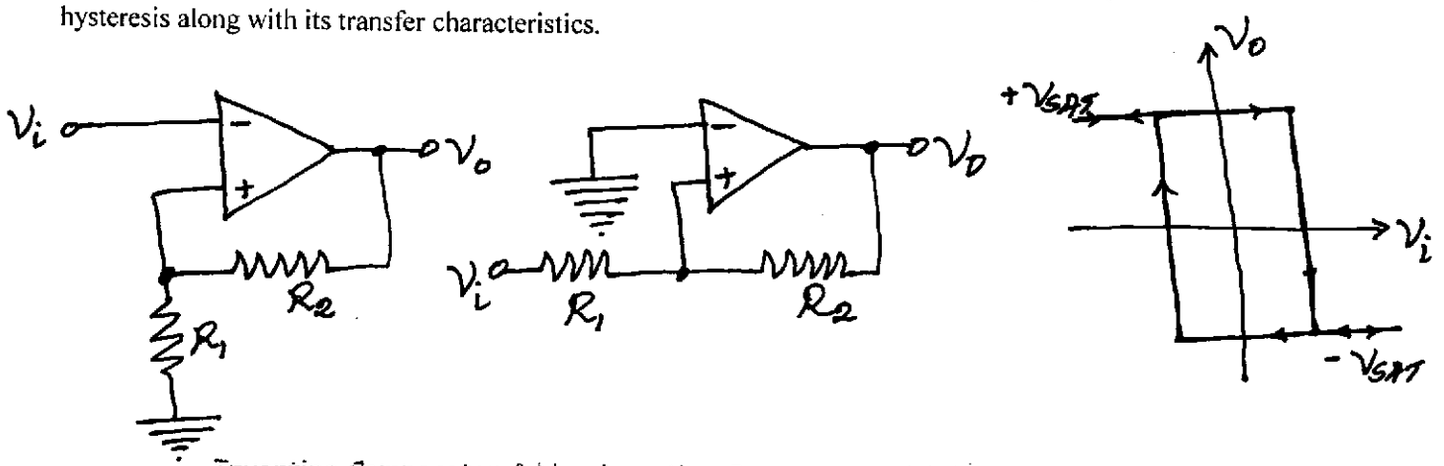
Application of zero-crossing detector is to convert sine wave signal to a square wave signal.

Comparator with Hysteresis: When the input signal applied to the comparator contains noise, transitions at the output around the trip point tend to become highly erratic (as shown below).



Transitions Caused by Ideal Input Signal & Noisy Input Signal

The following Fig shows the circuit schematic of a non-inverting and inverting comparators with hysteresis along with its transfer characteristics.



Inverting Comparator & Non-inverting Comparator with Hysteresis

Assume that, the output is in positive saturation ($+V_{SAT}$). Voltage at non-inverting input is $+V_{SAT} * R_1 / (R_1 + R_2)$. Due to this small positive voltage at the non-inverting input, the output is reinforced to stay in positive saturation.

Now, the input signal needs to be more positive than this voltage for the output to go to negative saturation. Once the output goes to the negative saturation ($-V_{SAT}$), voltage feedback to the non-inverting input becomes $-V_{SAT} * R_1 / (R_1 + R_2)$. Due to this small negative voltage at the non-inverting input, the output is reinforced to stay in negative saturation.

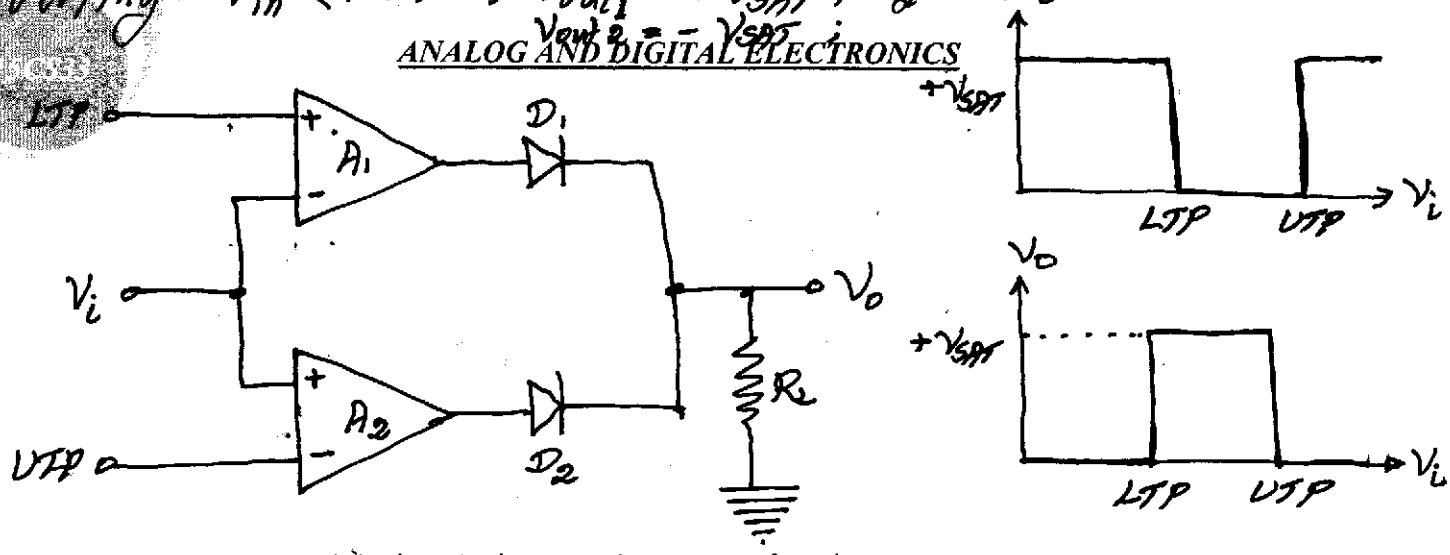
In this manner, the circuit offers a hysteresis of $2V_{SAT} * R_1 / (R_1 + R_2)$.

Non-inverting comparator with hysteresis can explained in the similar manner. In this case, the upper and the lower trip points (UTP & LTP) are $+V_{SAT} * R_1 / R_2$ and $-V_{SAT} * R_1 / R_2$. Hysteresis is equal to $2V_{SAT} * R_1 / R_2$.

Window Comparator: In window comparator, the output changes state when the input voltage goes above or below the reset reference voltage. In a window comparator, there are two reference voltages, called lower and upper trip points. Output is in one state, when it is inside the window created by the lower and the upper trip points and in the other state when it is outside the window.

Non-Inverting: $V_{in} > UTP$; $V_{out} = -V_{SAT}$; $D_1 \rightarrow FB$; $V_{out_2} = +V_{SAT}$; $V_o = +V_{SAT}$

Inverting: $V_{in} < LTP$; $V_{out_1} = +V_{SAT}$; $D_2 \rightarrow RB, V_o$ $V_{out_2} = -V_{SAT}$;



Window Comparator & Its Transfer Characteristics

When the input voltage is less than the voltage reference corresponding to the LTP, output of the Op-Amp A_1 is at $+V_{SAT}$ and that of Op-Amp A_2 is $-V_{SAT}$. Diodes D_1 and D_2 are respectively, forward- and reverse-biased. Hence, output across R_L is $+V_{SAT}$.

When the input voltage is greater than the voltage reference corresponding to the UTP, output of the Op-Amp A_1 is at $-V_{SAT}$ and that of Op-Amp A_2 is $+V_{SAT}$. Diodes D_1 and D_2 are respectively, reverse- and forward-biased. Hence, output across R_L is again $+V_{SAT}$.

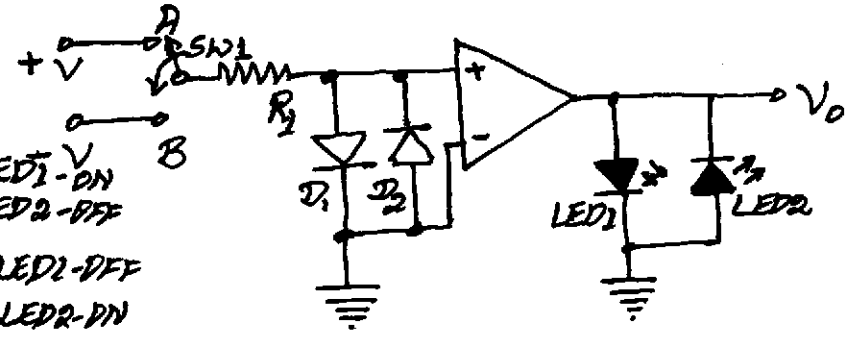
When the input voltage is greater than LTP and less than UTP, the output of both Op-Amps is at $-V_{SAT}$. Hence, both the diodes are reverse-biased and output across R_L is zero.

The first waveform shown in the above Fig shows the transfer characteristics of window comparator shown. The second waveform shown in the above Fig shows the transfer characteristics of window comparator, if we interchange the positions of LTPs and UTPs.

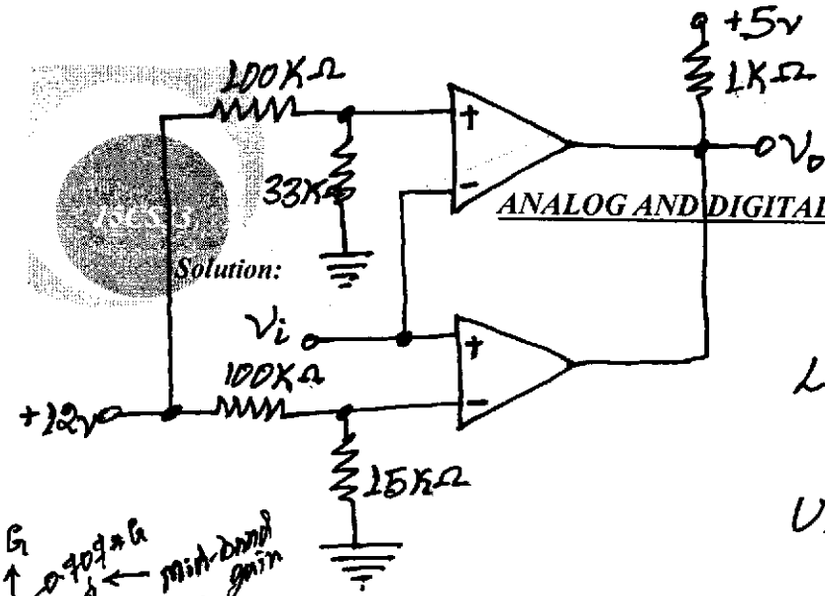
Problem: *Refer to the comparator circuit given below. Determine the state of LED1 and LED2, when the switch SW1 is in (a) position A and (b) position B.*

Solution:

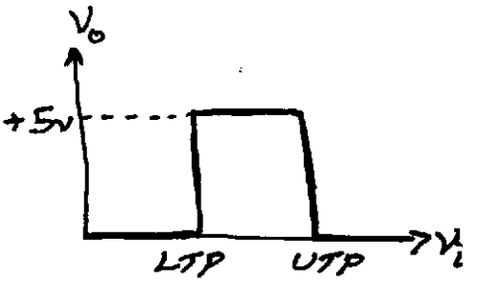
SW2	V_{ni}	V_o	
A	$+0.7_V$	$+V_{SAT}$	LED1-ON, LED2-OFF
B	-0.7_V	$-V_{SAT}$	LED1-OFF, LED2-ON



Problem: *The following Fig shows a non-inverting type of window comparator. Determine the lower and upper trip points of the comparator and also draw the output voltage V_o versus input voltage V_i transfer characteristics.*

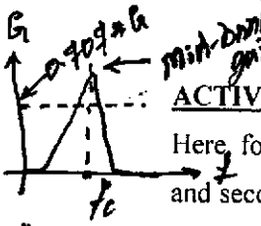


Solution:



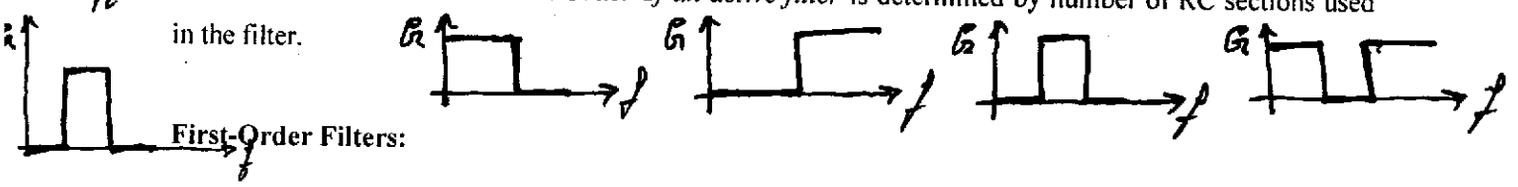
$$LTP = \frac{12 \times 15 \times 10^3}{(100+15)\times 10^3} = 1.565V.$$

$$UTP = \frac{12 \times 33 \times 10^3}{(100+33)\times 10^3} = 2.977V.$$

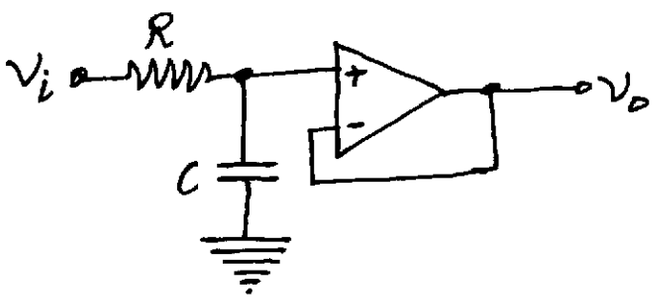


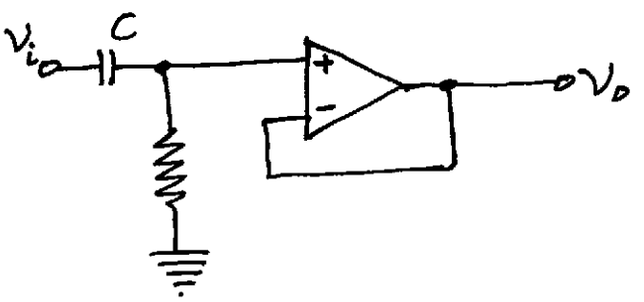
ACTIVE FILTERS:

Here, four types of active filters, viz., low-pass, high-pass, band-pass, and band-reject filters of first-order and second-order will be studied. *Order of an active filter* is determined by number of RC sections used in the filter.



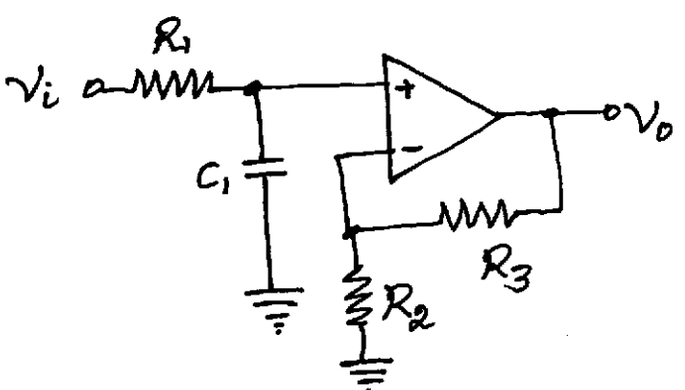
First-Order Filters:

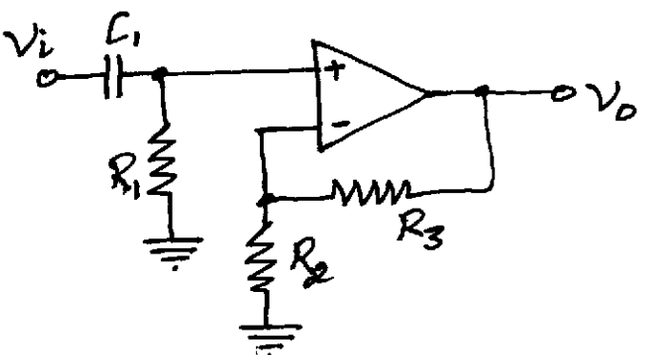




First-order Active Filters (Non-inverting): Low-pass & High-pass

In the case of low-pass circuit; at low frequencies, reactance offered by the capacitor is much larger than the resistance value. Hence, the applied input signal appears at the output un-attenuated. At high frequencies, the capacitive reactance becomes much smaller than the resistance value. Hence, the output will be zero. When the signal frequency is such that, the capacitive reactance is equal to resistance value, the output is 0.707 times the input. This is called upper cut-off frequency. $f_C = \frac{1}{2\pi RC}$



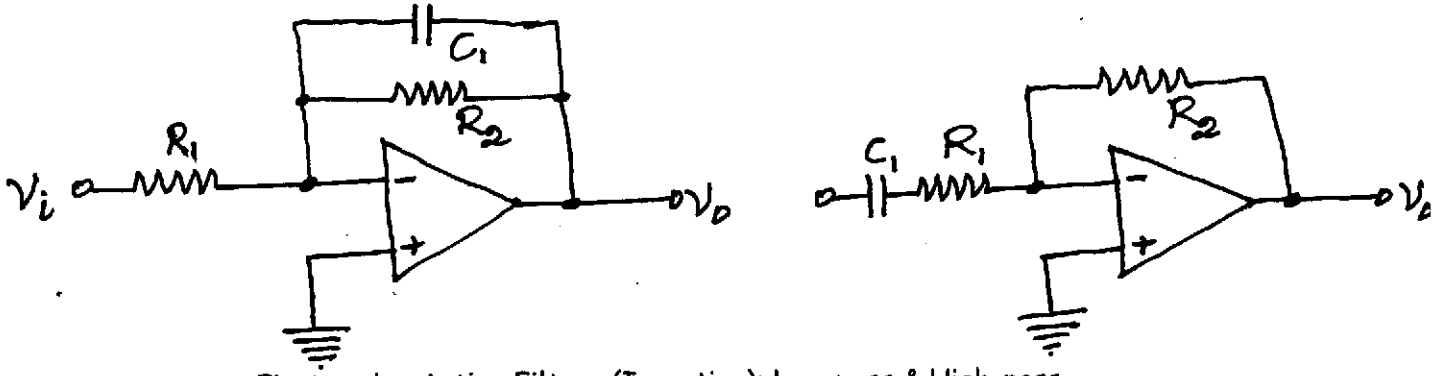


First-order Filters with Gain (Non-inverting): Low-pass & High-pass

If an active filter with desired amplification is required; the above circuits may be modified as given in the ~~following~~ above Fig. The voltage gain is given by;

$$A_v = 1 + \frac{R_3}{R_2}$$

These filters could also be implemented using inverting amplifier configuration.



First-order Active Filters (Inverting): Low-pass & High-pass

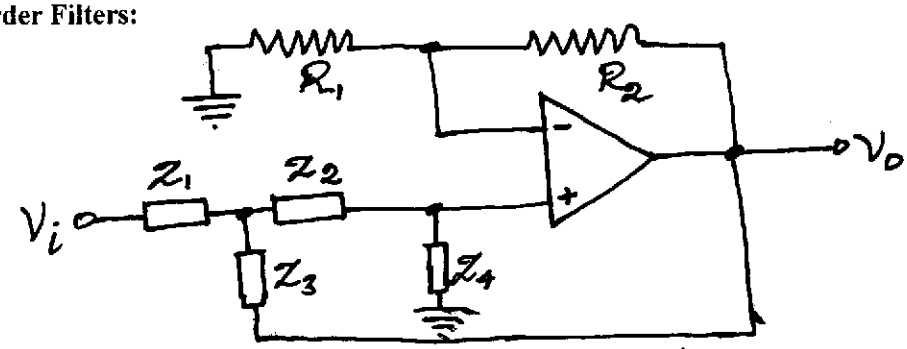
Cut-off frequency and mid-band gain values in the case of low-pass filter are; $f_C = \frac{1}{2\pi R_2 C_1}$

$$A_v = -\frac{R_2}{R_1}$$

Cut-off frequency and mid-band gain values in the case of high-pass filter are; $f_C = \frac{1}{2\pi R_1 C_1}$

$$A_v = -\frac{R_2}{R_1}$$

~~First~~ Second-Order Filters:



Second-order Butterworth Filter

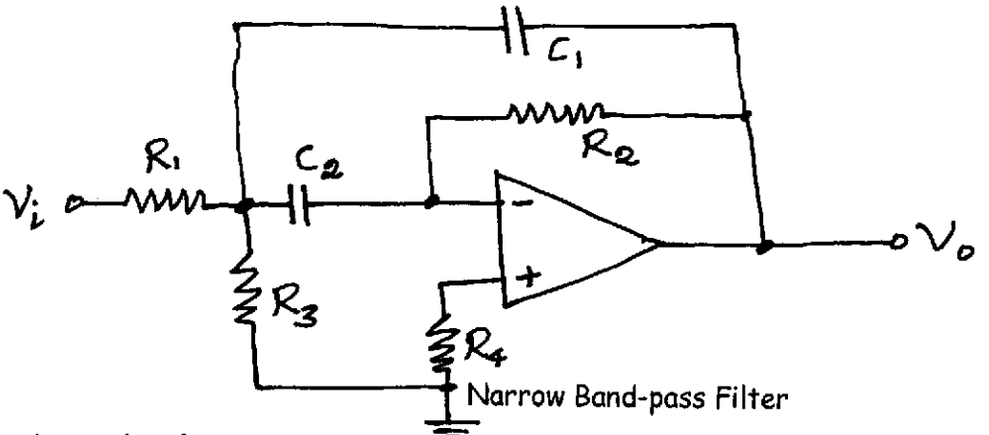
Butterworth filters, also called maximally flat filters, offers a relatively flat pass and stop band response. This has the disadvantage of relatively sluggish roll-off.

In the above Fig –

- ✓ If $Z_1 = Z_2 = R$ and $Z_3 = Z_4 = C$, we get a second-order low-pass filter
- ✓ If $Z_1 = Z_2 = C$ and $Z_3 = Z_4 = R$, we get a second-order high-pass filter

The cut-off frequency and pass-band gain values are given by; $f_C = \frac{1}{2\pi RC}$ $A_v = 1 + \frac{R_2}{R_1}$

A *narrow band-pass filter* required multiple feedbacks, as shown in the following Fig.



Narrow Band-pass Filter

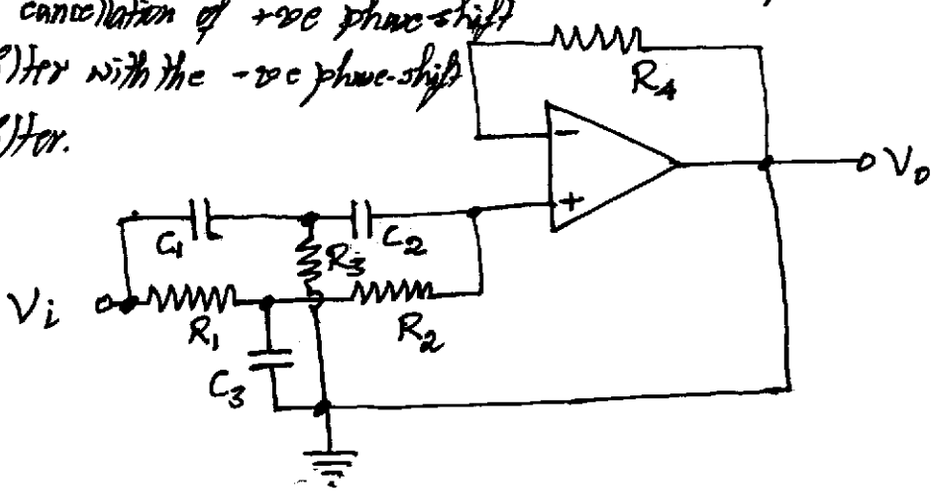
At very low frequencies, C_1 and C_2 offer very high reactance. As a result, the input signal is prevented from reaching the output. At very high frequencies, output is shorted to the inverting input. Hence, again there is no output. At some intermediate frequencies, the gain provided by the circuit offsets the loss due to the potential divider $R_1 - R_3$.

The resonant frequency is given by; $f_R = \frac{2Q}{2\pi R_2 C}$ where, Q is the quality factor.

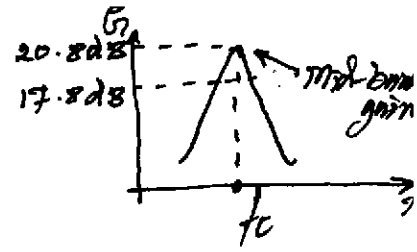
For $C_1 = C_2 = C$, the quality factor is given by; $Q = [R_1 R_2 / 2R_3]^{1/2}$

The voltage gain is given by: $A_v = \frac{Q}{2\pi R_1 f_R C}$

A *second-order narrow band-reject* filter uses a twin-T network as shown in the following Fig. A twin-T network offers very high reactance at the resonance frequency and very low reactance at frequencies off-resonance. In the circuit diagram, very low frequency signals find their way to the output via low-pass filter (formed by $R_1 - R_2 - C_3$); and very high frequency signals find their way to the output via high-pass filter (formed by $C_1 - C_2 - R_3$). Hence, in an intermediate band of frequencies, both filters will not pass signals to the output; due to cancellation of +ve phase-shift of high-pass filter with the -ve phase-shift of low-pass filter.



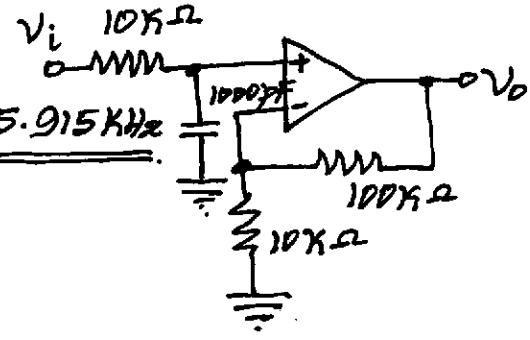
Second-order Band-reject Filter



If $R_1 = R_2 = R$, $R_3 = R/2$ and $C_1 = C_2 = C$, $C_3 = 2C$, with $0 \le R4 \le (R_1 + R_2)$ then; $f_R = \frac{1}{2\pi RC}$

Problem: *Refer to the first-order low-pass filter of following Fig. Determine the cut-off frequency and the gain value at four times the cut-off frequency.*

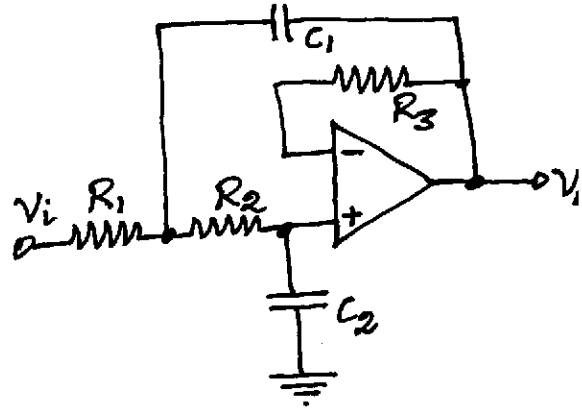
Solution:



- $f_C = \frac{1}{2\pi \times 10 \times 10^3 \times 1000 \times 10^{-12}} = \frac{10^5}{2\pi}$ Hz = 15.915 KHz
- $A_v = 1 + \frac{100 \times 10^3}{10 \times 10^3} = 11 =$ 20.827 dB.
- Gain at cut-off frequency; = 20.827 − 3 = 17.827 dB.
- Gain at frequency, four times the cut-off frequency is; 3×4 = 12dB below the value of mid-band gain. Therefore, gain at four times the cut-off frequency = 20.827 − 12 = 8.827 dB.

Problem: *The following Fig shows a second-order low-pass filter. Calculate the values of R_1, R_2, C_1, C_2 and R_3, if the cut-off frequency of the filter is 10 KHz, Q-factor is 0.707 and input impedance not less than 10 KΩ.*

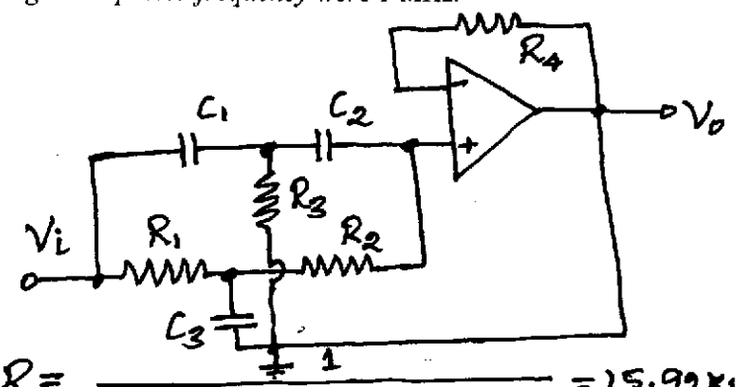
Solution:



- For $R_1 = R_2 = R$; $f_C = \frac{1}{2\pi R\sqrt{C_1 C_2}}$
- $Q = \frac{1}{2}\sqrt{C_1/C_2}$
- For $Q = 0.707$; $C_1 = 2C_2$
- For input impedance of 10KΩ; $R_1 = 10K\Omega = R_2$
- $f_C = \frac{1}{2\pi \times 10 \times 10^3 \times C_2\sqrt{2}}$ $\Rightarrow$ $C_2 = 0.0011\,\mu F$ & $C_1 = 0.0022\,\mu F$. each
- To have equal DC resistance, between Op-Amp inputs & ground; $R_3 = R_1 + R_2 = 20K\Omega$.

Problem: *Design an Op-Amp based twin-T band-reject filter having a notch frequency of 100 KHz. Specify the small-signal bandwidth of the Op-Amp if the highest expected frequency were 1 MHz.*

Solution:



o Notch frequency $f_R = \frac{1}{2\pi RC}$

where; $R_1 = R_2 = R$; $C_1 = C_2 = C$;

$R_3 = R/2$; $C_3 = 2C$.

o Let $C = 0.0001\mu F$. This gives; $R = \frac{}{2\pi * 0.0001 \times 10^{-6} * 100 \times 10^3} = 15.92K\Omega$

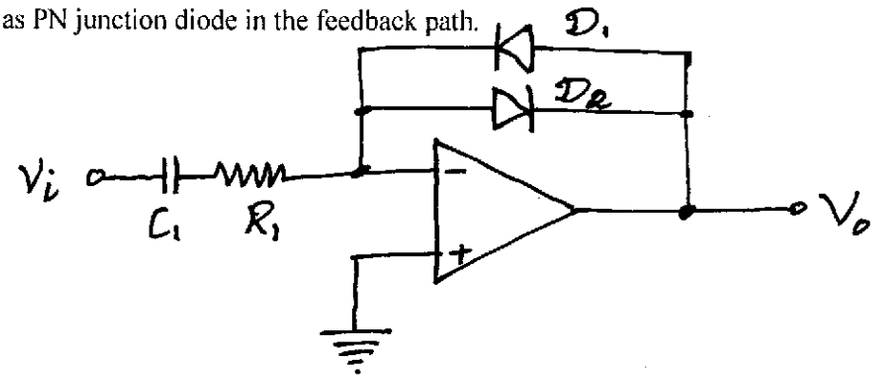
Hence; $R_1 = R_2 = 15.92K\Omega$ $R_3 = 7.96K\Omega$ $C_1 = C_2 = 0.0001\mu F$

$C_3 = 0.0002\mu F$

$\therefore R_4 = R_1 + R_2 = 31.84K\Omega$.

NON-LINEAR AMPLIFIER:

In a non-linear amplifier, the gain value is a non-linear function of the amplitude of the signal applied at the input. For example, the gain may be very large for weak input signals and may be very small for large input signals. A simple method to achieve non-linear amplification is by connecting a non-linear device such as PN junction diode in the feedback path.



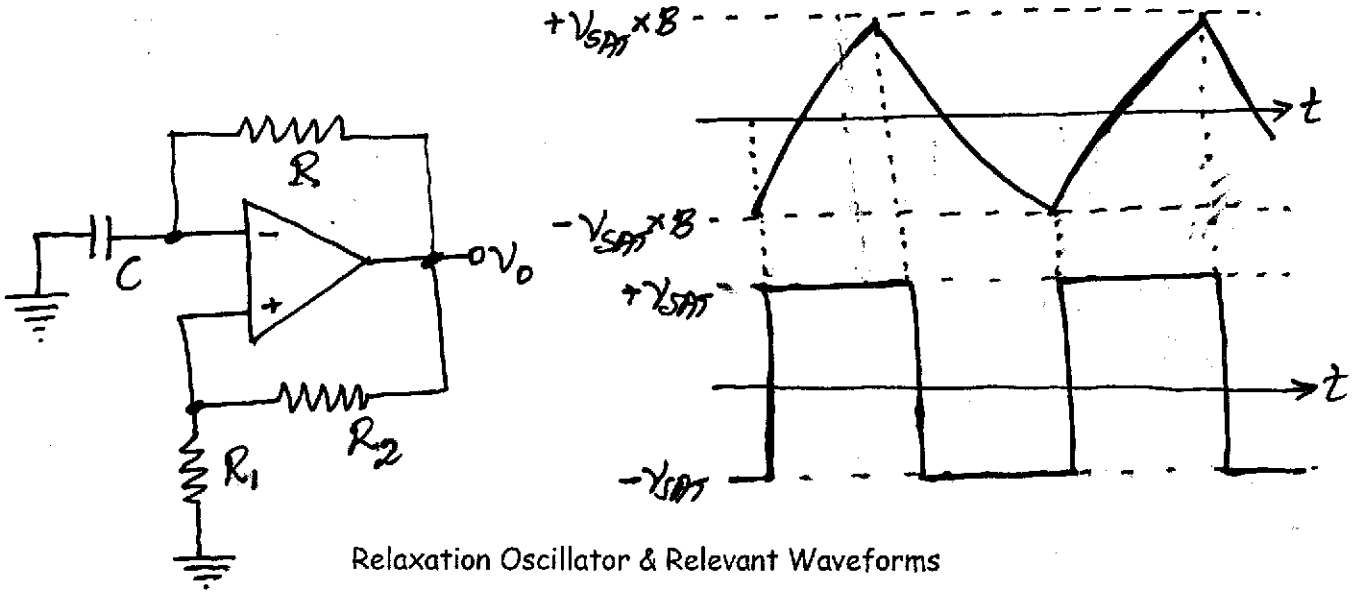
Non-linear Amplifier

For small values of input signal, diodes act as open circuit and the gain is high due to minimum feedback. When the amplitude of the input signal is large, diodes offer very small resistance and thus gain is low.

Application of non-linear amplifier is in AC bridge balance detectors.

RELAXATION OSCILLATOR:

Relaxation oscillator is an oscillator circuit that produces a non-sinusoidal output whose time period is dependent on the charging time of a capacitor connected as a part of the oscillator circuit.



Relaxation Oscillator & Relevant Waveforms

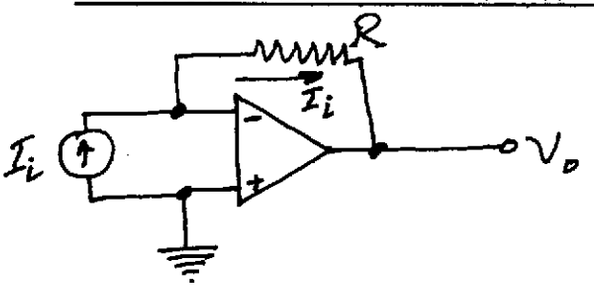
Assume that, the output is initially in positive saturation. As a result, voltage at non-inverting input of Op-Amp is $+V_{SAT} * R_1 / (R_1 + R_2)$. This forces the output to stay in positive saturation as the capacitor C is initially in fully discharged state. Capacitor C starts charging towards $+V_{SAT}$ through R. The moment the capacitor voltage exceeds the voltage appearing at the non-inverting input, the output switches to $-V_{SAT}$.

Now, the voltage appearing at the non-inverting input changes to $-V_{SAT} * R_1 / (R_1 + R_2)$. The capacitor starts discharging and after reaching zero, it begins to discharge towards $-V_{SAT}$. Again, as soon as it becomes more negative than the voltage appearing at the non-inverting input of the Op-Amp, the output switches back to $+V_{SAT}$.

The expression for the time period of the output rectangular waveform is given by; $T = 2\,RC \ln\left(\frac{1+B}{1-B}\right)$ where, $B = R_1 / (R_1 + R_2)$. By varying the value of resistor R, the time period of the output waveform can be varied.

CURRENT-TO-VOLTAGE CONVERTER:

Current-to-voltage converter is nothing but a transimpedance amplifier. An ideal transimpedance amplifier makes a perfect current-to-voltage converter as it has zero input impedance and zero output impedance.



Current-to-Voltage Converter

The circuit is characterized by voltage shunt feedback with a feedback factor of unity. The expression for output voltage is given by; $V_o = I_i * R * (\frac{A_{OL}}{1+A_{OL}})$

For $A_{OL} >> 1$; $V_o = I_i * R$ Also, $Z_{in} = (\frac{R}{1+A_{OL}})$ and $Z_o = (\frac{R_o}{1+A_{OL}})$

where, R_O is the output impedance of the Op-Amp.

VOLTAGE-TO-CURRENT CONVERTER:

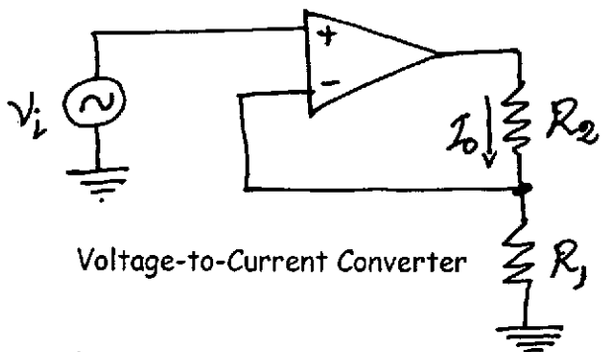
Voltage-to-current converter is a case of a transconductance amplifier. An ideal transconductance amplifier makes a perfect voltage-controlled current source or a voltage-to-current converter.

The circuit is characterized by current series feedback. The expression for output current is given by; $I_o = \frac{V_i}{R_1+[(R_1+R_2)/A_{OL}]}$ For $A_{OL} >> 1$, $I_o = \frac{V_i}{R_1}$

Closed-loop input impedance; $Z_{in} = R_i * \left(1 + A_{OL} * \frac{R_1}{R_1+R_2}\right)$

where, R_i is the input impedance of the Op-Amp.

Closed-loop output impedance; $Z_o = R_1 * \left(1 + A_{OL} * \frac{R_1}{R_1+R_2}\right)$



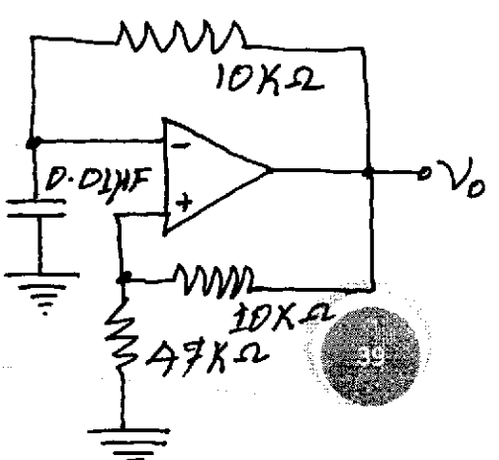
Voltage-to-Current Converter

Problem: *Refer to the following relaxation oscillator circuit. Determine the peak-to-peak amplitude and frequency of the square wave output; given that, the saturation output voltage of the Op-Amp is ±12.5 V at power supply voltages of ±15 V.*

Solution:

The feedback factor

$$\beta = \frac{47\times10^3}{47\times10^3+10\times10^3} = 0.825$$



∘ The time period T is given by; $T = 2RC \ln\left[\frac{1+\beta}{1-\beta}\right]$

$= 2\times10\times10^{3}\times0.01\times10^{-6} \ln\left[\frac{1+0.825}{1-0.825}\right]$

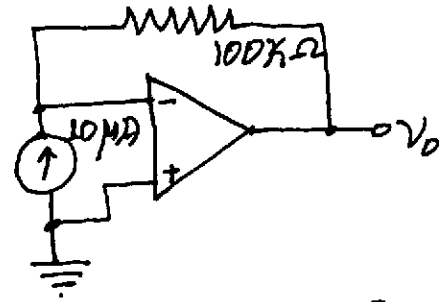
$= \underline{0.469 \text{ ms.}}$

$\therefore f = \frac{1}{0.469\times10^{-3}} = \underline{2.13 \text{ KHz}}$.

Peak-to-peak amplitude of output $= 2V_{SAT} = \underline{25 \text{ V.}}$

Problem: *For current-to-voltage converter shown in the following Fig, determine output voltage, closed loop input and output impedances; given that the Op-Amp has open-loop transimpedance gain of 100,000, input impedance of 1 MΩ, and output impedance of 100 Ω.*

Solution:



∘ Output voltage, $V_o = 10\times10^{-6}\times100\times10^{3}$

$= \underline{1 \text{ V.}}$

∘ Closed-loop input impedance, $Z_{in} = \frac{R}{1+A_{OL}} = \frac{200\times10^{3}}{1+100,000}$

$= \underline{1\ \Omega}$.

∘ Closed-loop output impedance, $Z_o = \frac{R_o}{1+A_{OL}} = \frac{100}{1+100,000}$

$= \underline{0.001\ \Omega}$.

By: MAHESH PRASANNA K.,

DEPT. OF CSE, VCET.

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